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Design and Implementation of Nine Level T-Type Inverter with Minimal Components

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ABSTRACT

The multilevel inverters are resourceful in producing a voltage waveform with superior-quality staircase counterfeit sinusoidal and depressed harmonic distortion. Several conventional topologies are proposed to realize the MLI however, the limitations of these topologies may involve more DC sources, Complex control circuit and power-switching devices, which in turn, increases the cost and size of the inverter. These drawbacks can be eliminated with the combined topology by cascaded H-Bridge and T-Type inverter. As compared with the established multilevel topologies the recommended topology having a reduced number of DC sources, power-switching devices, component count level factor, more efficient, and cost-effective. The proposed MLI is a blend of a single-phase T-Type inverter and an H-Bridge module made of sub switches. This article incorporates the design and simulation of the multilevel inverter with staircase PWM technique. Further, the 9-level is examined with different combinational loads. The proposed inverter is stable during nonlinear loads, and it is well suited for FACTS and renewable energy grid-connected applications. An operational guideline has been explained with correct Figures and tables.

KEYWORDS:Multi-Level Inverter (MLI), Half height method, Equal phase method, Total harmonic distortion (THD), T-Type inverter

1. INTRODUCTION

Multilevel inverters are the inverters in which the output of the inverter will have more than one level and as number of levels increase the output voltage is closer to sinusoid and gradually the THD decreases. As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel inverter not only achieves high power ratings but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high-power application. The concept of multilevel inverters has been introduced since 1975. The term multilevel began with the three-level inverter. Subsequently, several multilevel inverter topologies have been developed. However, the elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregates these multiple dc sources in order to achieve high voltage at the output.

MLI's incorporate with power semiconductor components and various DC links to build up staircase waveform tends towards sinusoidal. Mainly three traditional multilevel inverter topologies have existed: they are neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs). CHB-MLI having high voltage and power levels also more reliable, it requires more power semiconductor switches [2],The topology in [3] suggested a basic structure with eight unidirectional and one bidirectional switch to produce 15 levels, A Square T-Type topology was proposed in [4] to produce seventeen levels with four DC power sources. In [5] modular multilevel converter, many modules can be connected in series parallel combination to produce higher number of levels but number of capacitors required is more, The circuit in [7] is a nine-level inverter with twelve switches; three different frames are cascaded in [8] to get the desired nine-level output with ten switches.

STRUCTURE OF PAPER

In this paper, a 13-level MLI topology is presented this topology's main benefit is having reduced THD without increasing the output levels. This 9 level T-Type inverter topology is well-suited for the high and medium power applications such as FACTS, UPS, active filters and renewable energy sources. This work is organized as follows: In Section I, the introduction of the paper is provided along with the structure, important terms, objectives and overall description. Section II describes the T-Type inverter topology. Section III elaborates the various

Control Techniques used. Section IV Describes results and discussion and Section V summarizes the work

OBJECTIVES

1. To select the most suitable inverter topology with least components to make it economic in order to generate desired AC voltage waveform.
2. To generate higher steps in the AC vo1tage waveform so that the THD (Tota1 Harmonic Distortion) of the obtained wave is within the defined standards. Higher the output leve1s, lesser is the %THD.
3. To Simulate the designed circuit using MATLAB.

2. NINE LEVEL T-TYPE INVERTER

1. T-Type Inverter Topology

The circuit diagram of proposed T-type Multi-Level inverter cascaded with hybrid H-bridge inverter.

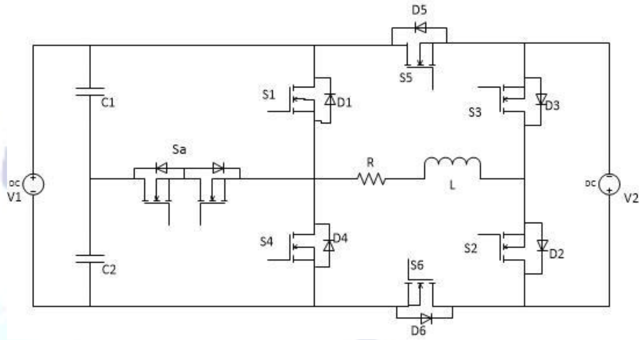

Fig. 1 Circuit diagram of 9-level inverter

The structure of the proposed 9 level inverters is incorporated with two DC sources V1, V2, and six unidirectional switches from S1 to S6 along with bidirectional switch Sa and two Capacitors C1, C2 which are connected in a blend of single-phase T-Type inverter and a module of H-Bridge made of sub switches are depicted. The specific arrangement reduces the additional DC source requirement also simplifies the number of switches needed. For a superior comprehension of working and the functioning of the introduced topology, various working modes have been represented along with conducting power electronic devices and path of load current I0 as depicted.

2. Load Design

AMPERE 0.25 HP (180 W) Single Phase AC motor

Specifications:

RMS Input voltage = 230 V

Peak Input voltage = 325.2 V

Speed = 1440 RPM

Frequency = 50 Hz

Power factor = 0.7

Power Output of motor = $\frac{Hp}{4} = \frac{746}{4}$ = 186.5 W

RMS output current = $\frac{Po}{Vrms} = \frac{186.5\ W}{230\ V}$ = 0.81 A

Peak output current = I rms * √2 = 1.14 A

Peak output voltage = Vrms * √2 = 325.2 V

Impedance = $\frac{Vm}{Im}$ = 285.21 Ohm

Power factor = $\frac{Active\ \ power}{Apparent\ \ power}$ = $\frac{I^2R}{I^2Z}$ = $\frac{R}{Z}$

Cos (Ø) = $\frac{R}{Z}$

0.7 = $\frac{\text{R}}{285.21}$

R = 199.64 Ohm

$$Z^2 = R^2 + Xl^2$$
$$Xl^2 = Z^2 - R^2$$
$$Xl = \sqrt{(Z^2 - R^2)}$$

XL = 203.68 Ohm

2*pi*f*L = 203.68

L = $\frac{203.68}{2*3.14*50}$

L = 0.64 H

3. ModesofOperation

In this portion, the proposed inverter operation is explained through the various modes of output voltage levels produced in a steady-state. In this, the DC source voltage (VDC) is equally shared by the two DC link capacitors C1 and C2 with equal magnitudes, i.e., VC1 D VC2 D VDC/2.

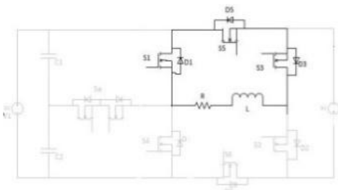

Fig:2(a)Mode 0 operation

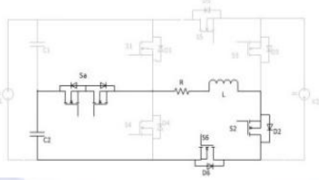

Fig:2(b)Mode 1 operation

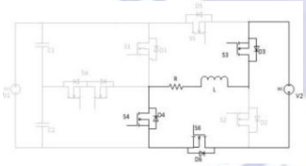

Fig:2(c) Mode 2 operation

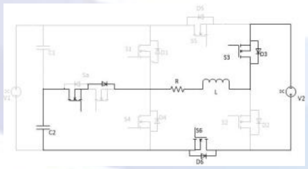

Fig:2(d)Mode 3 operation

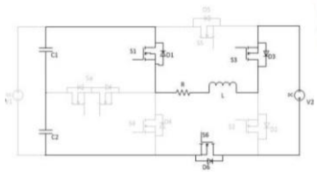

Fig:2(e) Mode 4 operation

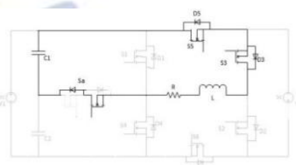

Fig:2(f)Mode 5 operation

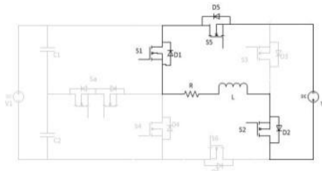

Fig:2(g) Mode 6 operation

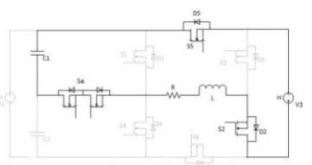

Fig:2(h)Mode 7 operation

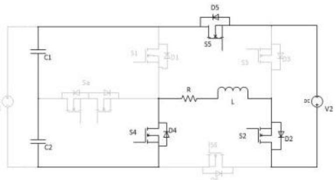

Fig:2(i)Mode 8 operation

TABLE I

MODES OF OPERATION OF PROPOSED INVERTER

Modes	Path of load current Io	Output voltage
Mode – 1	C2- Sa- D8-load- D2-S6-C2	+81.6 V
Mode - 2	V2-S6-D4-load-S3-V2	+162.5 V
Mode – 3	V2-S6-C2-Sa-D8-load_S3-V2	+244.1 V
Mode – 4	V2-S6-C2-C1- S1-load_S3-V2	+325 V
Mode – 5	C1-S5-D3-load- Sa- D7-C1	-81.6 V
Mode – 6	V2-S2-load-D1-S5-V2	-162.5 V
Mode – 7	V2-S2-load-Sa-D7-C1-S5-V2	-244.1 V
Mode – 8	V2-S2- load-S4-C2-C1-S5-V2	-325 V
Mode - 9	S5, S3, S1	0 V

Switching States of 9 Level T type Inverter

The expressions for the number of DC sources n, number of output levels NLev, the required number of power switches NS, necessary number of diodes Nd, number of DC-link capacitors required Ncap, peak voltage (VDC)max

TABLE II

SWITCHING STATES OF NINE LEVEL INVERTER

Switching levels	Sa	S1	S2	S3	S4	S5	S6	Output voltage V
L1	0	1	0	1	0	0	1	**+325 V**
L2	1	0	0	1	0	0	1	**+244 V**
L3	0	0	0	1	1	0	1	**+162.5 V**
L4	1	0	1	0	0	0	1	**+81.25 V**
L5	0	0	1	0	1	0	1	**0 V**
L6	1	0	0	1	0	1	0	**-81.25 V**
L7	0	1	1	0	0	1	0	**-162.5 V**
L8	1	0	1	0	0	1	0	**-244 V**
L9	0	0	1	0	1	1	0	**-325 V**

3. MODULATION TECHNIQUES

Modulation is the technique used to change the state of a power electrical device. The multilayer output waveform is produced by the modulation techniques. To produce the required output waveform, each modulation approach generates a unique switching pulse.

1. EQUAL PHASE ANGLE MODU1ATION TECHNIQUE

In this technique the switching ang1es are distributed average1y over the full complete cycle ranging from 0 – 360 degrees. The equation to calculate the switching angles by Equal Phase angle

Ws = s ∗ (180/ M) where s = 1, 2, 3, 4…, 2M M = Number of output voltage levels

2. HALF HEIGHT MODULATION TECHNIQUE

The half-height method is employed to reduce the harmonic content at the output voltage side. This modulation technique is proposed in this work which gives better total harmonic distortion as compared to equal phase modulation technique. In the Half Height switching modulation technique the total period (0 – 360 degrees) of the output waveform are divided into four quadrants

4. SIMULATION MODEL

Nine level t-type inverter circuit is simulated in computer using MATLAB software and the circuit is analysed forresistive-inductive load with the help of fundamental switching techniques to compare the results. The THD obtained in this simulation is within the IEEE519 standards limit without using any filter circuits. The circuit is also simulated with equal phase angle and half height method techniques and the THD obtained is compared. Through the half height method, we obtained the lowest THD. The Simulink circuit model of the symmetrical inverter and its gate pulse simulation circuits are shown.

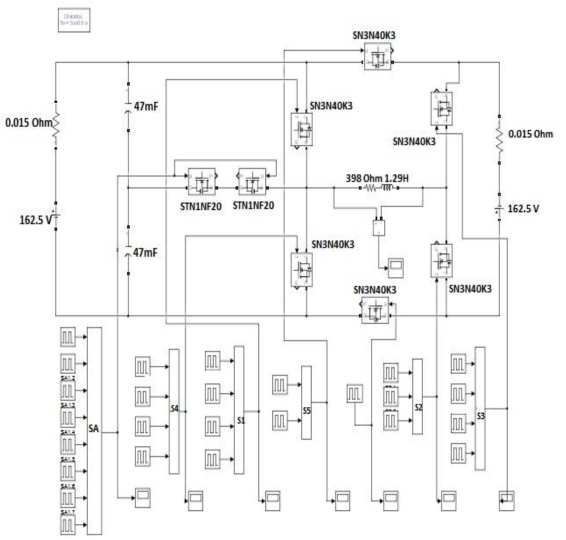

Fig. 2 MATLAB Simulink Model of 9-level T type inverter

MOSFET used = STN1NF20 and STN3N40K3

Battery internal resistance = 0.015 Ohm

Load resistance = 398 Ohm

Load inductance = 1.29 H

Resonating frequency = 50 Hz

Switching frequency = 400 Hz

Battery specifications = 12V 5Ah Battery connected in series to get 162 V

Gate Pulses for Equal Phase Angle Method

Fig. 3 Gate pulse for 9-level T type inverter equal phase angle method

Gate Pulses for Half height Method

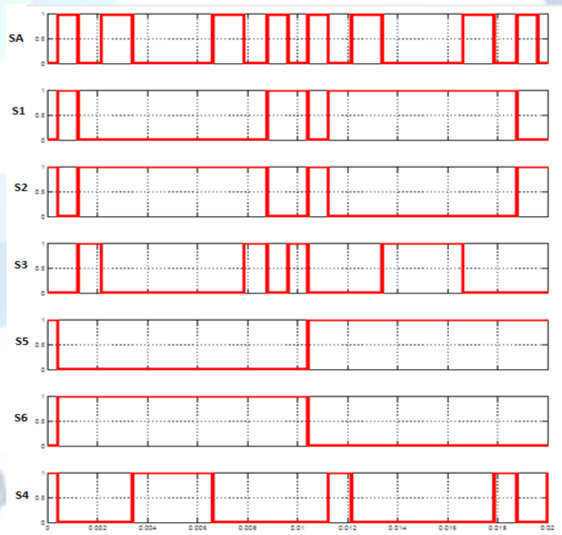

Fig. 4 Gate pulses for 9-level T type inverter half height method

RESULTS

Output Voltage

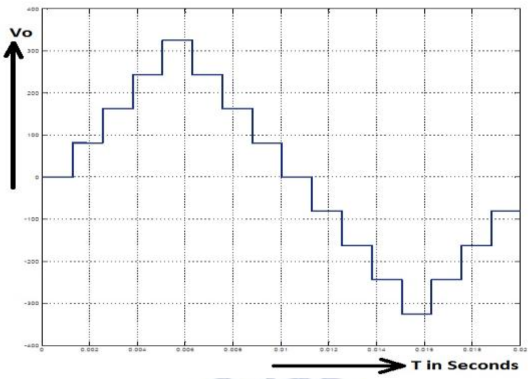

Fig. 5 Output voltage for 9-level inverter using equal phase angle method

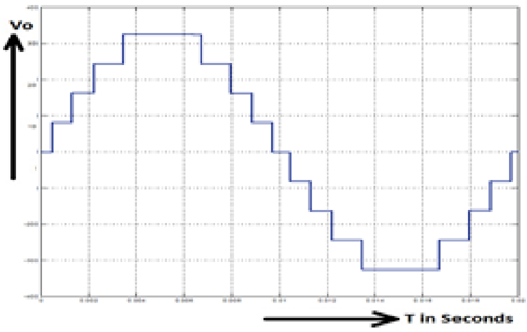

Fig. 6 Output voltage for 9-level inverter using half height method

B. THD Analysis

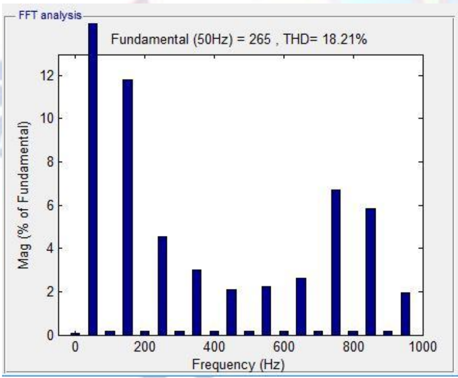

Fig. 7 FFT analysis for equal phase angle method

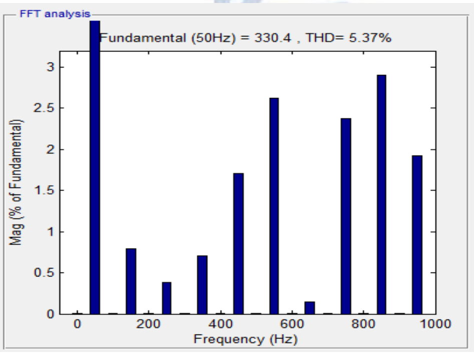

Fig. 8 FFT analysis for equal phase angle method

TABLE IIII

SWITCHING STATES OF NINE LEVEL INVERTER

Modulation technique	Type of load	THD % Volltage
Equal phase angle modulation technique	R-L Load	18.21%
Half height modulation technique	R-L Load	5.37%

5. CONCLUSION

This work mainly concentrates on reducing number of switches and reducing total harmonic distortion. This 9-level T type inverter generates 9 (4 positive, 4 negative and one zero level) levels output waveform. Due to the use of fewer number of components, the circuit complexity, cost, voltage stresses on switches are reduced. The MATLAB simulatiois done for equal phase angle method and half height modulation technique. The comparison is done between equal phase method and Half Height modulation technique in terms of simulation results with RL loads considering the THD parameter to highlight the best performance of the 9-level T type inverter circuit with Half Height modulation technique. Thus simulation results show the better performance and superiority of the 9-level T type inverter circuit over the conventional multilevel inverter topologies. The THD value obtained for voltage is about 18.21% for RL load using Equal Step method and THD with same RL load using Half Height modulation technique about 5.37%. So there by concluding that THD using Half Height PWM technique is better. The presented MLI is accomplished with reduced THD and reduces number of switches. This MLI is well suited for renewable energy applications.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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