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Analysis of Cascaded H-Bridge 11-level Multilevel Inverter

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ABSTRACT

This study primarily focuses on the design and implementation of a topology for a three phase eleven level cascaded H-bridge multilevel inverter using a variety of switching mechanisms, with the goal of achieving higher efficiency. The primary goal of this effort is to increase the number of voltage levels available at the output while simultaneously reducing the complexity of the power circuit. With this suggested architecture, the Total Harmonic Distortion is reduced, as is electromagnetic interface EMI production, and high voltage is generated with a sine waveform that is extremely close to it. A number of different types of carrier pulse width modulation techniques are described in this paper, each of which reduces total harmonic distortion and improves the output voltage from the proposed architecture. POD modulation approaches also lower Total Harmonic Distortion. A number of H-bridges are stacked in a cascade configuration in order to raise the voltage level using various switching strategies. It has been discovered that this novel topology may be applied to three phase eleven level cascaded H-bridge inverters in order to get the best possible performance above the standard techniques. The eleventh level of the inverter is responsible for optimising this performance. A topology in cascaded form is used to improve the fundamental waveforms while simultaneously minimising the overall harmonic distortion. This is accomplished by utilising 60 IGBTs and switching is structured in a cascaded form. Modeling and simulation are carried out using the MATLAB 2018 software version.

KEYWORDS: Cascaded H-bridge multilevel inverter, total harmonic distortion THD, Electromagnetic Interface,different phase pulse width modulation,

1. INTRODUCTION

The most frequently encountered issue with dc to ac conversion is the quality of the waveform, which includes the presence of harmonics. All traditional inverters create a two-level output voltage (square wave), with more harmonic [1-3] components present than in the input voltage (square wave). In the case of rotating machines, the heat losses would be increased, and the parasitic torque would be created as a result of the harmonics. As a result, research has been initiated to find a solution to this problem, with the multilevel inverter architecture being one of the potential options.

There are several advantages to using a multilayer inverter [4-6], including the ability to produce output voltage with a lower dv/dt, reduced distortion in input current, and a low switching frequency. Furthermore, these multilevel inverters are categorised into three types: diode clamped, flying capacitor, and cascaded H-Bridge [7-9]. When it comes to diode clamped and flying capacitor multilevel inverters, the number of diodes and capacitors required is greater in both cases. As a result, the cascaded H-Bridge type multilevel inverter is the kind that is most usually used. When using this design, we may obtain a waveform that is almost sinusoidal by increasing the number of levels in the output voltage. Increases in the number of levels correspond to an increase in the number of H-Bridges that need to be cascaded. Generally speaking, each H-Bridge is composed of four switches, and the generalised formula for the number of levels is 2n + 1. The number n represents the number of H-Bridges. To obtain seven levels, for example, three level 5 bridges are necessary, and eleven level 5 bridges are required for a total of eleven levels. The rate of change of voltage (dv/dt) for each level of the eleven-level output is Vdc/5 for each level of the output. However, as the number of levels increases, the number of switches required increases, causing the cost of the inverter to increase. The hybrid H-Bridge type multilevel inverter is therefore presented to alleviate the difficulty associated with cascaded-Bridge architecture. A bidirectional switch and a Diode Bridge are linked at the input side of the circuit in this suggested topology, which is similar to that employed in the previous one. When we compare the cascaded H-Bridge multilevel inverter [10-12] to this switch, we may get the eleven level output with fewer switches by operating this switch in different combinations with other switches. With the help of the Matlab/Simulink software, the design and simulation of both cascaded and hybrid H-Bridge inverters are completed. In addition, the FFT analysis is performed in order to determine the total harmonic distortion (THD) for both topologies. The architecture and switching table for the same eleven-level output voltage were also examined in detail.

2. CONCEPT OF MULTI-LEVEL INVERTERS AND STAIRCASE WAVEFORM

A classification of inverters is based on the output waveform, and the four major types are as follows: square wave, quasi wave, two-level pulse width modulation inverter, and multi-level inverters [13]. In recent decades, multi-level inverters have become increasingly common in both the industrial and research sectors. Using power semiconductor switches in conjunction with direct current voltage sources, multi-level inverters may produce a stepped voltage waveform at the output that is very near to a sinusoidal waveform [14]. In order to generate a stepped waveform that is closer to a sinusoidal waveform, a correct driving circuit as well as isolated or nonisolated DC sources are used to regulate power semiconductor devices in multi-level inverters. The number of step levels at the output should be increased in order to approach the sinusoidal waveform without the need of an expensive passive filter and a large transformer [15-16]. According to the research [17-20], the advantage for which multi-level inverters are gaining popularity is their ability to reduce energy consumption.The staircase waveform produces lower harmonic and smaller dv/dt which results in minimization of bulky filters.

- The lesser common-mode voltage thus motor bearing stress get reduces.
- Electromagnetic interference is lower.
- Multi-level inverters draw low distortion current.
- If the asymmetrical sources are used then more levels can be generated with the equal number of switches, practically it can be possible by using different RES like solar photovoltaic, wind, fuel, cell, etc.

3. MULTI-LEVEL INVERTERS

MLIs follows the arrangement of power switches like IGBTs/MOSFETs/Thyristors along with capacitor fed voltage sources. The common three types of MLIs are:
(i) Diode/Neutral Clamped,
(ii) Capacitor-clamped/Flying capacitors and
(iii) Cascaded H-Bridge MLIs. Diode-clamped MLIs were introduced in 1981 by Nabae et al., where diodes are used to reduce the voltage stress, in which an n level inverter requires switching devices, input voltages and operating diodes of $(2n - 2)$, $(n - 1)$ and $n - 1 * (n - 2)$ in number respectively.

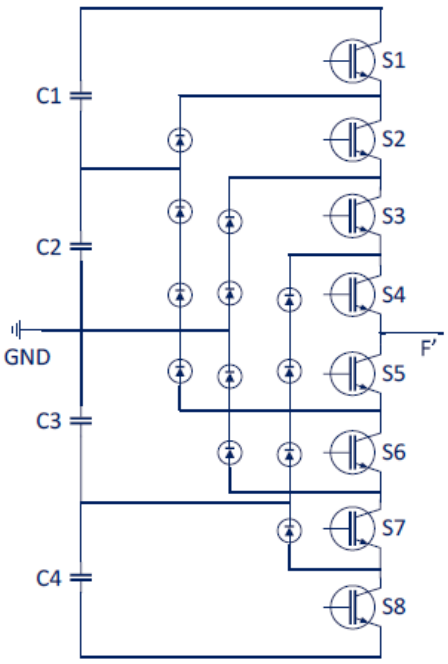

Figure 1. Circuit diagram of a diode-clamped MLI

However, in case of Capacitor-clamped MLIs, the voltage stress by controlled by capacitors instead of diodes in diode-clamped. An n level capacitor-clamped MLI must have switching devices and flying capacitors of (2n − 2) and n − 1 ∗ (n − 2) 2 respectively. The circuit diagrams of diode-clamped and capacitor clamped are given in the Figure.1 and Figure.2.

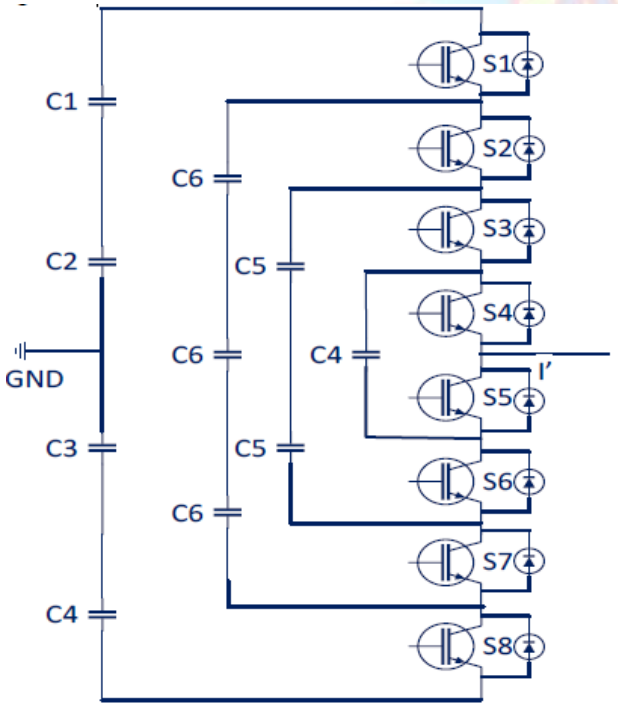

Figure 2. Circuit diagram of capacitor-clamped MLI

Cascaded H-Bridge Inverters

Essentially, an H-bridge inverter is a single-phase full bridge inverter equipped with four switching devices and a separate DC power source. H-bridges may generally yield voltage levels of Vdc, 0, and +Vdc when different combinations of switches are used, as shown in the figure. Normally, when two diagonal switches are turned on, the output voltage is +Vdc, and when the other two switches are turned on, the output voltage is Vdc. When all of the switches are turned on at the same time, the output voltage is zero. Illustration of a single H-bridge inverter, and illustration of the output waveform of the H-bridge inverter, respectively..

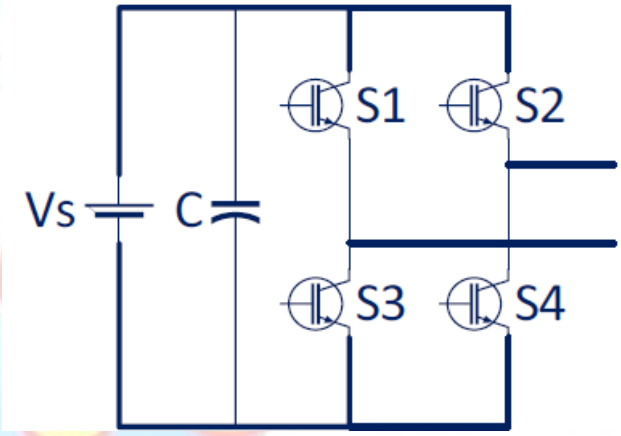

Figure 3. Circuit diagram of H-bridge inverter

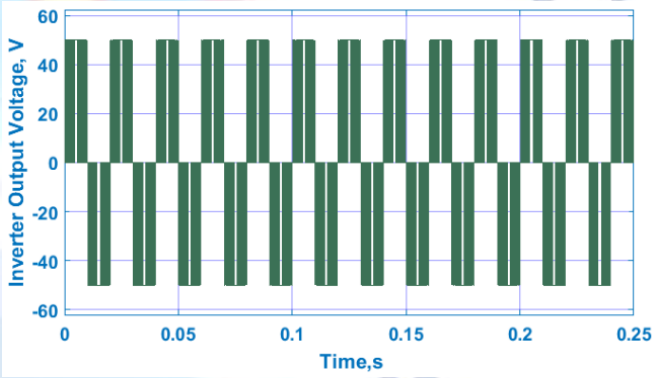

Figure 4. Three-level output voltage/output voltage of a single H-bridge

4. 11-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

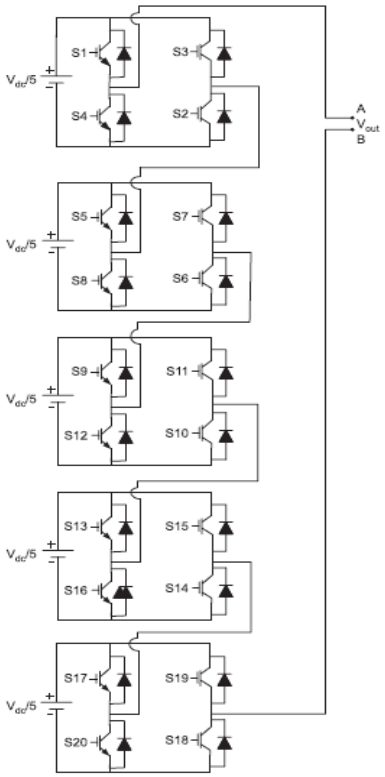

Figure 5: 11 level cascaded H-Bridge multilevel inverter

The Figure 5 represents the 11 Level cascaded H-Bridge multilevel inverter configuration. In this configuration, total five H-Bridges have connected in series to get the output voltage and each bridge consists of four switches. The total number of switches required is 20. The voltage source connected to each bridge is Vdc/5. The number of gate driver circuits and protection circuits for switches is 20 each. However, the rate of change of voltage (*dv*/*dt*) for each level is Vdc/5. Hence, the stress on switches wouldddecrease.

Table 1 gives the switching sequence for 11 level cascaded H-Bridge multilevel inverter. To get the corresponding level the number of switches to be active is clearly shown in this table. For example, to get zero output voltage the load must be short circuited by all the bottom switches and the path is A-S2-S4-S6-S8-S10-S12-S14-S16-S18-S20-B. To get 2Vdc/5, the switches S5 & S6 should be ON. In this manner by giving the gate pulse to required switches for particular level, we can get 11 level outputvoltage

Table 1
Switching Sequence for 11 Level Cascaded H-Bridge

Voltage level	*Switching operation*																			
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{20}
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$V_{dc}/5$	1	1	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2V_{dc}/5$	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3V_{dc}/5$	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
$4V_{dc}/5$	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
V_{dc}	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
$-V_{dc}/5$	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$-2V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
$-3V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
$-4V_{dc}/5$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0
$-V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1

5. MATLAB MODELING AND SIMULATION RESULTS

The simulink model of an 11-level cascaded H-Bridge multilevel inverter with a resistive load is seen in the preceding image. The load is assumed to be 10 kW in this case, and all of the relevant characteristics are taken into consideration. It is necessary to utilise the repeating sequence block in order to provide timing

sequence for switches, and the same is true for bottom switches that do a NOT operation.

The output voltage and current waveforms of a cascaded H-bridge multilevel inverter with a resistive load of 10 kW are depicted in the diagram to the right. Because of the resistive load, the current waveform is similar to the voltage waveform, but the magnitude is different.

Using a cascaded H-Bridge inverter, the FFT analysis of the voltage is shown in figure 8. According to the results of the FFT analysis of voltage, the total harmonic distortion (THD) is equal to 8.85 percent.

The output voltage and current waveforms of a cascaded H-bridge multilevel inverter for an RL load of 10 kW are depicted in the image to the right. Because of the existence of the inductor in the load, we can see a difference in the current waveform in this case.

In the example above, the simulation for an 11 level hybrid H-Bridge is given, and the difference between cascaded and hybrid H-Bridge is the number of switches, which can be noticed immediately. The same load is linked in this location as well. Additional diode bridge circuits have been attached to the input side switches for improved performance.

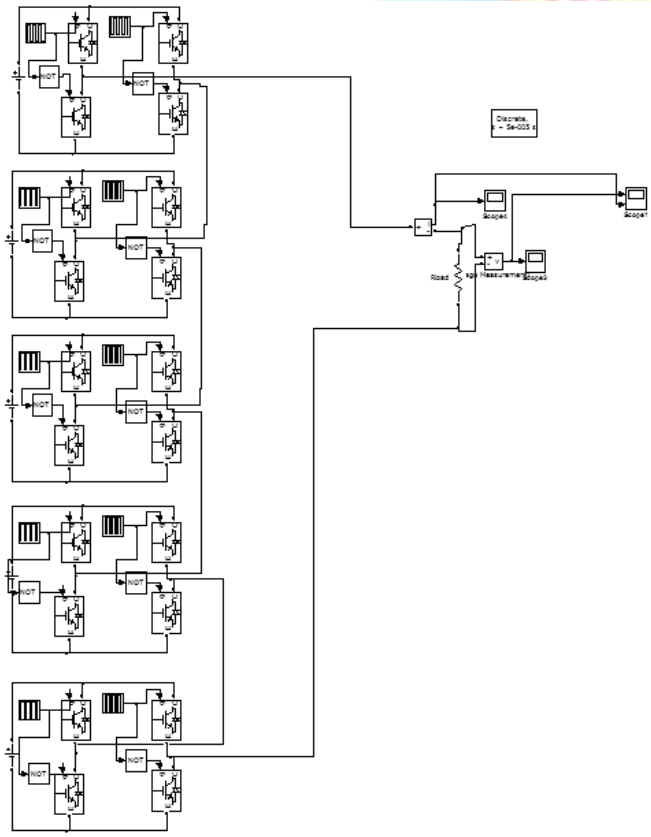

Figure 6: Matlab/simulink model of 11 level cascaded H-Bridge Multilevel inverter

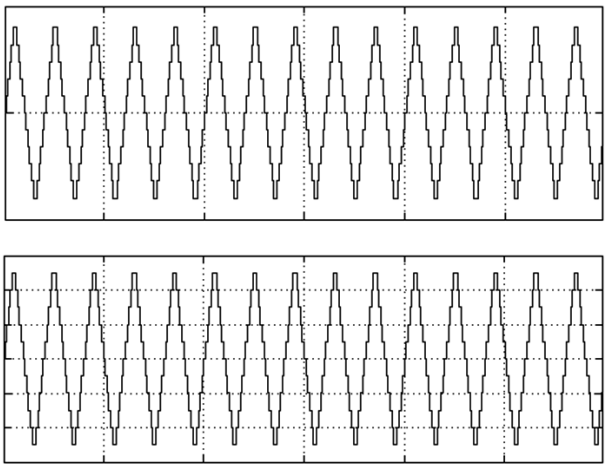

Figure 7: Output wave forms of 11 level cascaded H-Bridge multilevel inverter for R load

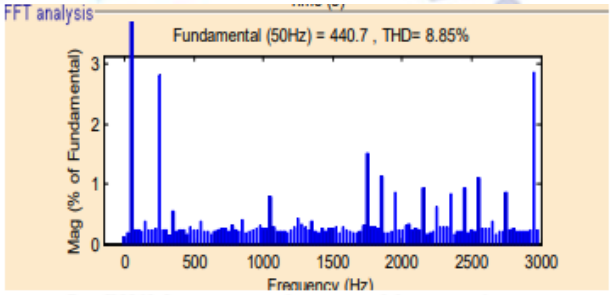

Figure 8: FFT analysis of voltage for eleven level hybrid H-Bridge

Table 2. Overall Analysis of Cascaded H-Bridge Inverters

Inverter Level Type	No. of H-Bridges	Total no. of Switches	THD, %
Three	1	4	52.12
Five	2	8	34.58
Seven	3	12	21.71
Nine	4	16	13.83
Eleven	5	20	8.85

6. CONCLUSION

Several types of Cascaded H-bridge multi level inverters are discussed in this thesis. Three-level, five level, seven level, nine level, and eleven level Cascaded H-bridge multi-level inverters are discussed in this thesis. In comparison to diode-clamped and capacitor-clamped MLIs, cascaded H-bridge MLIs have several advantages. A three-level inverter is achieved by using a cascaded H-bridge circuit with four switches. The SPWM control approach is used to

control the four switches in each H-bridge configuration. For this reason, two H-bridges, three H-bridges, and four H-bridges (in cascade) are necessary in order to get five-level, seven-level, and nine-level inverters, among other things. The input DC voltage of 50V applied to each H-bridge frames a symmetrical MLI when applied to each H-bridge. The simulation modelling of all four layers of MLIs is completed in the manner depicted in the images of Chapter 5. Table 2 displays the total harmonic distortion (THD) values for all four different levels of inverters. The eleven-level MLI, which requires four Cascaded H-bridges and has a lower THD value of 8.85 percent than the other four, is the least expensive of the four.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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