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# Design and Analysis of 4K Real Time Display System on FPGA Implementation

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## ABSTRACT

***An FPGA implementation to combine and analyse multi-channel independent films and rebuild a 4K real-time display. The video system can accept multi-channel FHD (1920 x 1080 pixels) films, process each channel, then rebuild and show the combined video up to 4K (3840 x 2160 pixels). We use parallel processing and a hardware-based framework to ensure great efficiency and low latency. To provide real-time display, each channel video may be processed independently and shown in 4K format. The Xilinx Spartan-6 FPGA module controls the input, video reconstruction, and output operations. High-speed memory chips and a ten-layer PCB enable effective video data caching and signal integrity. Real-time UHD implementation on FPGA can be utilised for contemporary surgery, patient monitoring, diagnostics, office meetings, video surveillance, etc.***

*KEYWORDS- FPGA; multi-channel video; UHD video; real-time video*

## 1. INTRODUCTION

Video is the next information carrier. Cameras, tablets, and even phones can record video. The several source videos necessitate too many monitors, making simultaneous analysis of all video data impossible. To solve the problems of multi-channel video data real-time processing. Moreover, with the advancement of hardware and video processing, the use of 4K (3840x2160) screens is expanding. In some applications, such as modern surgery, patient monitoring, and diagnostics, multi-channel video processing is required to maximise the 4K screen's efficiency.

As a result, most current multi-channel display devices are PC software-based, rendering them impotent to process the ever-increasing amounts of data and visual resolution. As a result, FPGA-based hardware with multi-thread and real-time processing capabilities may be a perfect answer to these issues. Parallel video processing is ideal for high-speed, multi-tasking applications.

Many researchers now focus on FPGA video processing. This is due to the FPGA's flexibility, efficiency and low power consumption. Weiguo Zhou and Yunhui Liu provide an FPGA-based picture mosaic algorithm for processing camera video. Peng Sun presented a video fusion using CPU + FPGA architecture that can efficiently

speed up the process. Luis Araneda and Miguel Figueroa presented an FPGA-based digital video stabilisation architecture.

However, the above efforts are for a low-resolution video channel. A new architecture is needed to process FHD or UHD videos. Fast processing, low power consumption, and reliable performance can be achieved with FPGA-based design. The proposed solution uses hardware architecture to address the requirement of real-time video processing. Architecture: FPGA core processor, SiI9616 video processor, ARM coprocessor, and DDR3 memory. The SiI9616 video processor can decode, encode, and enhance several video formats.

The parallelism video processing technique with DDR3 storage can be implemented in FPGA. System states are analysed by ARM coprocessor. Clearly, the implementation can support 4K resolution.

The video processing is complex. Basic processing based on FPGA hardware design was required from the start, such as video scaling, Gamma conversion, and on-screen display (OSD). These earlier efforts used FPGA architecture to process real-time FHD video sequences at 60 frames per second (fps), which helped develop multi-channel video merge. The speed of DDR3 storage is also important for 4K real-time video processing. So we used Verilog code to build the DDR3 driver and manage the video storage process. Based on the memory mechanism, Verilog can implement all arithmetic. They are all one channel video processing. However, processing multi-channel videos at the same time requires rethinking video management and DDR3 SDRAM storage strategies. The approach will consider four to nine channel videos, which is substantially more data than earlier efforts. The balanced, distinct channel data transition, timing design, and display stability must be seriously examined. With the support of earlier research, a novel hardware architecture for high-performance multi-channel video processing was built.

The rest paper is organized as follow: Section 2 presents an over view of implementation architecture, Section 3 will demonstrate the implementation result and Section 4 concludes the work.

## 2. PROPOSED SYSTEM

The proposed system aims at a low-resolution video channel. A new architecture is needed to process FHD or UHD videos. Fast processing, low power consumption, and reliable performance can be achieved with FPGA-based design. The proposed solution uses hardware architecture to address the requirement of real-time video processing.

To process higher resolution videos, a faster hardware board system is required. A nine-path real-time video data processing solution is presented in Fig. 1. It can also seamlessly integrate two High Definition (HD) video channels and deliver them to a new designed higher performance hardware system. The new system can analyse higher resolution movies and create 4K real-time videos, which is the implementation's core.

For 4K video processing, the new video processing board storage data throughput rate is up to 25.6Gbit/s. The Xilinx FPGA XC6SLX150 core video processor has 147K logic cells, which is enough for video processing. The new system also offers hardware-based video processing such as HDMI signal decoding and encoding, noise reduction, video smoothing, and picture enhancement. ARM Cortex A9 can assess video states and control the full implementation.

The new board system has two parts: hardware implementation and HDL implementation.

### Hardware implementation architecture

The new processing board has two HDMI video inputs and two HDMI video outputs, a Xilinx FPGA XC6SLX150 core processor, SiI9616 video processors, an ARM 9 coprocessor, Ethernet ports, and DDR3 memory that can drive DDR3 memory at 25.6Gbits/s. Moreover, ARM 9 is the system's controller. So the ARM 9 will set up the SiI9616 and talk to the FPGA. Ethernet is a valuable connector for online control and communication with the system. Fig. 2 depicts the processing board's structure.

The HDMI video input module can send differential signals to the SiI9616. HDMI signals are anti-interference. The HDMI interface is also smaller than the DVI digital interface. The HDMI video data is standard. So, to simplify FPGA processing and ensure fast decoding of HDMI videos, HDMI format data will be converted to parallel data. The SiI9616 processor can convert parallel data to 12-bit true colour. Intuitive hard process core can convert the format

It's like the input module. A 36-bit parallel visual output from an FPGA video processor drives the SiI9616 processor. Because the implementation must support 4K films, the parallel data speed is around 268MHZ. The

speed for a 1080p FHD movie is merely 148.5MHZ. So, 4K video timing should be more careful. Finally, the decoded HDMI 4K definition video will be displayed.

The Xilinx FPGA XC6SLX150 core processor implements the video processing algorithm and manages multi-channel video data streams.

The SiI9616 video processors have a digital processing core that converts video formats and improves images. It accepts any input format up to 4K resolution. The video processor can reduce mosquito noise, smooth video, and enhance detail. It all starts with the firm core design. So the video latency will be greatly minimised.

The ARM 9 Coprocessor is the system controller. To control the implementation, the image analysis and top-level operating platform should be built. To configure the SiI9616 processor, write video data to the FPGA, and analyse the key image and FPGA state.

Control commands can be sent via Ethernet ports. Wireless Fidelity can manage multi-channel video displays (WIFI).

The video data will be stored in DDR3 memory. The design has 4GB of video data storage. The outside video data arrives in a separate clock. But their operation speed is slower than DDR3. So FIFOs will be added to the system to match DDR3 operation speed. Also, the DDR3 memory is driven by an FPGA core.

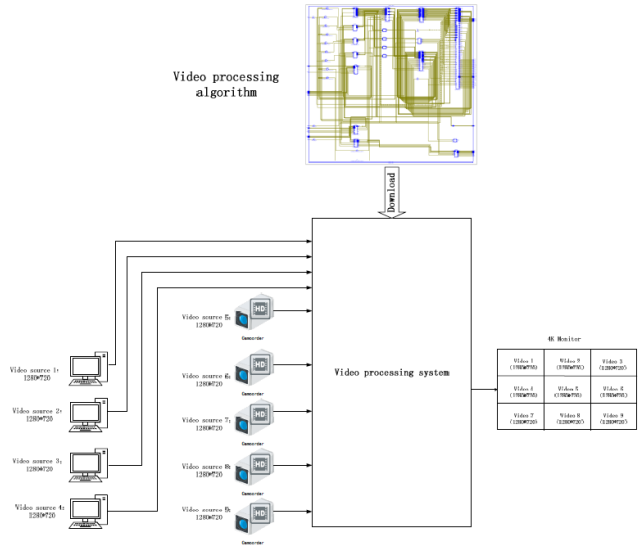


Fig. 1. The function overview of the whole system

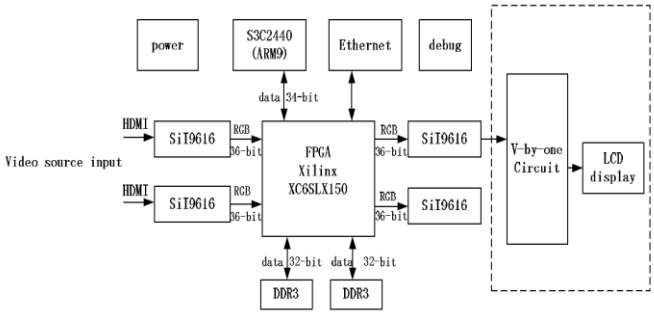


Fig. 2. The processing board architecture

**HDL Implementation Architecture**

The ISE software runs the video processing algorithm and simulation. Design and simulation of video data timing and storage method. The ISE application will then create the bit-stream file. The next step is to download the file into the board and start debugging it. Fig. 3. A visual processing arithmetic module, DDR3 controller, DDR3 driver and output controller module were integrated in the design.

The video processing board can receive and send two video channels. The video input channels are fully independent. Thus, the time of the two channel videos is not synchronised. A preprocessing module can improve the colour and picture quality while reducing noise. FIFO is appropriate for dealing with the multi-clock issue that comes with multi-channel video processing. The configure module is in responsible of converting control words into module parameters. It manages both video data write and read procedures. The DDR3 driver module directly drives the DDR3 IP-core. States are generated by the output controller module. To process a steady frame, precise timing is required. The HDL implementation's video processing arithmetic module. Fig. 4.

Controlling time is crucial when processing two path movies, since it determines the image processing order and storage block design. The calculating storage parameters module calculates video storage addresses, video read/write numbers, and frame packing parameters. The video storage map will stabilise Parameters for configuring video dispatching time can be obtained. Each frame of the movies must be filtered and denoised. That is followed by storing the video data. To make 4K resolution movies, the output data controller must be configured.

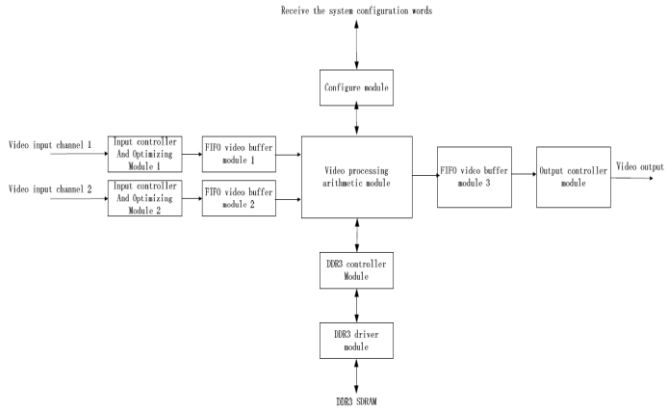


Fig. 3. HDL implementation architecture

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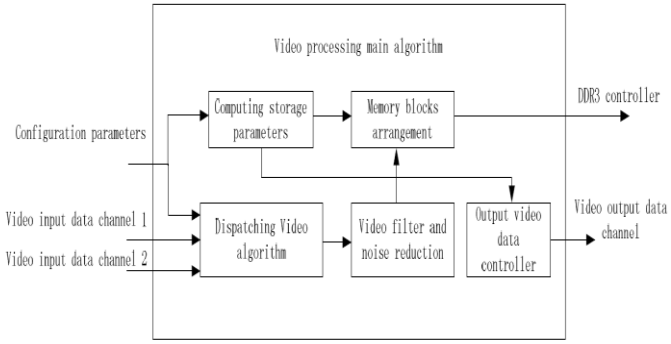



Fig. 4. A block diagram of video processing arithmetic module

## 3. EXPERIMENT RESULT

The platform is designed to handle multi-channel footage and show 4K real-time films. The algorithm can be boarded. Figure 1 depicts the video processing board's construction.

The HDL code is put onto the FPGA. The SiI9616 processor can decode, encode, and enhance video sources. The system may be built using video processing boards. So the system can analyse nine pathways' films at once and display the results in real-time on a 4K screen.

Derived from Verilog HDL. After designing and building the modules, a DDR3 gate level simulation was required. The graphic simulates DDR3 and multi-channel video data.

Figure shows the nine-path video processing outcome utilising the suggested video processing system design. Due to the video source limitations, we cloned the video sources and presented them again to demonstrate multi-channel video processing. Each input video source is 1280 (H) x 720 (V). For real-time processing and display, the input frame rate can approach 60 frames/sec.

The final video frame rate is 30 HZ due to the 4K screen's 30 HZ frame rate.

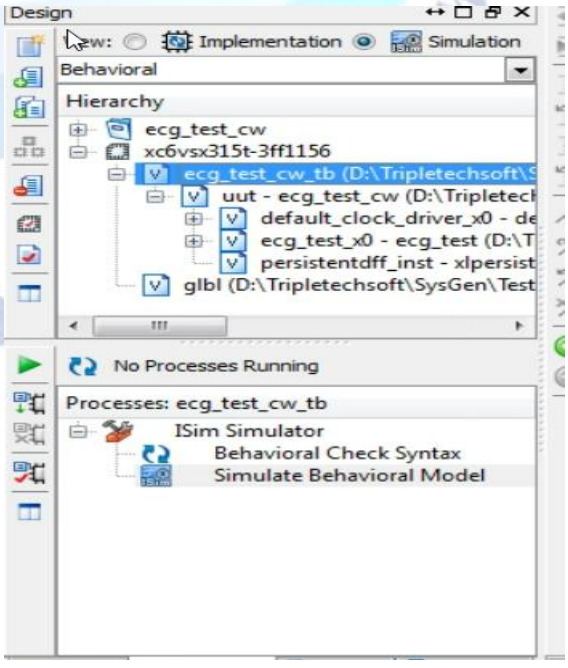
The technology can also handle higher resolution videos. Figure shows four paths of 1920 (H) x 1080 (V) films on a 4K screen. For real-time processing and display, the input frame rate can approach 60 frames/sec.

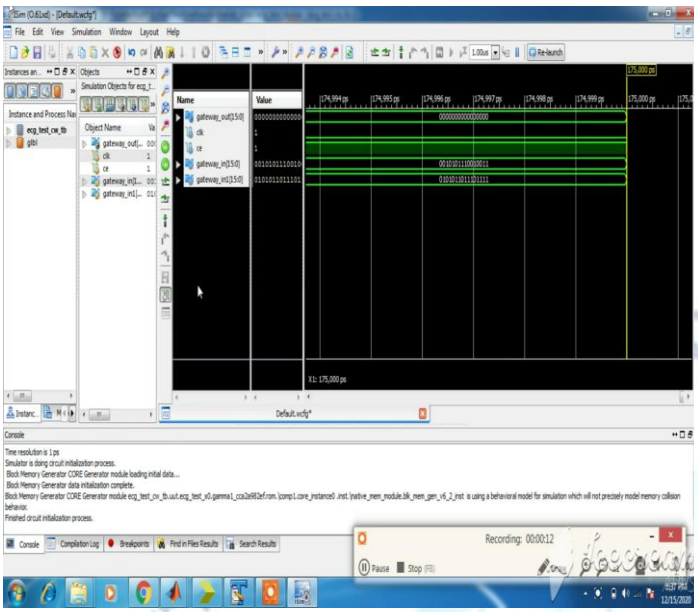
The system may scale films using the ARM to control the full system mode. As demonstrated in Figure, we may magnify the first channel video twice. Video processing hardware is designed. Thus, the time delay is minimal, ensuring real-time presentation.

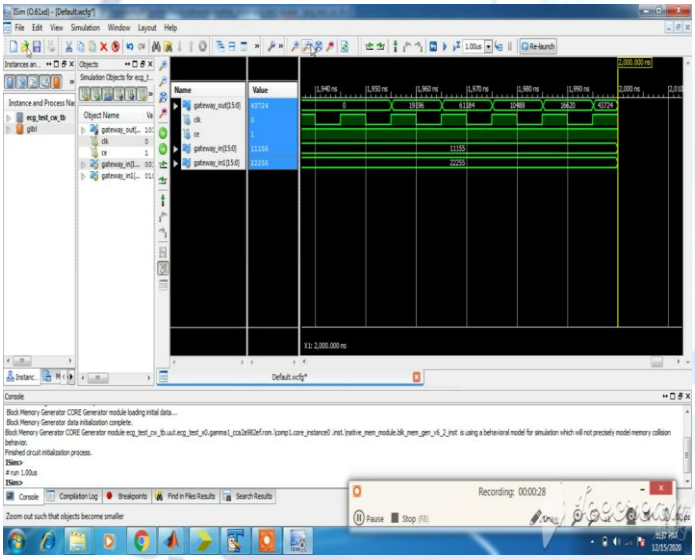
## 4. PERFORMANCE ANALYSIS

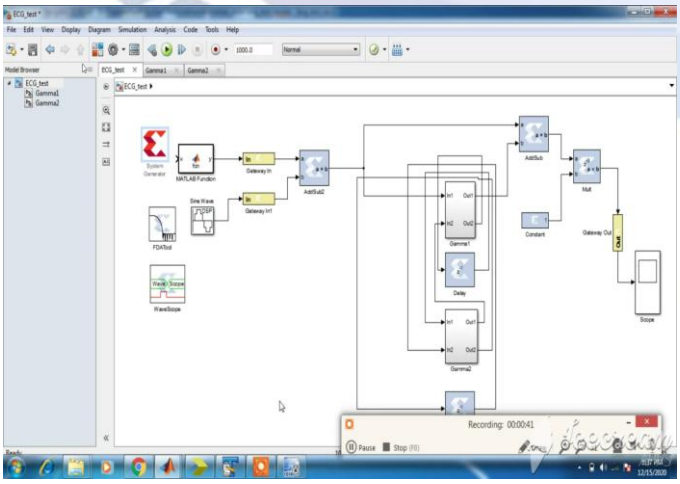
The Xilinx FPGA XC6SLX150 can process 4K real-time video. The hardware is designed. So, compared to a PC's hundreds of watts, the power usage will be little. As demonstrated in Fig. 10, the video processing board consumes just 1.943w. The FPGA meets the on-chip resource consumption. So the system can do considerably more arithmetic.

With the growth of VR/AR technology, several research breakthroughs have showed tremendous interest for video processing. Traditionally, video data is generated and processed by GPU and CPU. However, FPGA is excellent for constructing a flexible new architect to cope with multi-channel films and adjustable applications. Future display technology will rely on multi-channel video processing and real-time 4K display. Applications include contemporary surgery, patient monitoring, diagnostics, office meetings, and video surveillance.









## 5. CONCLUSION

To combine and analyse multi-channel independent videos while reconstructing 4K real-time video, this article introduced an FPGA implementation in this paper. This device has the capability of processing full-HD (1920x1080 pixels) movies and displaying the resulting result on a 4K UHD (3840 x 2160 pixels) screen, according to the manufacturer. Furthermore, it is capable of processing video input frames at a speed of up to 60 frames per second, allowing it to satisfy the needs of real-time applications. It is possible to minimise visual latency and power consumption while improving the durability of the video system by using a hardware design with HDL implementation.

While the traditional CPU + graphics processing unit (GPU) architecture is capable of dealing with rapid changes in video processing development by customising the processing structure, the FPGA solution has the ability to significantly improve the performance of multi-channel video processing and real-time display at a lower cost. VR/AR video processing, contemporary surgical procedures, patient monitoring, diagnostics and video surveillance are some of the applications for this technology.

### Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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