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First-Order Open Loop VCO-Based ADC with XOR Gates as differentiator

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ABSTRACT

In this paper, detail analysis for an open loop Voltage-Controlled Oscillator (VCO)-based ADC is discussed. The ADC includes a ring oscillator with several inverters to extract the phases. The circuit uses the VCO as an integrator in time domain and it uses the inverters in the VCO to perform multi-bit quantization. XOR gates are used to operate as differentiators and all the circuit is done through CMOS transistors. Mathematical analysis has been included to prove the ADC topology. Behavioral simulations have been added to validate the proposed architecture.

KEYWORDS: *Voltage-Controlled Oscillator, VCO ADC, Multi-bit quantization.*

I. INTRODUCTION

Voltage-controlled oscillator (VCO) based ADCs have attracted a lot of attention from the researchers over the last decade due to the fact that ring VCOs are able to replace opamp-based integrators which are challenging to design in scaled CMOS technology nodes. In addition to being highly digital, ring VCOs come with inherent multi-bit quantization. ADCs are widely used in medical applications such as Positron Emission Tomography (PET) [1] and Electrical Impedance Tomography (EIT) [2], to name but two. Also, ADCs are applied in applications which need current sensing to change an analog current to digital [3].

VCO output can be quantized by sampling the phase of each inverter stage with edge triggered flip-flops. VCO quantization noise depends on gate delay which scales down with technology, thus providing additional incentive to using VCOs as ADCs. Despite all these advantages, VCOs are highly nonlinear and sensitive to variations in process, voltage, and temperature (PVT). Several techniques have been introduced to mitigate the nonlinearity issue. Reference [4] presents an all-digital VCO ADC in which calibration is used to suppress VCO nonlinearity. A pseudorandom sequence is injected into a replica VCO through a DAC and correlated at the output to extract coefficients of nonlinearities in the VCO transfer function. [5] calculates the inverse of the VCO transfer function and adds the inverse function to the signal path to cancel VCO nonlinearity. However, accuracy of nonlinearity suppression for both [5] and [6] depends on accuracy of replica matching. Reference [7] presents a current feedback technique which linearizes delay cell in ring oscillator by reducing short circuit current. A two-stage architecture is presented in [8] that uses

a coarse flash ADC and sends the residue to VCO quantizer to suppress nonlinearity. The two-stage ADC is embedded inside a high-gain loop to reduce PVT sensitivity and interstate gain mismatch without requiring calibration. Process scaling enables higher performance and it is expected that the bandwidth of VCO-based ADCs gets improved. Although mentioned improvements as well as faster switching devices are brought about by process scaling, it poses difficulties in analog design as it lowers the voltage headroom. However, since VCO-based ADCs perform in a highly digital environment and are inherently digital, those process scaling challenges which happen for ADCs using amplifiers do not exist in VCO based ADCs.

ADC is an essential step in any digital signal analysis. Recently compressive sensing has been proposed to efficiently sample signal with fewer number of samples required by the Nyquist theorem. The original idea of CS that was developed by Donoho [19] was to investigate if it was possible to only select the necessary samples for lossy compression from analog during the A to D process. Since then the CS method has been applied in many fields from biomedical signals to image enhancement [20].

The CS method has since changed from Donoho's original idea; however, researcher have tried to deploy ADCs that work based on compressive sensing [9]. However, the quality of sampled signal in those approach is not comparable with that of the state-of-the-art ADCs. But some signal processing technique for CS recoveries has been proposed to accelerate the improve the recovery phase [10], and also for accelerating the recovery phase [11]. Those techniques widely have been used for sampling biomedical signals, namely ECG, MRI and heart rate [12-14].

In order to capture the time behavior of the measured signal, it is very important to decrease the sampling lag in the ADC module. In high fidelity fault detection application for sensitive actuators [15-16], the lagged time behavior causes incorrect alarm generation in the FDIR process. Because of this phenomenon, the modeling of the RW [17], the time accuracy of the ADC module plays an important role.

In this paper, we are analyzing an open loop VCO ADC for first-order noise shaping through a behavioral model. Although thermal noise of VCO can affect the performance of the circuit, it cannot affect the performance as the circuit does not have any feedback loop. In addition, having no feedback leads to have no delay loop as it appears in the other ADCs. The performance of the ADC is based on the phase quantization which is done through the VCO; and the number of quantizations is equal to the number of VCO stages. [18] presents a VCO ADC and used a feedback to increase the order of noise shaping and uses a switched ring oscillator as the second integrator, and the differentiator comes after it. In this paper, we applied that switched ring oscillator with XOR differentiator structure to form a first-order VCO ADC. The most important advantage of the proposed ADC is that it uses all the VCO stages for sampling and differentiating processes bringing about the capability of the circuit to serve higher center frequencies. In contrast, in other works specially those which use PFD as an edge detector for the pulses created by the differential VCOs, the phase information of one of the VCO stages is used to be processed rather than all the phases. Therefore, the center frequency of VCO should be reduced to not let the VCO be overflowed.

The rest of the paper is organized as follows: the principle operation of VCO is presented in Section II. In section III, the block diagram of the VCO ADC is presented and section IV analyzes the circuit. Section V introduces the digital calibration for VCO nonlinearities. Simulation results are shown in VI section and the rest which is the conclusion is presented in section VII.

II. VCO-Based ADCs

A VCO is a circuit that generates an oscillating signal whose oscillation frequency depends linearly on the input voltage x(t). In this paper, we will focus on VCOs with digital outputs. This means that the output signal will be always a 50% duty cycle square signal. The output oscillation frequency (fosc) can be expressed as:

$$f_{osc}(t) = f_0 + K_{vco}.x(t), \quad K_{vco} \le f_0 \qquad (1)$$

Where we can distinguish between a rest oscillation frequency (f0) term and a VCO gain (Kvco) term. The input signal x(t) is considered dimensionless and belonged to the ranged [-1,1] [21].

III. ADC Block Diagram

A simplified architecture of a conventional VCO-based ADC along with its operation principle is shown in Fig. 1. As mentioned in introduction section, this open loop ADC is based on a switched ring oscillator and the differential circuit in [18], but in this paper, the input of the switched ring oscillator (SRO) is not just a two-level input '0' and

'1' and it is called VCO rather than SRO. The VCO integrates the input, during a sampling period and represents it in phase domain. The digital output, d, is produced by a reset counter which counts the output edges of the VCO during a sampling period. The phase change of the VCO, [n] due to the input can be represented as:

$$\phi_x[n] = \int_{nT_s}^{(n-1)T_s} 2\pi\left(K_{vco}x[n] + f_{vco}\right)dx$$
$$\approx 2\pi\left(K_{vco}x[n] + f_{vco}\right)T_s \quad (2)$$
$$2\pi d[n] + \phi_q[n] - \phi_q[n+1]$$

Where K_{vco} and f_{vco} are the gain of the tuning curve and the center frequency of the VCO [11]. T_s is the sampling period and $\phi_q[n]$ is the quantization error, which is in form of time. High OSR is assumed and thus $x[n] = x(nT_s) \approx x((n-1)T_s)$. It is evident from (1) that the VCO-based ADC achieves first-order quantization noise shaping since difference of two consecutive errors are taken. Note that the quantization error that is in phase domain can be represented in form of a pulse.

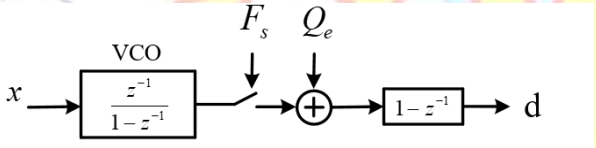

Fig. 1. Block diagram of conventional ADC.

IV. VCO ADC Analysis

One of the main components in every ΔΣ modulator architecture is the integrator. There are many different ways to implement an integrator, however, not all of them are suitable for all the possible situations. Typically, an analog integrator can be implemented through two ways: using an opamp-based integrator (Fig. 2(a)) or a transconductance-based integrator (Fig. 2(b)) [18]. As can be observed, both of them require analog circuits. The recent development of nanometer CMOS processes has led to major challenges in analog design. On the one hand, narrow-length devices show a high amount of non-desired effects (i.e. hot carrier injection, leakage and mobility effects, etc.) [24]. On the other hand, the threshold voltage has not been reduced at the same rate as the supply voltage. Consequently, transistor voltage headroom is lower and the number of transistors that can be stuck in series is very limited. As a result, analog design becomes difficult. In the opposite situation, digital circuits benefit from this scaling process in terms of area, speed and power consumption. Digital designs are less sensitive to transistor non-desired effects, mismatch phenomena and temperature, which makes them suitable for nanometer architectures [25]. Against this background, the current trend is towards replacing analog architectures by digital ones as far as possible.

As mentioned, the VCO is used for integrating on the input signal and it includes inverters in series. In this case, the VCO has 11 inverters. The output of this ADC is equal to:

$$d = x.STF + Q_e.NTF$$
$$STF = z^{-1}, NTF = 1 - z^{-1} \quad (3)$$

The whole circuit diagram of the ADC is shown in Fig. 3.

Based on this circuit, the VCO has been modeled by a differential inverters and DFF have been used in sampling the VCO outputs and the differentiator. As there are 11 inverters for the VCO, there will be 11 DFFs and XORs. In this open loop VCO ADC, all the VCO stages are used to get sampled and this helps with having low center frequency for the VCO which will be helpful for reducing the power consumption as there will be no need for applying a high frequency sampler.

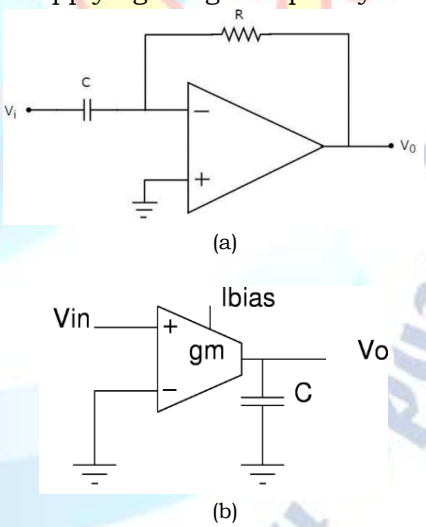

Fig. 2. (a) Opamp-based integrator, and (b) transconductance-based integrator

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V. Digital Calibration

As the VCO nonlinearity is one of the main issues with VCO-based ADCs, to cancel this or at least make it minimum, a digital circuit is placed in parallel with the ADC to compensate the nonlinearity [5,24]. [26] shows one of this type of implementation. The structure in [18] follows the structure shown in Fig. 4(c). The idea behind this topology is that the VCO distortion can be evaluated in a deterministic manner. If the VCO distortion calculation is done and we can figure out the shape of this distortion regardless of the input

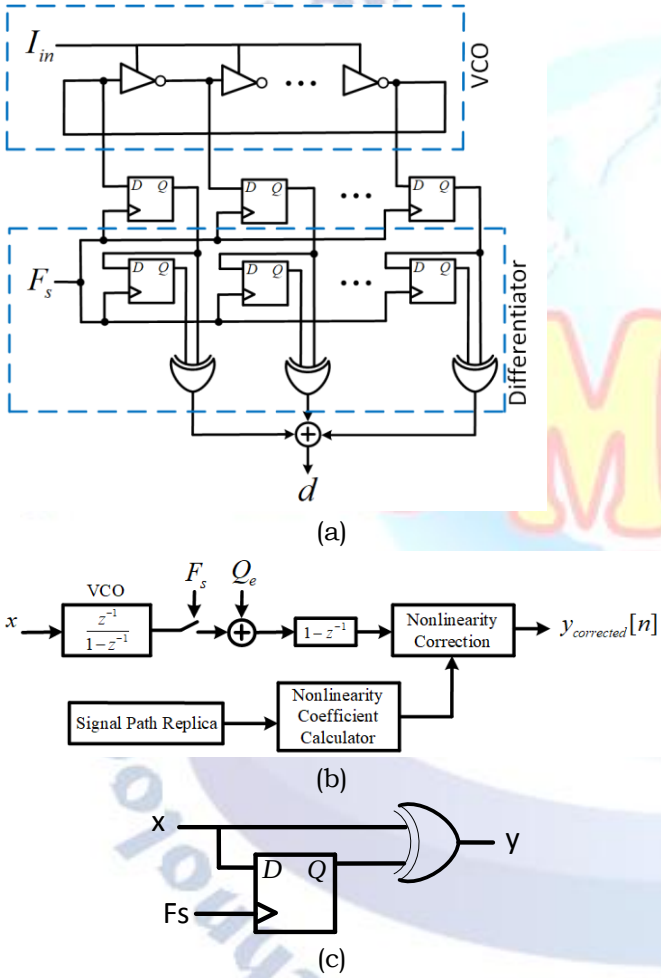

Fig. 4. (a) Circuit diagram of the VCO ADC, (b) differentiator Circuit, (c) VCO linearity correction by means of digital post-processing

signal of the system, after sampling, we will be able to cancel the distortion in the discreet form. To estimate the distortion of the VCO, the signal path through the converter is replicated. Then, the output of this replicated system is measured and the distortion components are estimated through digital circuits (non-linearity coefficient calculator). When they are calculated, they are subtracted from the digital output data y[n] to correct the non-linearity (non-linearity correction block) and get the corrected output data. The advantage of this technique is that it allows us to highly compensate the distortion of the VCO. For example, in [26], the third harmonic distortion (HD3) is reduced from -48.5dB to -80dB. However, there are three disadvantages. Firstly, the system area is remarkably increased due to the compensation logic required.

The compensation logic is composed of a signal path replica (as large as the converter signal path), and digital circuitry to calculate the distortion coefficient and correct the output of the system. This means that the area occupied might be doubled. Secondly, the required compensation logic supposes the design of complex circuits. Finally, these circuits may increase the power consumption of the system in a significant way [18].

VI. Simulation Results

To show the performance of the ADC, a behavioral simulation is done. For the VCO, 11 inverters have been used. The Gain for this VCO is equal to K_{vco} = 1µA/MHz. A center frequency of 100MHz has been chosen for the VCO. The input which is in current mode has the frequency of 50KHz and amplitude of 3µA. The ADC has a sampling frequency of 90MHz. It should be noted that the ADC parameters like the sampling frequency, input amplitude and the VCO gain should be designed to avoid overflow.

In the simulations, no thermal noise has been considered.

Fig. 5 shows the simulated spectrum of the ADC. The FFT has been normalized with respect to input signal amplitude. The ADC reaches to a SQNR of 60dB with first-order noise shaping.

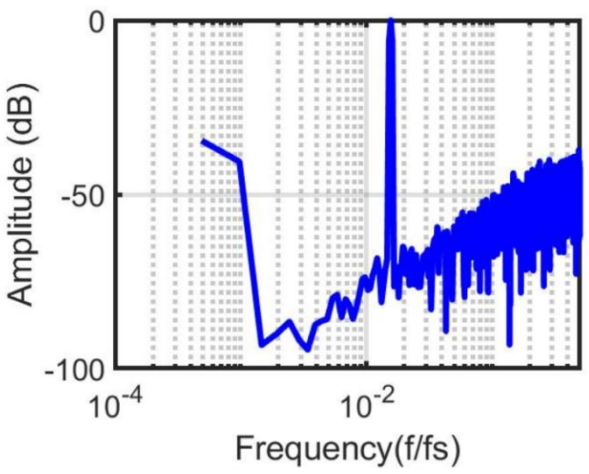

Fig. 5. FFT plot for the first-order VCO-ADC

VII. CONCLUSION

This paper presented an open loop VCO ADC which is highly digital and helps with the power consumption for the application needing low power dissipation. We explained the way for eliminating the issue of VCO nonlinearity. It is expected that the power consumption can get reduced through technology scaling as the nature of the circuit is digital. A behavioral simulation has been done to show the performance of this circuit and the FFT plot verifies the first-order noise shaping.

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