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Insights on Ternary Content Addressable Memory for Network Applications

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ABSTRACT

Ternary Content-Addressable Memory (TCAM) is a critical component in modern network systems, widely used for high-speed packet forwarding and classification tasks. This review paper presents a comprehensive survey of various TCAM architectures, highlighting their design principles, performance characteristics, and application domains. We explore traditional TCAM designs alongside recent advancements aimed at improving performance, reducing power consumption, and improving scalability. The survey covers different TCAM optimization techniques, including algorithmic improvements, hardware modifications, and hybrid approaches that combine TCAM with other memory technologies. Additionally, we examine the effect of TCAM on emerging networking paradigms such as software-defined networking (SDN) and network function virtualization (NFV). Through this review, we identify current challenges and potential future directions in TCAM research, providing valuable insights for researchers and practitioners seeking to leverage TCAM technology in next-generation network infrastructures demands.

KEYWORDS: Ternary Content-Addressable Memory (TCAM), Packet Forwarding, High-Speed Search

1.INTRODUCTION

Telecommunication is the passing on data over long distances using various technologies, like radio, optical, satellite, and wireless networks. Communication speed is a measure of how fast data can be sent and received over a communication channel, and it is usually expressed in bits per second (bps). Communication speed is important for telecommunication applications, as it affects the quality, reliability, and efficiency of the information exchange. Content-addressable memory (CAM) is a type of memory that allows fast searching of data based on its content, rather than its address. CAM can help improve communication speed in telecommunication applications, as it can perform parallel search operations in a single clock cycle, reducing the time and energy required for data lookup and retrieval. CAM can also support approximate matching, where a certain Hamming distance (number of mismatching bits) between a query pattern and the stored data is tolerated. This can enable faster and more flexible data processing, especially for applications that deals with noisy, incomplete, or uncertain information , such as genomics, image recognition, and natural language processing. CAM can also enhance the security

and privacy of telecommunication, as it can implement encryption and authentication schemes based on the content of the data, rather than its location or address. Content-Addressable Memory (CAM) is a specialized type of computer memory that allows for parallel search and retrieval of information based on content, rather than requiring an address. Unlike traditional memory, where data is accessed by providing a specific memory address, CAM allows for direct matching of data content. This feature makes CAM particularly useful in applications where rapid searching and retrieval based on content are essential. CAM is commonly employed in networking devices, such as routers and switches, to facilitate fast and efficient packet routing.

2. LITERATURE SURVEY

Prem Kumar, et al. proposal for a Ternary Content Addressable Memory (TCAM) utilizing Carbon Nanotube Field-Effect Transistors (CNTFETs) based on 32nm technology is presented as an alternative to the traditional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The research employs two models: Virtual Source CNTFET (VS-CNTFET) and Stanford CNTFET (S-CNTFET). An 8x8 TCAM array is constructed, and power and delay analyses are conducted. These findings are later compared with results obtained from MOSFET models: MOSFET-Low Power (MOSFET-LP) and MOSFET High-Performance (MOSFET-HP). Simulations are executed using Cadence Virtuoso 6.1.7-64b, 2018. The outcomes reveal that the average Power-Delay Product (PDP) of the VS-CNTFET TCAM array is 27.53% lower than that of the MOSFET-LP TCAM array and 23.32% less than that of the MOSFET-HP TCAM array. Additionally, the average PDP of the S-CNTFET TCAM array is 18.21% less than that of the MOSFET-LP TCAM array and 13.5% less than that of the MOSFET-HP TCAM array.[1]

Yen-Jen Chang, et al. addressed the issue of presence of large number of transistors in TCAM used in routing tables with a novel technique called Data Retention based TCAM (DR-TCAM). DR-TCAM aims to decrease the leakage power dissipated in TCAM memory by preserving the state of data. By leveraging the continuous nature of mask data, DR-TCAM dynamically adjusts the power source of mask cells, thereby reducing TCAM's leakage power without compromising the integrity of mask data. Simulation results conducted on TSMC 40nm technology demonstrate that DR-TCAM outperforms existing approaches. Compared to conventional TCAM designs, DR-TCAM achieves a remarkable 41% reduction in TCAM leakage power for real routing table scenarios. Moreover, it achieves an overall power reduction of approximately 12%.[2]

Esteban Garzón, et al. has introduced a novel non-volatile ternary content-addressable memory (TCAM) called the hybrid 10-transistor/2-Double-Barrier Magnetic-Tunnel-Junction (10T2DMTJ) TCAM, aiming for energy efficiency, reliability, and fast search operations. Our design features low-energy-demanding MTJs arranged within a simple voltage-divider-based circuit, accompanied by a straightforward dynamic logic CMOS matching network to enhance search reliability. Implemented in a 28nm FDSOI process, our NV-TCAM undergoes exhaustive Monte Carlo simulations for evaluation. Comparative analysis against previous NV-TCAM designs demonstrates superior performance: notably, our solution achieves a significantly lower search error rate (3.8 times less) and reduced write and search energy consumption (by 73% and 79% respectively). Additionally, this design exhibits a smaller area footprint, reduced by 74%. However, there is a trade-off of reduced search speed.[3]

Ruifu Zhang, et al. propose a novel magnetic skyrmion-based ternary Content-Addressable Memory (CAM) design, termed Sky-TCAM, aimed at providing low-cost, high-speed search capabilities for applications like network routers and machine learning. Each cell of this CAM consists of a 5T2R structure, integrating five transistors and two magnetic tunnel junctions (MTJs). By combining the search current polarity with the stored bit, the XOR logic is realized. In case of a mismatch, a skyrmion forms beneath one MTJ, causing discharge of the matchline (ML). While the energy-delay-product (EDP) for search operation is comparable to that of non-volatile (NV) ternary CAMs (TCAMs), Sky-TCAM exhibits the lowest EDP among all TCAMs evaluated, at 8.74 × 10−25 J · s. The findings suggest that Sky-TCAM holds promise for constructing low-power and low-latency computation applications.[4]

H. V. Ravish Aradhya, et al. noticed that conventional 6-T Static Random Access Memory (SRAM) cells based early TCAM architectures suffered from high power consumption. To solve this issue, researchers explored read-decoupled logic for multi-transistor SRAM, aiming to reduce power consumption. Hence, they proposed two TCAM architectures that demonstrate decreased power consumption compared to traditional TCAM designs. These architectures utilize SRAM cells with additional circuitry, and our approach integrates low-power 6-T and 8-T SRAM cells into the designs. The TCAM cell schematics were simulated and tested using Cadence Virtuoso with gpdk090 technology. Analysis of power consumption values and static noise margins (SNM) was conducted. Results showed a notable 67% decrease in cumulative power consumption for the low-power (LP) 8-T-TCAM compared to typical 8-T TCAM, and a 17% reduction for the single-ended 6-T TCAM compared to typical 6-T TCAM. These enhancements in power efficiency, combined with optimal SNM values across extreme temperatures, render these architectures versatile for many applications requiring low power consumption.[5]

Sadegh Rouhi, et al. found that, recent advancements have leveraged memristors as non-volatile memory elements within CAM structures, consequential in a notable reduction in power utilisation and offering promising prospects for the future of CAM technology. They introduce innovative architectures for memristor-based CAMs, showcasing significant optimizations in physical layout area, power consumption, and operational simplicity compared to prior similar works. Our primary objective is to present more advantageous options for manufacturers in the near future.[6]

The article by Krishna P. Gnawali introduces a high-speed, low-power memristor-based Ternary Content Addressable Memory (TCAM) designed for real-time and big-data applications. It proposes a novel memristive TCAM (MTCAM) cell that utilizes memristors as bit storage devices, paired with an ultra-fast match line sense amplifier to minimize search time. SPICE simulations conducted on 45nm technology demonstrate that the search delay for a 144-bit proposed MTCAM, operating at a supply voltage of 1V and a sense margin of 140mV, is 175 picoseconds, with a per bit search energy of 1.2 femtojoules. Compared to the fastest existing 144-bit MTCAM design, this proposed MTCAM is 1.12 times faster and consumes 67% less search energy per bit.[7]

Honglan Zhan, et al. to over-come the limitations of multi-port CAM and enhance search stage performance, introduces a high-speed and energy-efficient single-port (SP) CAM configured to achieve dual-port (DP) operation. Two novel peripheral schemes, namely CShare and VClamp, are proposed for different bit cell topologies, including the traditional 9T CAM cell and 6T SRAM cell. These schemes are extensively validated using various process corners, temperature ranges, and detailed Monte-Carlo variation analysis. Utilizing a 65-nm process and a 1.2 V supply, CShare and VClamp exhibit search delays of 0.55 ns and 0.6 ns, respectively, representing an approximate 87% reduction compared to state-of-the-art works. Furthermore, when compared with the recently introduced 10T BCAM, CShare and VClamp demonstrate energy reductions of 84.9% and 85.1% in the TT corner, respectively. Experimental results obtained from an 8 Kb CAM under a 1.2 V supply and across various corners reveal that CShare and VClamp improve energy efficiency by an average of 45.56% and 45.64%, respectively, compared to DP CAM.[8]

Kangqiang Pan, et al. introduce a novel design for ternary content addressable memory (TCAM) utilizing a resistive random-access memory (RRAM) array configured in a 2T2R setup. The proposed memory array employs a current-race (CR) sensing mechanism coupled with a match-line (ML) booster in the sensing amplifier (SA) to enhance energy efficiency, search speed, and tolerance to RRAM switching variation. Various innovations are integrated into the design to further improve its performance. For large TCAM arrays, two cascading schemes, match-line sensing amplifier (MLSA) direct cascading (DC) and SR-latch cascading (SRC), are proposed and compared in terms of search speed, energy efficiency, and MLSA noise margin. Additionally, a same clock phase cascading (SCPC) scheme is introduced to reduce latency in the cascading structure by aligning the evaluation phase of all stages in the same clock phase. Moreover, an RRAM-based

tunable delay element (RRAM-TDE) is incorporated into the TCAM design to offer flexibility and robustness against RRAM switching variation. The resulting system demonstrates outstanding speed, energy, and area efficiency compared to other TCAM designs utilizing CMOS and emerging non-volatile memory (eNVM). Notably, the proposed 64-bit 1-stage TCAM system achieves speed and energy consumption levels matching the best reported performance of other eNVM-based TCAM designs. Similarly, the proposed design for a 128-bit 2-stage system exhibits speed and energy consumption comparable to SRAM-based TCAMs, with the additional advantages of compact size (90% reduction) and non-volatility.[9]

Feng Wei, et al. introduce an SRAM cell featuring 11 transistors, designed to operate in four distinct modes: SRAM mode, logic mode, and BCAM/TCAM modes. Unlike previous works that primarily focus on column-wise logic/CAM operations, which necessitate column-wise stored operands and are incompatible with traditional row-wise SRAM mode, this novel SRAM cell facilitates operations in both column-wise and row-wise styles across all four modes, eliminating compatibility issues. In the logic mode, the proposed SRAM achieves a frequency of 595MHz and energy consumption of 17.94fJ/bit at 1.2V using TSMC 65nm technology. In BCAM/TCAM modes, it operates at 407MHz with energy consumption rates of 0.62fJ/bit and 1.38fJ/bit at 1.2V, respectively.[10]

Hyunju Kim, et al. Content-Addressable Memory (CAM) executes a parallel search by comparing the search data against all the stored memory contents within a single cycle, bypassing the need for address-based data retrieval. The configuration of the match line (ML) and the search line (SL) significantly impacts power consumption. Various CAM designs aim to achieve low-power and high-speed matching. The paper explores a CAM structure that eliminates the pre-charge phase, resulting in lower power consumption and addressing the drawbacks of traditional AND gate-based CAMs. The proposed CAM architectures are designed using a 65-nm process node with a 1.2 V operating voltage. Results indicate that the new design achieves a 21% increase in speed while reducing leakage power consumption by 23% compared to conventional designs.[11]

S.V.V. Satyanarayana, et al. researched that I n network routers, hardware-based search engines are used to enable parallel data lookup processing, with Content Addressable Memory (CAM) being a crucial component for high-speed lookup searches. However, this high-speed capability comes at the cost of increased energy consumption, particularly due to power dissipation in the Match Lines (MLs). This problem is especially significant in NOR MLs, where short-circuit currents occur during searches. To advance the energy efficiency of CAM architectures, this paper presents a new method featuring a pre-charge-free ML division combined with a dual-bit control technique. The proposed design, a 128 × 32 CAM architecture, is implemented using CMOS 45nm technology with a 1V supply voltage. Extensive verification across various supply voltages, temperatures, and process corners confirms the design's functionality. Simulation results show that the new design achieves a significant reduction in energy consumption, with decreases of 57% and 52% compared to traditional CAM designs.[12]

Gunampalli Manasa Lakshmi, et al. researched that CAM functions as a black box, comparing input search data against a stored data table and returning the address of the matching entry and the current models exhibit significant delay and power consumption, especially with 8*8 array configurations. This research aims to design an 8*8 CAM array using a Transmission Gate (TG) based CAM cell to effectively reduce power consumption. The proposed TG-based CAM array consists of an 8*8 Static Random-Access Memory (SRAM) array, decoder, priority encoder, TG CAM cell, multiplexer, and CAM array as its fundamental components. Designed using the gdpk180 technology in the Cadence Virtuoso tool, the functionality of the anticipated design was evaluated through simulations in the Cadence Spectre tool. The system achieved a delay of 10.17ns and an average power consumption of 856.05 μW. These results were then compared with several existing methods.[13]

V V Satyanarayana Satti, et al. Content-Addressable Memory (CAM) is a hardware-based memory device

used for low power and high-speed applications. CAMs are designed for precise applications without compromising their search speed, making them much quicker than random access memory (RAM) in search operations. CAM performs two key functions: storing and comparing data. The comparison process requires additional circuitry, which increases the size of the CAM and, consequently, the fabrication cost. The dynamic nature of the comparison circuitry during each clock cycle also increases power consumption. To achieve low power designs, new implementations mimic CAM operations using various CAM cell designs within the CAM architecture. Designing novel CAM cells for low power applications in CAM architecture presents a significant challenge for designers. Various CAM cell designs at 180nm, 90nm, and 45nm nodes, were compared evaluating their power and delay, with the analysis conducted using the Cadence Virtuoso tool.[14]

Bohan Zhao, et al. introduce a TCAM update optimization framework designed to ensure consistent forwarding throughout the entire update process by utilizing a layered TCAM structure. Their method employs a modified-entry-first write-back strategy, which significantly reduces the overhead associated with TCAM entry movements. Furthermore, the approach detects reordering cases and addresses them with efficient solutions. Estimated results indicate that this framework can reduce TCAM update costs by 30% to 88% compared to current state-of-the-art techniques.[15]

3. CONCLUSION

This review paper provides an in-depth survey of various Ternary Content-Addressable Memory (TCAM) architectures, highlighting the significant advancements and innovations in this field. TCAMs are crucial for high-speed and low-power applications, particularly in network systems where rapid packet forwarding and classification are essential. The surveyed literature demonstrates a diverse range of approaches to address the inherent challenges in TCAM design, including power consumption, scalability, and fabrication costs.

The reviewed studies underscore the importance of continuous innovation in TCAM technology to address the growing demands for faster, more efficient, and scalable memory solutions in network systems and other high-performance applications. These advancements not only improve the performance and energy efficiency of TCAMs but also open new avenues for integrating novel materials and technologies in future CAM designs. This comprehensive survey serves as a valuable resource for researchers and practitioners seeking to leverage TCAM technology in next-generation network infrastructures and beyond.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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