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Implementation and Analysis of Full Adder using TG-CMOS and DTMOS

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ABSTRACT

Advances in single-chip applications, from high-speed computing to smart health monitoring, demand efficient technologies. Implementing power-hungry algorithms like rapid Fourier transforms and discrete cosine transforms requires essential adder logic for real-time multimedia processing. This study examines the design and simulation of traditional CMOS full-adders and proposed transmission gate buffered full-adder. Using the tanner tool and a 1.5V power supply, the suggested transmission gate buffered full-adder logic circuit is implemented in a 90nm process. When the simulation results of the two logic circuits are compared, it becomes clear that the transmission gate buffered full-adder circuit, which is the primary goal in the implementation of high-speed multimedia processors. In addition to this full adder implementation is compared with DTMOS and Power gate logic to reduce the power usage and the design will not be effected that much leading to the improvement in the performance of the Transmission gate buffered full-adder design. Additional buffers are used in the proposed Transmission gate buffered CMOS full-adder logic circuit to increase the fan-out and driving capability of the digital circuit. Keywords: Adder logic, CMOS logic, chip area, speed-power product, high speed , low power, DTMOS and Power gate logic.

KEYWORDS: Adder logic, CMOS logic, chip area, speed-power product, high speed , low power, DTMOS logic.

1. INTRODUCTION

Since the year 2000, portable electronic devices have become ubiquitous in many aspects of daily life. Because each gadget is now smaller and costs less, these have developed into more figures and have improved their penetration of users.

A few commonly used examples are Bluetooth keyfinders, Wi-Fi hotspot devices, paging devices, smart health monitors, personal digital assistants, core mini-speakers, paging devices, pocketalk language translators, mobile phones, computers, tyre inflators, and many more. In order to extend the battery life of electronic portable devices, lower currents must be used during operation. As a result, ultra-low power consumption and lower propagation delay levels are key design considerations for portable electronics.

The suggested HFA functions without intermediate buffered stages and shows reduced speed-power product values. Bhattacharyya et al. described a one-bit FA (full adder) manufactured in 0.09 mm and 0.180 mm

manufacturing technology using EDA tools. By comparing different parameters with the previous methodologies, it was shown that the strategy suggested in this work produced better results in terms of propagation latency and power usage.

2. FULL-ADDER DESIGN DETAILS

Adder circuits are extensively utilised and located in the critical path of most systems. Therefore, when adding circuit architectures, the crucial specification must be

Low chip area, high processing speed, and low power management are taken into consideration. A CMOS Full adder is a combinational circuit that generates two outputs, a sum and a carry-out data output, by performing binary addition on two bits and a carry-in data input . Table I displays the truth table for the fundamental Full adder logic circuit.

Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Using the truth-table in Table I and minimizing using K-map, the characteristic expressions for sum and carry-out are given as S=A⊕B⊕Cin , Where ⊕means XOR$S=A\oplus B\oplus Cin$, Where ⊕means XOR and Cout=AB+ACin+BCin$Cout=AB+ACin+BCin$But when a Full Adder is created by combining two half-adders, the obtained equation for carry out is

Cout=AB+(A⊕B)Cin

The static CMOS full-adder circuit is the most popular and fundamental adder logic circuit which has robust features with respect to scaling of transistor dimensions, operating voltages, and process parameters Using 28 MOS transistors, the CMOS full adder circuit is shown in Fig. 1

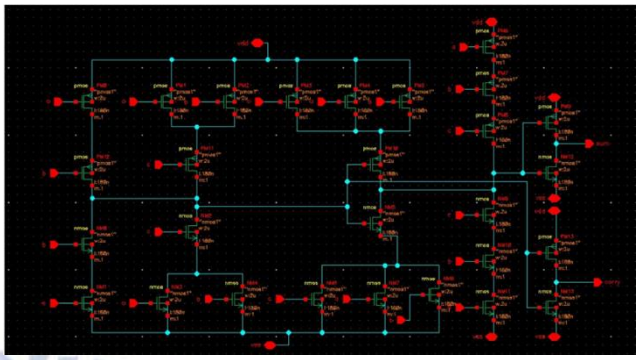

Fig1: - Schematic for a CMOS Full-adder

One of this full-adder circuit's shortcomings is the internconsection of more amount of MOS transistors, increasing the chip's overall size and circuit area. Another issue with this logic circuit is power dissipation. Additional buffer circuits are required to compensate for stability issues.

3. PROPOSED METHODOLOGY

i)A transmission gate full-adder is a sophisticated version of a full-adder circuit shown in fig 2 that enhances signal integrity and performance by adding buffer stages and transmission gates. It addresses signal degradation and drive capability difficulties while providing efficient binary number addition by combining the ideas of a full-adder, gearbox gates, and stages.

A normal full-adder's drawbacks, including limited driving capability, signal distortion, and latency in signal propagation, are intended to be addressed by the gearbox gate full-adder. It guarantees that the signals are correctly transported, amplified, and capable of driving succeeding circuitry without noticeably degrading by integrating transmission gates and stages.

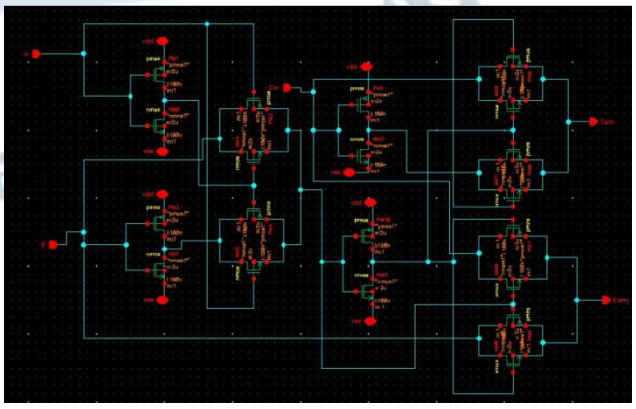

Fig 2: Schematic for Transmission gate full-adder

An improved version of a full-adder circuit that uses buffer stages and transmission gates to enhance signal integrity and performance is called a transmission gate buffered full-adder. It solves signal degradation and driving capability problems by combining the ideas of a full-adder, transmission gates, and buffer stages to create an efficient way to add binary integers. The gearbox gate buffered full-adder is intended to get around some of the drawbacks of a conventional full-adder, including restricted driving capabilities, signal distortion, and delay in signal propagation. It guarantees that the signals are correctly transported, amplified, and capable of driving succeeding circuitry without noticeably degrading by integrating transmission gates and buffer stages.

ii) The logic of the transmission gate DTMOS logic is utilised in the design of a full adder. Now let's talk about DTMOS logic shown in fig 3.Low power techniques" are a collection of tactics and approaches used to reduce power consumption in electronic circuit and system design and operation. These methods are essential for lowering the environmental impact of electronic systems as well as for battery-operated or power-constrained devices.

A method used in CMOS (Complementary Metal-Oxide-Semiconductor) technology to dynamically regulate the threshold voltage of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) is called Dynamic Threshold MOS (DTMOS). One important factor that establishes whether a MOSFET is in the ON or OFF state is the threshold voltage. During operation, DTMOS permits this threshold voltage to be adjusted, offering flexibility in controlling power usage.

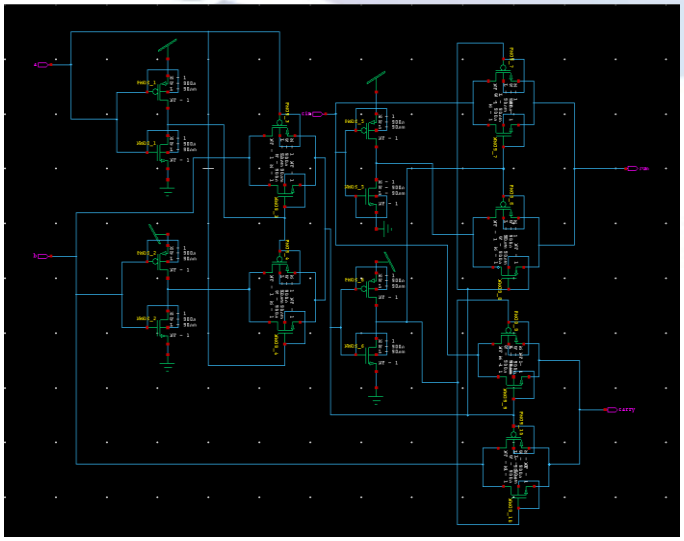

Fig 3: Schematic for Transmission gate full-adder

Applications of DTMOS are common in high-performance computing, where the trade-off between power consumption and speed is critical. Although DTMOS offers advantages in terms of performance and power optimisation, its implementation can add complexity to the design. Designers must carefully balance the benefits of dynamic threshold adjustment with the additional circuitry and potential challenges in manufacturing.

Advantages:

- Reduced Propagation Delay
- Easy design
- Low power consumption

Applications:

- Level Shifting and Voltage Translation
- Data Communication Systems
- System-on-Chip (SoC) Integration
- Data Converters

4. RESULTSANDDISCUSSIONS

The Tanner tool is used to design, develop, and simulate both the suggested Transmission gate full-adder and the DTMOS full-adder circuits in 90nm CMOS technology.

i)The simulation results of the proposed transmission gate full-adder has been designed and the simulated waveforms for both input and output are given in fig 4.

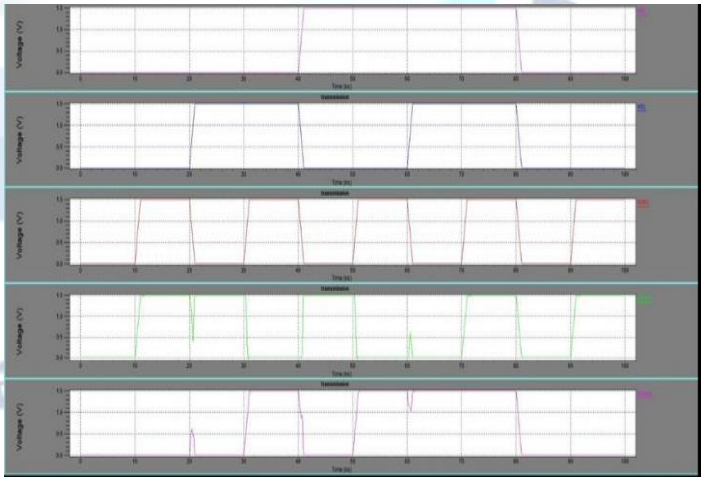

Fig 4: Results of Transmission gate full adder

ii The simulation results of the proposed transmission gate full-adder has been designed and the simulated waveforms for both input and output are given in fig 5.

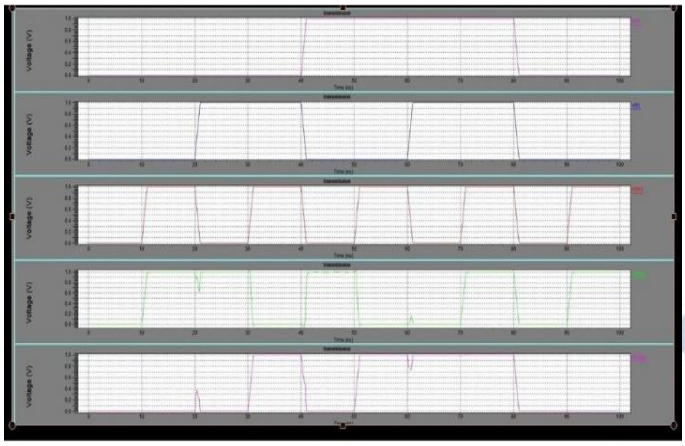

Fig 5: Results of DTMOS full adder

The results are given in terms of Area, Power and delay for both the proposed methods and the comparison table for the existing conventional full adder and the proposed methods is shown in fig 6 below.

Parameters	Traditional CMOS FA	TG-FA	DTMOS FA
Power	47.33	2.655141E-006	1.036681E-006
Area (transistor count)	28	20	20
Delay	1.5*10^.8	3.0838E-011	1.5525E-011

The Power and propagation delay calculations of both fulladder logic circuits are presented in Fig.6 and fig 7. From the results it is revealed that the proposed DTMOS full-adder circuit offers less delay as compared to the Transmission gate full adder logic.

Fig 6 Comparison of power

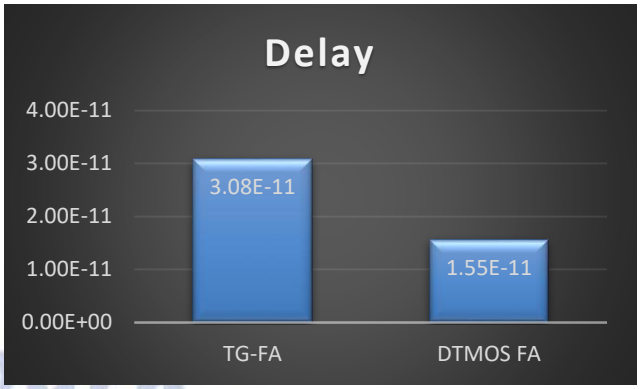

Fig 7 Comparison of Delay

5. CONCLUSIONS AND FUTURE SCOPE

This study designs, simulates, and compares a proposed transmission gate buffered full-adder logic circuit to a standard CMOS full-adder. Tanner EDA tool is used for the entire design and simulation process for 90nm manufacturing technology at a power supply voltage of 1.5V. In contrast to the conventional CMOS full-adder logic circuit, which needs 28 transistors to implement the sum and carry logic operations, the transmission gate buffered full-adder employing DTMOS logic only needs 20 transistors. The recommended circuit requires fewer transistors and nodes. There was less wiring, kinks, and switching faults as a result, which reduced the amount of circuit space. It was discovered that the two full-adder logic circuits had superior transmission efficiencies. Additional circuit design optimisation is needed to achieve gains in speed, power consumption, and space efficiency. investigating the incorporation of the planned complete adder into more substantial circuits or systems, including more intricate processors or arithmetic logic units (ALUs).By comparing and contrasting TG-MOS and DT-MOS with other complete adder implementations currently in use in order to assess the benefits and drawbacks of each. investigating new uses or developments for the TG-MOS and DT-MOS technologies outside of conventional digital logic circuits by advancing current research in the areas of digital circuit design and MOSFET technology, which may result in papers for conferences or scholarly journals.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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