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# Advanced Control of a 63-Level Multilevel Inverter in a Grid-Connected Photovoltaic System

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# ABSTRACT

This project mainly focus on the development of an advanced power conversion system for grid-connected photovoltaic (PV) installations, with a primary focus on a 63-level multilevel H-bridge inverter. The heart of the project lies in the precise control of the 63-level inverter output, achieved through a multi-carrier offset method implemented with a proportional-integral (PI) controller. This control strategy optimizes the synchronization of the inverter output with the grid, minimizing harmonics and enhancing overall system stability and efficiency. The PV panel output is efficiently processed through a fly back converter, and the resulting energy is fed into the high-performance 63-level inverter. This synergy between the control strategies for the fly back converter and the 63-level inverter ensures the seamless and reliable integration of clean energy into the grid. The proposed control methodologies promise enhanced performance, reduced harmonic distortions, and improved power quality, aligning with the global push towards sustainable and efficient renewable energy utilization. This proposed topology is simulated in MATLAB/Simulink and verified experimentally with a hardware prototype under various conditions

#### INTRODUCTION

Nowadays, electric power generation through PV systems has emerged as an alternative to conventional power generating systems due to simple maintenance, eco-friendly nature, low noise and abundant availability. Extracting maximum power and inverting the output power of the PV system into useful AC to feed the utility are the tedious task associated with solar power generation.

To feed the utility grid DC power generated from the PV array has to be inverted into AC power. The

conversion circuit includes a dc-dc power converter and Multi-Level Inverter (MLI). Multilevel inverters (MLIs) are the most popular means for voltage conversion from DC to AC power, and are used in fuel cell and photo-voltaic (PV) based sustainable or renewable energy systems (RES). In this project a Novel PV fed Fly back converter based MLI is introduced for grid utility applications.

The generated power from PV is fed to the load power network through an inverter. For high power applications it is necessary to transform the generated DC into AC. For this conversion, traditional two level inverter is not sufficient due to harmonics and switching losses.

Hence, a novel 63 level based MLI is introduced for domestic applications and elimination of harmonic distortion and its effects.

# LITERATURE SURVEY

#### **OBJECTIVE**

To develop a 63-level multilevel H-bridge inverter capable of efficiently converting the PV panel output to a form suitable for grid integration. To implement a fly back converter to process the PV panel output, ensuring optimal power transfer and compatibility with the 63-level inverter. To utilize a multi-carrier offset method in conjunction with a PI controller to regulate and control the 63-level inverter output. To achieve precise synchronization with the grid, minimize harmonic distortions, and enhance overall system stability.

S.N	TITLE AND	METHODOL	ADVANTA	DRAWBA	
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3	'An Improved	In this paper	The use	> The	
	Artificial Neural	presented an	of an	switching	
	Network-Based	i <mark>mpro</mark> ved	i <mark>mpr</mark> oved	angles	
22.93	Approach for	artificial neural	ANN-based	optimization	
*	Total Harmonic	network (ANN)	approach is	using the	
	Distortion	based approach	advantageous	ANN	
	Reduction in	that can be	for its ability	architecture <b>architecture</b>	
	Cascaded	useful to reduce	to learn and	have	
	H-Bridge	the THD levels	adapt to	limitations or	
	Multilevel	in a cascaded	complex	challenges,	
	Inverters' &Y. Y.	H-bridge (CHB)	patterns.	especially	
	Ghadi , et al	multilevel	> It	under	
	[2023] IEEE	inverter (MLI).	enhancing	varying	
			power quality	operating	
		1. A	by reducing	conditions.	
	-0		Total	Applicable	
			Harmonic	only for	
		1 . · · · ·	Distortion	Specific load	
		4	(THD) in	types.	
	2		energy		
			conversion.		
4	'A New	In this paper	> The	While the	
	Four-Level	introduces a	NFLI is	modified	
	Inverter-fed	new four-level	engineered to	multi-carrier	
	Motor Drive for	inverter (NFLI)	provide	PWM scheme	
	Marine	with a reduced	superior	is introduced	
	Propulsion	component	harmonic	to minimize	
	Systems:	count and	performance.	capacitor	
	Topology,	superior	The proposed	voltage	
	Control, and	harmonic	four-level	ripple, its	
	Analysis' & H.	performance for	inverter	complexity	
	Le, A. Dekka and	MV	(NFLI) is	may pose	

	D. Ronanki	applications.	designed with challenges ir		
	[2023] IEEE		a reduced	terms of	
			component	implementati	
			count	on.	
	'A	In this paper	The use of	> High	
	Switched-Capaci	voltage boost	CFDVM at the	Capacitor	
	tor Multi-Level	switched-capaci	input stage is	Voltage	
	Inverter With	tor multi-level	advantageous	Ripple rises.	
	Variable Voltage	inverter	as it limits the	Limited for	
	Gain Based on	(SCMLI)	capacitor peak	low power	
5.10	Current-Fed	structure is	current and	Applications.	
	Dickson Voltage	planned which	enhances the		
	Multiplier' & Y.	is able to control	voltage gain		
	Niazi , et al	the voltage gain.	compared to		
	[2023] IEEE	The structure is	other SCMLIs.		
		based on	Rea.		
		Current-fed			
	8 10	Dickson Voltage	0		
	1	Multiplier	-		
Μ.,	1.5-1 1	(CFDVM).			
5	A Five-Level	In this paper	> Dual	While using	
	X-Type Boosting	proposes a	Voltage	SCs rated for	
	Inverter With	novel five-level	Boosting	half of the	
0	Reduced Stored	(5L) common	Ability	peak output	
	Energy of	ground type	In the event of	voltage	
V	<mark>Switched</mark> -Capa <mark>ci</mark>	(CGT) inverter	capacitor	reduces the	
100	tors'' & A.	based on	fa <mark>ilure</mark> s, the	energy	
	J <mark>akha</mark> r, et al	switched	p <mark>ropo</mark> sed	storage	
(	[ <mark>2023]</mark> IEEE	capacitors (SCs)	inverter	requirement,	
		with dual	sustain	it trade-offs	
		voltage boosting	operation with	in terms of	
		ability.	reduced	overall	
			voltage levels.	system	
			This	effici <mark>e</mark> ncy.	
2			fault-tolerant	1	
			feature		
			enhances the		
			reliability of		
	and the second sec				
			the system.		





- The multilevel converter is an electronic device that can provide various levels of voltage at the output for more similarity with a pure sine wave.
- In such converters, various lower-level DC voltages are used at the input side. Multilevel converter applications have been mostly used in renewable energy systems.
- This project present a single-phase 17-level cascaded H-bridge multilevel converter (CHMC) model for a stand-alone system using solar PV arrays.
- The proposed model employs eight different flexible PV arrays that can be replaced with DC voltage sources when required to meet the load demand.
- The temperature and irradiance are provided to the solar PV arrays, which produce DC voltages, and these varying DC voltages are stabilized using capacitor banks.
- Then these fixed DC voltages are fed to the CHMC to convert these into AC voltages.
- The seventeen-level CHMC is used to convert the DC voltages into AC to drive the loads.
- This system converter is sinusoidal PWM controlled, which consists of a reference sinusoidal signal and sixteen triangular waves to achieve the desired 17 levels

# DEMERITS OF THE EXISTING SYSTEM

- It attains high harmonics.
- PV output changes periodically as a results it achieves poor efficiency.

It generate damping oscillations and power quality issues in the output of the load.

- High Switching losses.
- THD for this system is quit high compared to proposed work.

# PROPOSED SYSTEM

➤ In this proposed system, PV panel output is directed to a fly back converter, a power electronic device designed to efficiently transform and regulate the incoming energy.

> The fly back converter is controlled by a proportional-integral (PI) controller to optimize the

power transfer and ensure the stability of the conversion process.

> The regulated output from the fly back converter is then fed into a 63-level multilevel H-bridge inverter.

The 63-level inverter's output is precisely controlled using a multi-carrier offset method implemented with a PI controller.

> This control strategy ensures the inverter's output waveform is synchronized with the grid requirements, minimizing harmonic distortions and meeting the necessary grid standards.

> The controlled output from the 63-level inverter is then connected to the single-phase grid through an LC filter.

> The LC filter helps in refining the inverter output, reducing harmonics, and improving power quality before injection into the grid.

This proposed topology is simulated in MATLAB/Simulink and verified experimentally with a hardware prototype under various conditions.



#### PHOTOVOLTAIC SYSTEM

A photovoltaic (PV) system, also known as a solar PV system, is a technology that converts sunlight directly into electricity using solar cells.

It is a type of renewable energy system that harnesses the photovoltaic effect, which is the process by which certain materials can generate an electric current when exposed to sunlight.

PV modules and arrays are just one part of a PV system. The PV system also include mounting structures, along with the components that take the direct-current (DC) electricity produced by modules and convert it to the alternating-current (AC) electricity. The fluctuating nature of Sun, necessitates the use of DC-DC converters for boosting the PV output.



63 MLI CIRCUIT DIAGRAM



# MODES OF OPERATION

The proposed single-phase sixty three-level inverter was developed from the five-level inverter.

It comprises a Single phase conventional H-bridge inverter, three switches, and three voltage sources.

This H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, for inverters of the same number of levels.

Proper switching of the inverter can produce sixty three level output-voltage levels.

The proposed inverter's operation can be divided into sixty three switching states, the required sixty three levels of output voltage were generated.

When H1 and H2 are ON, connecting load terminals to Vdc, and specific switches are closed, the output voltage is set to maximum (Vdc).

By selectively activating different combinations of switches, the inverter produces variable positive output voltages, ranging from 31/31Vdc to 1/31Vdc in incremental steps.

The output voltage at each step is precisely controlled using a multi-carrier offset method implemented with a PI controller. This ensures accurate synchronization with the grid and minimizes harmonic distortions.

#### **MODES OF OPERATION (POSITIVE LEVEL)**

N H HO

				63					447		CONTENTIONIN	OUTPUT VOLTAGE
		55	54	53	52	51	H1 ON	HZ ON	PIS OFF	PH6	DC1(4) D2 D2 D4 H1 (04D H2 51 DC1()	6
	-	0	0	0			014	ON	000	055	002(4) 02 04 05 41 1040 42 51 52 002(4)	12
		0	0	0			04	01	0.00	OFF		
			0				011	ON	000	orr		10
	-	0	0		0	0	ON	ON	UPP.	000	DC3(*)-D+-D5-H1-CDHD-H2-31-DC1(-)-DC1-32-DC2-DC3(-)	24
	>	0	0	1	0	1	ON	ON	UPP	OH	DC3(+)-04-05-H1-L040-H2-51-0C1-02-53-DC3(-)	30
	6	0	0	1	1	0	ON	ON	OFF	OFF	DC3(+)-04-05-H1-L0AD-H2-D1-S2-DC2-S3-DC3(-)	36
	7	0	0	1	1	1	ON	ON	OFF	OFF	DC3(+)-04-05-H1-L0AD-H2-31-0C1-32-DC2-33-DC3(-)	42
	8	0	1	0	0	0	ON	ON	OFF	OFF	DC4(+)-D4-D5-H1-LO4D-H2-D1-D2-D3-DC4(-)	48
	9	0	1	0	0	1	ON	ON	OFF	OFF	DC4(+)-D5-H1-LOAD-H2-S1-DC1-D2-D3-DC4(-)	54
	10	0	1	0	1	0	ON	ON	OFF	OFF	DC4(+)-D5-H1-LOAD-H2-D1-52-DC2-D3-DC4(-)	60
	11	0	1	0	1	1	ON	ON	OFF	OFF	DC4(+)-D5-H1-LOAD-H2-S1-DC1-S2-DC2-D3-DC4(-)	66
	12	0	1	1	0	0	ON	ON	OFF	OFF	DC4(+)-D5-H1-LA0D-H2-D1-D2-S3-DC3-DC4(-)	72
	13	0	1	1	0	1	ON.	ON	OFF	OFF	DC4(+)-D5-H1-LO4D-H2-51-DC1-D2-53-DC3-54-DC4(-)	78
-	14	0	1	1	1	0	ON	ON	OFF	OFF	DC4(+LD5,H1J,D4D,H2,D1,52,DC2,53,DC3,54,DC4(-)	84
2	16	0	1	1	1	1	ON	ON	005	220	D04(4).05.41.1040.42.51.001.52.002.53.002.54.004(3)	90
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2	- 7	-					011	011	000	ore		20
2			0	0			UN	UN	OFF	OFF	003(*)+12-0040+12-01-02-03-04-005)-)	102
	18	1	0	0	1	0	UN	UN	UPP	UPP	DC5(+)+1-C04D+1-01-52-0C2-03-D4-0C5(-)	208
	19	- 1	0	0	1	1	ON	ON	OFF	OFF	DC5(+)H1-L0AD-H2-S1-DC1-S2-DC2-D3-D4-DC5(-)	114
	20	1	0	0	0	0	ON	ON	OFF	OFF	DCS(+)-H1-L0AD-H2-S1-DC1-D2-S3-DC3-D4-DC5(-)	120
	21	1	0	0	0	1	ON	ON	OFF	OFF	DC5(+)-H1-L0AD-H2-D1-52-DC2-S3-DC3-D4-DC5(-)	126
	22	1	0	0	1	0	ON	ON	OFF	OFF	DCS(+)-H1-LOAD-H2-D1-S2-DC2-S3-DC3-D4-DCS(-)	132
	23	1	0	0	1	1	ON	ON	OFF	OFF	DC5(+)-H1-LOAD-H2-51-DC1-52-DC2-53-DC3-D4-DC5(-)	138
	24	1	1	1	0	0	ON	ON	OFF	OFF	DC5(+)-H1-LOAD-H2-D1-D2-D3-S4-DC4-DC5(-)	144
	25	1	1	1	0	1	ON	ON	OFF	OFF.	DC5(+)-H1-LOAD-H2-S1-DC1-D2-D3-S4-DC3-DC5(-)	150
	26	1	1	1	1	0	ON	ON	OFF	OFF	DC5(+)-H1-L0AD-H2-D1-52-DC2-D3-54-DC4-DC5(-)	156
	27	1	1	1	1	1	ON	ON	OFF	OFF	DC5(+)-H1-LOAD-H2-S1-DC1-S2-DC2-D3-S4-DC4-DC5(-)	162
	28	1	1	1	0	0	ON	ON	OFF	OFF	DCSI+LH14.0AD-H2-D1-D2-S3-DC3-S4-DC4-DC5I-1	168
	29	1	1	1	0	1	ON	ON	OFF	OFF	DC5(+).+1.(040.+2.41.0C1.02.43.0C3.54.0C4.0C5).	174
	20	-		1	1	0	ON	ON	000	015	005(4) 41 J 040 42 01 83 003 83 003 84 004 005(1)	190
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#### 63 Level PWM Generation

In this project multi carrier pulse width modulation technique is used to generate the sixty three level output voltage.

Seven equal amplitude carrier triangular signals with offset is compared with the sinusoidal reference signal.

These PWM signals are given to the switches S1, S2, S3, S4, S5. Then the two sinusoidal signals having 180 degree displacement signals are compared with the carrier triangular signal, these PWM pulses are having dead band, it will avoid the shoot through problem between two devices.

These PWM pulses are given to the single phase inverter circuit switches H1, H2, H3 and H4.

This pulse having 5KhZ switching frequency to control the additional switches. These PWM pulses are the main reason to control the output voltage of the inverter.



# 63 Level DC Output Voltage Waveform



# Hardware Description

- Dspic30f4011 controller
- Works in 5 v supply.
- Micro controller belongs to transister-transister logic (ttl) family.
- Programmed using embedded c language.
- It generates pwm pulse for the switches used in converter and inverter.
- Driver circuit- tlp250
- Driver circuit has opto coupler.
- It enhances the 5v pulse to 15v pulse.
- It also provides isolation, for the protection of micro controller.

# DSPIC30F4011 CONTROLLER BOARD

DSPIC30F4011 microcontroller includes a large 48kB internal flash memory and a wide range of timers together with a number of PWM modules.



# FEATURES

- High Performance Modified RISC CPU
- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 84 base instructions with flexible addressing modes
- 24-bit wide instructions, 16-bit wide data path
- > 16 x 16-bit working register array
- DC to 40 MHz external clock input
- 4 MHz 10 MHz oscillator input with PLL active (4x, 8x, 16x)
- Peripheral and External interrupt sources
- > 8 user selectable priority levels for each interrupt
- ➤ 4 processor exceptions and software traps
- Primary and Alternate interrupt Vector Tables

# TLP250 DRIVER CIRCUIT

TLP250 is an isolated IGBT/Mosfet driver IC.

The input side consists of a GaAlAs light-emitting diode.

The output side gets a drive signal through an integrated photo detector.

Therefore, the main feature is electrical isolation between low and high power circuits It transfers electrical signals optically via light.

TLP250 has photo diode and photo transistor.

When 5v pulse is given to photo diode, it send signal to the gate of photo transistor, allowing it to send 15v

pulse.

Photo diode is current controlled device so there is a current limiting resistor is placed in the front.

Zener diode is used as voltage regulator for 15v. Then there is snubber protection for the circuit.



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# POWER SUPPLY

It has bridge rectifier and smoothing capacitor.

A bridge rectifier can be made using four individual diodes, but it is also available in special packages containing the four diodes required. It is called a full-wave rectifier.

Smoothing is performed by a large value electrolytic capacitor connected across the DC Supply to act as a reservoir, supplying current to the output when the varying DC Voltage from the rectifier is falling.

# FILTER CAPACITOR- 25V, 1000µF

A filter capacitor, also referred to as a smoothing capacitor or a decoupling capacitor, is an electronic component utilized in electronic circuits to mitigate voltage fluctuations.

Its primary function is to eliminate unwanted AC components from a DC power supply, resulting in a more stable DC voltage output.



#### INDUCTOR

An inductor is a passive component that is used in most power electronic circuits to store energy in the form of magnetic energy when electricity is applied to it. One of the key properties of an inductor is that it impedes or opposes any change in the amount of current flowing through it.

We use transformer type inductor, here primary winding and secondary windings are connected in series. This type of inductor provides galvanic isolation.



# **CRYSTAL OSCILLATOR**

With an operating frequency ranging from 10Hz to 16MHz, a crystal oscillator is an electronic circuit that leverages the mechanical resonance of a piezoelectric crystal to produce a stable frequency signal.

Upon application of an electric field to the crystal, it oscillates at an extremely accurate frequency, which can be utilized as a stable clock signal for digital electronics.



#### **CERAMIC CAPACITOR**

To stabilize the oscillation and establish a ground reference for the crystal, a ceramic capacitor is commonly used in a crystal oscillator circuit.

The capacitor is situated between the ground and the two crystal terminals

OVER ALL SIMULATION

10









# CURRENT THD WAVEFORM



# **ADVANTAGES**

Power low is less due to the usage of less components.

> It has no clamping devices.

> This 63 level inverter improves the efficiency and reduces the losses.

- Total harmonic distortion is low.
- Efficient load synchronization.
- Less switching losses.

# APPLICATION

- Industrial applications variable ac motor, induction heating, standby power systems.
- Solar pumping applications.
- Used in high speed AC motors.
- > Used in grid connected systems.
- On grid stations.
- Very less THD.
- > Reduced number of switches and DC sources.
- > Efficient load and grid synchronization.
- ➤ Less switching losses.
- Harmonics distortion are less.
- > Lesser the number of power switches.
- > Capacitor unbalancing problem will not come.

#### CONCLUSION

In conclusion, this project successfully demonstrates the feasibility and effectiveness of integrating a 63-level multilevel inverter into a grid-connected photovoltaic (PV) system.

The key components of the project, including the fly back converter and the 63-level inverter, are controlled by proportional-integral (PI) controllers, showcasing a enhanced system performance.

The implementation of a multi-carrier offset method with the PI controller for the 63-level inverter proves to be instrumental in achieving precise control over the output waveform.

This strategy ensures synchronization with the grid, minimizing harmonic distortions and meeting the stringent standards set for grid-connected renewable energy systems.

The findings of this project contribute valuable insights to the field of power electronics and renewable energy systems, promoting sustainable practices in grid-connected applications.

In MATLAB 2021a this topology is simulated and then empirically tested with a hardware prototype under various circumstances.

#### FUTURE SCOPE

**Enhanced Control Algorithms:** Further development in control strategies and modulation techniques for improved efficiency, reduced losses, and better harmonic suppression.

**High Power Charging**: Integration into high-power charging infrastructure for electric vehicles, facilitating faster charging and reducing grid stress during peak demand.

**Battery Energy Storage:** Utilizing 63-level inverters in battery energy storage systems for efficient power conversion and grid integration, optimizing the use of stored energy.

**Cyber security Measures:** Implement robust cyber security measures to secure the communication and control interfaces of the grid-connected PV system.

As these systems become more interconnected, ensuring cyber security is crucial for protecting against potential cyber threats.

#### Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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