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# Implementation and Performance Analysis of 4:1 Multiplexer using 90 nm Technology

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## ABSTRACT

***Multiplexer (MUX) which is also familiar as an input or information selector and a device that opts joining different analog or digital signal inputs and ahead the marked put in to sole yield. It is first of the salient components which upgrade the effectiveness of data transversal. Multiplexers are used to expand the amount of the data that can be transferred over a line of network with given bandwidth over a time of period. There are different multiplexers for digital and analog signals. A digital multiplexer has digital input signals coming from different data-acquisition networks. In this project, a 4:1 multiplexer is analyzed by numerous logics like CMOS logic, Transmission gate logic and PTL logic which recognize the foremost families that is appropriate for the outline of greatest methods of multiplexer. The execution is implemented in VLSI automation because it has characteristics such as less size, less cost, great operating speed and less power. The accomplishment research of the multiplexer using different logic families are executed in cadence virtuoso at 90nm. The results gathered shows that the Transmission gate logic method based 4:1 multiplexer is the well-organized method. The Transmission gate logic performs better than other logics, and it is strongly advised that the approach of Transmission gate logic be used to create a massive elevated various level multiplexer with shallow power and power delay product.***

***Keywords: MUX, CMOS, PTL, Transmission gate logic***

## 1. INTRODUCTION

VLSI engineers have been developing different devices that operate faster, use less power, and take up less space in a regular manner over the past 10 years. due to the fact that low-power portable devices are crucial to customers in the modern world. Building a gadget that satisfies every customer's requirement while taking all of these considerations into account presents a challenge for designers. Conventional design techniques are not enough to build an effective system. Therefore, a variety of cutting-edge design strategies are needed to give users a better experience.

A multiplexer, sometimes called a MUX and occasionally spelled multiplexer, is a combinational circuit that chooses one data input from a range and sends it to the output. A multiplexer may accept either

digital or analog inputs. Data selectors are another name for multiplexers. When sending a lot of data via a network in a limited amount of time and bandwidth, a multiplexer comes in handy. In analog applications, multiplexers constructed from transistors and relays are referred to as analog multiplexers; in digital applications, multiplexers constructed using logic gates are referred to as digital multiplexers. A demultiplexer is the opposite of a multiplexer. In digital systems, it is frequently required to choose one data line from a number of data-input lines, and the output line should contain the data from the chosen data input line. A multiplexer is the digital circuit that performs this function.

**2. LITERATURE SURVEY:**

A multiplexer (or mux; often spelt multiplexer) is a device in electronics that selects amongst many analogue or digital input signals and transmits the selected input to a single output line. A separate set of digital inputs known as select lines controls the selection. A two-channel multiplexer 2^n inputs have n select lines, which are used to determine which input line should be sent to the output. Two inputs D0 and D1, one selects input S, and one output Y make up a 2-to-1 multiplexer. The output is connected to either of the inputs depending on the select signal. Because there are two input signals, there are only two ways to connect the inputs to the outputs, so one chooses is required to perform these actions. A 4 to 1 MUX has "FOUR" input lines, D0, D1, D2, and D3, two selection lines, S0 and S1, and one output Y- line. Lines S0 and S1 choose one of the four input lines to link to the outgoing line. The diagram below depicts a 4 to 1 MUX block diagram in which the multiplexer selects the input via the selected line.

The 90 nm technology node represents a considerable improvement in semiconductor manufacturing, but it also offers new problems, such as higher leakage currents and lower noise margins. Using diverse logic families to implement multiplexers allows researchers and designers to investigate solutions to these difficulties while optimising performance and power consumption.

**3. EXISTING METHOD:**

A PMOS pull-up logic network and a NMOS pull-down logic network are used in conventional or complementary CMOS logic gates. The CMOS logic style benefits from robustness gains in voltage scaling and transistor sizing. It operates reliably at low voltages and has high noise margins. Only connect input signals to transistor gates. It makes it easier to use and characterise logic cells. The complementary transistor pair facilitates and simplifies the layout of CMOS gates. The main disadvantage of CMOS is the high input load caused by the large number of large PMOS transistors AND gates are used to generate the Partial Products, PP, If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product. The way that the partial products are generated or summed up is the difference between the different architectures of various multipliers.

By allowing the primary inputs to drive gate terminals as well as source drain terminals, pass-transistor logic reduces the number of transistors required to implement logic. The benefit is that only one pass-transistor network (NMOS or PMOS) is required to perform the logic operation. Several pass-transistor logic styles, including NMOS Pass Transistor Logic, CMOS Transmission Gate, and pass transistor logic (PTL), are being considered for use in the implementation of a four-to-one multiplier. Among these, the NMOS Multiplexer is the best. It employs two NMOS transistors, with two-pass transistors at the input determining which signal to propagate. The pass transistor will degrade the logic levels. For accurate operation, the threshold voltages of both pass-transistors should be identical Multiplication of binary numbers can be decomposed into additions. Consider the multiplication of two 8-bit numbers A and B to generate the 16 bit product P.

**4. PROPOSED DESIGN:**

A transmission gate is made up of two complementary metal-oxide-semiconductor (CMOS) transistors, one NMOS (n-type metal-oxide- semiconductor) and one PMOS (p-type metal-oxide-semiconductor). The output of the NMOS transistor is connected to the low logic level (usually ground or 0), whereas the output of the PMOS transistor is connected to the high logic level (usually the power supply voltage, denoted as VDD or 1). The NMOS transistor is turned on when the control signal is high, allowing the low logic level to pass through. Simultaneously, the PMOS transistor is turned

off, preventing the output from being affected by the high logic level. When the control signal is low, the NMOS transistor is turned off, allowing the high logic level to pass through. Transmission gate logic is frequently used in high-speed, low-power applications such as adders and multipliers. It can also be used to design analogue circuits.

The term "Complementary Metal-Oxide-Semiconductor (CMOS)‖ refers to a kind of MOSFET production technique that employs symmetrical and complementary pairings of p- type and n-type MOSFETs for logic tasks like Integrated circuit (IC) chips, such as microprocessors, microcontrollers, memory chips (including CMOS BIOS), and other digital logic circuits, are made using CMOS technology. Analog circuits such as data converters, RF circuits (RF CMOS), image sensors (CMOS sensors), and highly integrated transceivers for various forms of communication are also made using CMOS technology.

Pass transistor logic, or PTL, is a term used in electronics to describe a number of logic families used in integrated circuit design. By getting rid of unnecessary transistors, it lowers the number of transistors needed to create various logic gates. It might be necessary to build a conventional gate in order to restore the signal voltage to its full value when multiple devices are connected in series within a logic path. In contrast, logic voltage levels in a sequential chain do not drop because conventional CMOS logic switches transistors so the output connects to one of the power supply rails (similar to an open collector scheme). It might be necessary to simulate circuits in order to guarantee proper performance.

The gate of the n-channel MOSFET is at a negative supply voltage potential when the control input is a logic zero, or negative power supply potential. The inverter is responsible for driving the p-channel MOSFET's gate terminal towards the positive supply voltage potential. When a voltage is provided within the allowable range to either of the transmission gate's switching terminals (in or out), the gate-source voltage of the n-channel MOSFETs is always negative, while the p-channel MOSFETs is always positive. As a result, the transmission gate closes and neither of the two transistors will conduct.

The voltage drop issue with the pass transistor logic is resolved by using the transmission gate logic. The complimentary characteristics of PMOS and NMOS transistors are used in this method. For example, PMOS transistors pass a strong "1" but a weak "0," and NMOS devices pass a strong "0" but a weak "1." An NMOS transistor and a PMOS transistor are connected in parallel to create the transmission gate, which combines the finest features of both devices.

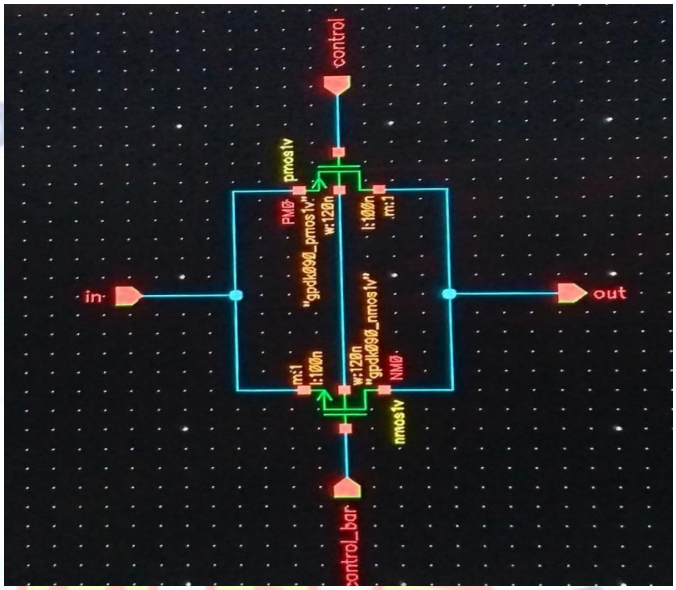


Fig: TGL LOGIC

When the transmission gate's switching terminal is elevated to a value that is close to the negative supply voltage, the N-channel MOSFET experiences a positive gate-source voltage, also known as the gate-to-drain voltage. This causes the transistor to start conducting, which in turn causes the transmission gate to conduct. As a result of the constant raising of the voltage at one of the transmission gate's switching terminals to the positive supply voltage potential, the n-channel MOSFET's gate-source and gate-drain voltages decrease and the MOSFET starts to shut off. The transmission gate switches and the p-channel MOSFET begins to conduct when a negative gate-source voltage (also known as a gate-to-drain voltage) builds up in the transistor.

## 5. SIMULATION RESULTS:

| S.No | Logic | Circuit mode | TransistorCount | Power | Delay |
|---|---|---|---|---|---|
| 1 | CMOS | 2:1 MUX | 10 | 141.4E-9 | 20.65E-12 |
| 2 | PTL | 2:1 MUX | 2 | 21.27E-6 | 20.58E-15 |
| 3 | TGL | 2:1 MUX | 4 | 4.933E-6 | 30.23E-15 |

Table: Power and Delay Analysis of 2:1 Multiplexer

| S.No | Logic | Circuit mode | Transisto Count | Power | Delay |
|---|---|---|---|---|---|
| 1 | CMOS | 4:1 MU | 26 | 311.4E-9 | **2.09E-12** |
| 2 | PTL | 4:1 MU | 6 | 36.22E-6 | **4.32E-15** |
| 3 | TGL | 4:1 MU | 12 | 34.52E-6 | **8.70E-15** |

Table: Power and Delay Analysis of 4:1 Multiplexer

## 6. CONCLUSION:

The analysis of a 4:1 multiplexer using various CMOS logics, including Transmission Gate Logic and PTL Logic, provides valuable insights into the optimal design choices for VLSI implementation. The project aimed to identify the most suitable logic family based on factors such as size, cost, operating speed, and power consumption. The utilization of a 4:1 multiplexer underscores the importance of efficient signal selection and routing in digital circuits. Different CMOS logics, each with its unique characteristics, were evaluated to determine their impact on the overall performance of the multiplexer. Transmission Gate Logic, known for its simplicity, and PTL Logic, recognized for its low area consumption, were specifically chosen for analysis. The comparative study likely involved assessing trade- offs between these logics in terms of design complexity, speed, and power efficiency. The decision to implement the project in VLSI automation reflects the advantages offered by this technology, including reduced size, lower cost, enhanced operating speed, and efficient power management. VLSI allows for the integration of a large number of transistors on a single chip, making it a suitable platform for implementing complex digital circuits like multiplexers Ultimately, the conclusion of this project would likely highlight the optimal logic family or combination of logics for the 4:1 multiplexer design, taking into consideration the specific requirements of the application and the desired balance between size, cost, speed, and power efficiency. The findings contribute to the broader understanding of efficient digital circuit design in VLSI applications

### Conflict of interest statement

Authors declare that they do not have any conflict of interest.

## REFERENCES


[1] Neil H. E.Weste and David Money Harris, —Implementation and performance Analysis of 2:1 Multiplexer using Different Logic Families at 130nm Technology‖, 3rd International Conference on Advances in Computing , Communication Control and Networking(ICAC3N).2021.

[2] Neil H. E.Weste and David Money Harris, —CMOS VLSI Design A Circuits and System Perspective‖, Pearson Education (Asia) Pvt.Ltd.2000.

[3] J. M. Rabaey, A. Chandrakasan, and B. Nicolic, —Digital Integrated Circuits: A Design Perspective‖, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.

[4] M. Padmaja, V.N.V. Satya Prakash, —Design of multiplexer in multiple logic styles for low power VLSI‖, International Journal of Computer Trends and Technology – volume 3 Issue 3 – 2012.

[5] Gurjeet Kaur, Gurmohan Singh, —Analysis of low power CMOS current comparison domino logic circuits in ultra-deep submicron technologies,‖ International Journal of Computer Applications (0975 – 8887), February 2014, Volume 88 – No.7.

[6] Purnima Kumari Sharma, Neeraj Kumar Singh, —Power comparison of single and dual rail 2:1 MUX design at different levels of technology,‖ IEEE Conference, 2014, pp. 671-775.

[7] S. Abirami, M. Arul Kumar, E. Abinaya and J. Sowmaya, "Design and analysis of 2:1 multiplexer circuit for high performance", International Journal of Electrical and Electronics Engineers, vol. 7, no. 01, Jan-June 2015.

[8] B. Madhav, G.S. Dheeraj and S.S. Raghavarapu, "Multiple band mobile antenna for LTE GSM PCS UMTS & IoT applications", International Journal of Engineering and Technology(UAE), vol. 7, no. 27, pp. 609-612, 2018.

[9] B.T.P. Madhav, G. Sai Dheeraj and S.S. Raghavarapu, "Design of a CPW-fed monopole antenna for ultrawide band based iot and medical applications", International Journal of Pharmaceutical Research, vol. 10, no. 4, pp. 74-79, 2018.

[10] N. Siddaiah, B. Manjusree, A.L.G.N. Aditya and D.V.R.K Reddy, "Design simulation and analysis of u-shaped and rectangular mems based triple coupled cantilevers", Journal of Scientific and Industrial Research, vol. 76, no. 4, pp. 235-238, 2017.