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Adopting an Enhanced Reconfigurable Built-in Self-Repair Plan in SOCs

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ABSTRACT

As RAM is major component in present day SOC, by¬Improving the yield of RAM improves the yield of SOC. So the repairable memories play a vital role in improving the yield of chip. Built-in self-repair (BISR) technique has been widely used to repair embedded random access memories (RAMs). This paper presents a reconfigurable BISR (Re BISR) scheme for repairing RAMs with dif¬ferent sizes and redundancy organizations. An efficient redundancy analysis algorithm is proposed to allocate redundancies of defective RAMs. In the Re BISR, a re¬configurable built-in redundancy analysis (Re- BIRA) circuit is designed to perform the redundancy algorithm for various RAMs. Also, an adaptively reconfigurable fusing methodology is proposed to reduce the repair setup time when the RAMs are operated in normal mode. The experimental results show that proposed Re BISR circuit reduces the area and increases the yield of the memory.

1. INTRODUCTION

BUILT-IN SELF-TEST (BIST) techniques can effectively reduce the difficulty and complexity of VLSI testing, by introducing on-chip test hardware into the circuit-under-test (CUT). In conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers.

A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to Significantlyhigh switching activities in the CUT [1], which can cause excessive power dissipation. They can also damage the circuit and reduce product yield and lifetime [2], [3]. In addition, the LFSR usually needs to generate very long pseudorandom sequences in order to achieve the target fault coverage in nanometer technology.

2. LITERATURE REVIEW

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard

etal.analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4].applied. The first class is the LFSR tuning. Girard et al. analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4].

The second class is low-power TPGs. One approach isto design low-transition TPGs. Wang and Gupta used twoLFSRs of different speeds to control those inputs that haveelevated transition densities [5]. Corno et al. provided a lowpowerTPG based on the cellular automata to reduce the testpower in combinational circuits [6]. Another approach focuseson modifying LFSRs. The scheme in [7] reduces the powerin the CUT in general and clock tree in particular. In [8],a low-power BIST for data path architecture is proposed,which is circuit dependent.

However, this dependency impliesthatnondetecting subsequences must be determined for eachcircuit test sequence. Bonhomme et al. [9] used a clock gatingtechnique where two nonoverlapping clocks control the oddand even scan cells of the scan chain so that the shift powerdissipation is reduced by a factor of two. The ring generator[10] can generate a single-input change (SIC) sequence whichcan effectively reduce test power. The third approach aimsto reduce the dynamic power dissipation during scan shiftthrough gating of the outputs of a portion of the scan cells.Bhunia et al. [11] inserted blocking logic into the stimuluspath of the scan flip-flops to prevent the propagation of thescan ripple effect to logic gates. The need for transistorsinsertion, however, makes it difficult to use with standardcell libraries that do not have power-gated cells. In [12], theefficient selection of the most suitable subset of scan cells forgating along with their gating values is studied.

The third class makes use of the prevention of pseudorandompatterns that do not have new fault detecting abilities[13]–[15]. These architectures apply the minimum number oftest vectors required to attain the target fault coverage andtherefore reduce the power. However, these methods havehigh area overhead, need to be customized for the CUT, andstart with a specific seed.Gerstendorfer et al. also proposedto filter out nondetecting patterns using gate-based blockinglogics [16], which, however, add significant delay in the signalpropagation path from the scan flip-flop to logic.Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scanenable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR [20], a low-transition random TPG [21], and the weighted LFSR [22]. The TPG in [20] can reduce the transitions in the scan inputs by assigning the same-value to most neighboring bits in the scan chain. In [21], power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in [22] decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various probabilities.

3. CONTRIBUTION AND PAPER ORGANIZATION:

This paper presents the theory and application of a class of minimum transition sequences. The proposed method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence can be summarized as follows.

1) Minimum transitions: In the proposed pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power.

2) Uniqueness of patterns: The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequencecan meet the requirement of the target fault coverage for the CUT. 3) Uniform distribution of patterns: The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time [23]. It is proved in this paper that our multiple SIC (MSIC) sequence is nearly uniformly distributed.

4) Low hardware overhead consumed by extra TPGs: The linear relations are selected with consecutive vectors

or within a pattern, which has the benefit of generating a sequence with a sequential decompressor. Hence, the proposed TPG can be easily implemented by hardware.

The rest of this paper is organized as follows. In Section II, the proposed MSIC-TPG scheme is presented. The principle of the new MSIC sequences is described in Section III. In Section IV, the properties of the MSIC sequences are analyzed. In Section V, experimental methods and results on test power, fault coverage, and area overhead are provided to demonstrate the performance of the propsoed MSIC-TPGs. Conclusions are given in Section VI.

4. MSIC-TPG SCHEME:

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple codewords. Meanwhile, the generated codewords will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

A.Test Pattern Generation Method:

Assume there are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has l scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as S(t) = S0(t)S1(t)S2(t), . . . , Sm−1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . . , Jl−1(t).

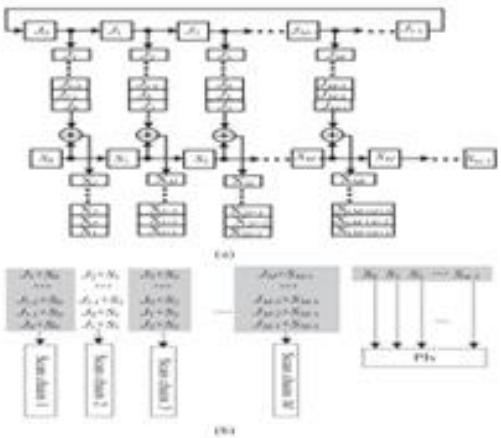

Fig. 1. (a) Symbolic simulation of an MSIC pattern for scan chains. (b) Symbolic representation of an MSIC pattern.

In the first clock cycle, J = J0 J1 J2,..., Jl−1 will bit-XOR with S = S0 S1 S2,..., SM−1, and the results X1Xl+1X2l+1,..., X(M−1)l+1 will be shifted into M scan chains, respectively. In the second clock cycle, J = J0 J1 J2,..., Jl−1 will be circularly shifted as J = Jl−1 J0 J1,..., Jl−2, which will also bit-XOR with the seed S = S0 S1 S2,..., SM−1. The resulting X2Xl+2X2l+2,..., X(M−1)l+2 will be shifted into M scan chains, respectively. After l clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed S0 S1 S2,..., Sm−1 will be applied to m PIs. Since the circular Johnson counter can generate l unique Johnson codewords through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential decompressor.

B. Reconfigurable Johnson Counter:

According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson codewords, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

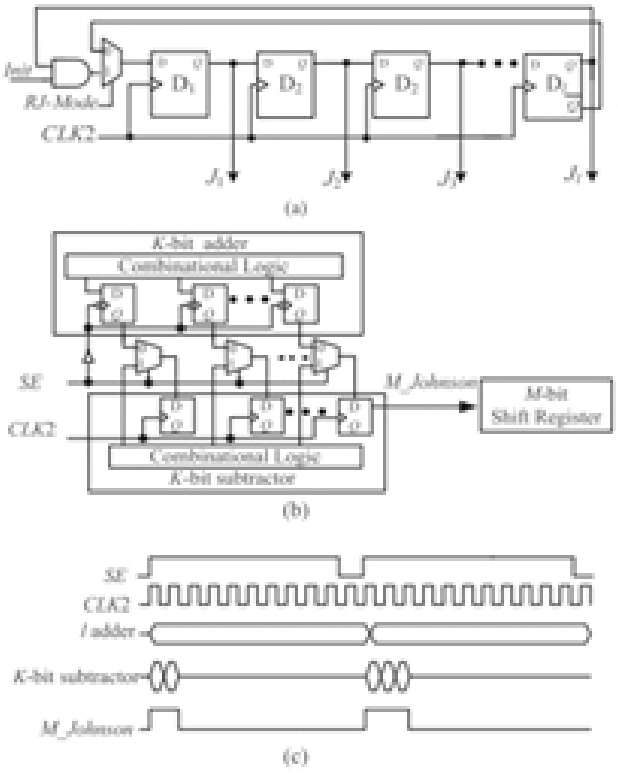

Fig. 2. SIC generators. (a) Reconfigurable Johnson counter. (b) Scalable SIC counter. (c) Waveforms of the scalable SIC counter.

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time

domain. As shown in Fig. 2(a), it can operate in three modes.

1) Initialization: When RJ_Mode is set to 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.

2) Circular shift register mode: When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.

3) Normal mode: When RJ_Mode is set to logic 0, the re-configurable Johnson counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

C. Scalable SIC Counter:

When the maximal scan chain length l is much larger than the scan chain number M, we develop an SIC counter named the "scalable SIC counter." As shown in Fig. 2(b), it contains a k-bit adder clocked by the rising SE signal, a k-bit subtractor clocked by test clock CLK2, an M-bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of log2(l − M). The waveforms of the scalable SIC counter are shown in Fig. 2(c). The k-bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 2(b), it can operate in three modes.

1) If SE = 0, the count from the adder is stored to the k-bit subtractor. During SE = 1, the contents of the k-bit subtractor will be decreased from the stored count to all zeros gradually.

2) If SE = 1 and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0).

3) Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson codewords will be applied into different scan chains.

For example, after full-scan design, ISCAS'89 s13207 has 10 scan chains whose maximum scan length is 64. To implement a scalable SIC counter as shown in Fig. 2(b), it only needs 6 D-type flip-flops (DFFs) for the adder, 6 DFFs for the subtractor, 10 DFFs for a 10-bit shift register for 10 scan chains, 6 multiplexers, and additional 19 combinational logic gates. The equivalent gates are 204 in total.

For a 64-bit Johnson counter, it needs 64 DFFs, which are about 428 equivalent gates. Generally, the gate over-head of a MSIC-TPG can be estimated by the number of DFFs (NDFF) used NDFF = m + M + 2log2l = (m + M) 1 + 2log2l m + M (1)where m, M, and l are the seed number, scan chain number, and the maximum scan length, respectively. If l is doubled, the number of DFFs is only increased by 2/(m + M) times. If 2i−1 < l < 2i (i is a natural number), the number of DFFs does not vary with the CUTs' sizes. For example, as will be shown in Table II, for ISCAS'89 benchmarks, when the seed num-ber increases from 20 to 38 and the maximum scan length increases from 54 to 87, their area overheads change only from 397.40 to 488.29 μm2.

D. MSIC-TPGs for Test-per-Clock Schemes:

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 3(a). The CUT's PIs X1 − Xmn are arranged as an n × m SRAM-like grid structure. Each grid has a two-in-put XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed genera-tor is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure is as follows. 1) The seed generator generates a new seed by clocking CLK1 one time. 2) The Johnson counter generates a new vector by clock-ing CLK2 one time. 3) Repeat 2 until 2l Johnson vectors are generated. 4) Re-peat 1–3 until the expected fault coverage or test length is achieved.

E. MSIC-TPGs for Test-per-Scan Schemes: The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 3(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator isnot smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to M scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows

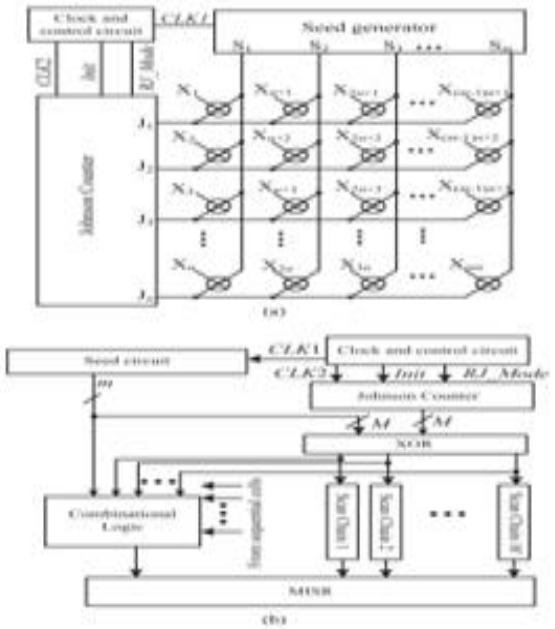

Fig. 3.MSIC-TPGs for (a) test-per-clock and (b) test-perscan schemes.

1) The seed circuit generates a new seed by clocking CLK1 one time. 2) RJ_Mode is set to "0". The reconfigu-rable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time. 3) After a new Johnson vector is generated, RJ_ Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates l codewords by clocking CLK2 l times. Then, a capture operation is inserted. 4) Repeat 2–3 until 2l Johnson vec-tors are generated. 5) Repeat 1–4 until the expected fault coverage or test length is achieved.

BISR ARCHITECTURE:

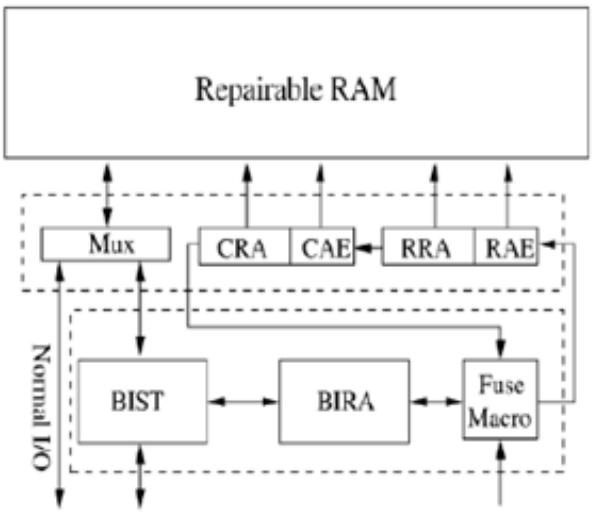

Fig. 4.Typical BISR scheme forembeddedRAMs.

Fig. 4 shows the block diagram of a typical BISR scheme for a RAM, which consists of four major components. 1) Repairable RAM: A RAM with redundancies andRecon-figurationcircuit. Fig. 5 depicts an example of an 8*8 bit-oriented RAM with 1 spare row and 1 spare column. If a spare row is allocated to replace a defective row, then the row address of the defective row is called row repair address (RRA).

Then a decoder decodes the RRA into control signals for switching row multiplexers to skip the defective row if the row address enable (RAE) signal is asserted. The re-configuration of the defective column and the spare col-umn is performed in a similar way, i.e., give a column repair addresses (CRA) and assert the column address enable signal to repair the defective column using the spare column.

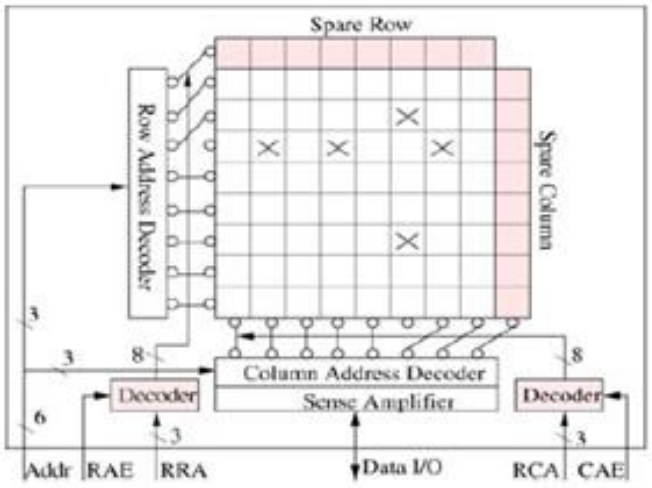

Fig.5. Conceptual diagram of an 8*8 bit-oriented re-pairable RAM with one spare row and one spare col-umn.

2) Built-in Self-Test (BIST) Circuit. It can generate test patterns for RAMs under test. While a fault in a defective RAM is detected by the BIST circuit, the faulty informa-tion is sent to the BIRA circuit.

3) BIRA Circuit. It collects the faulty information sent from the BIST circuit and allocates redundancies accord-ing to the collected faulty information using the imple-mented redundancy analysis algorithm.

4) Fuse Macro. It stores repair signatures of RAMs under test. The fuses of the fuse box can be implemented in different technologies, e.g., laser blown fuses, electronic programmable fuses, etc. The fuse register is the trans-portation interface between the fuse box and the repair

register in the repairable RAM. If a fault is detected, then the fault information is stored in the BIRA circuit.

Then, the BIRA circuit allocates redundancies to replace defective elements. As soon as the repair process is completed, the repair signatures are blown in the fuse box. Subsequently,the repair signatures are loaded into the fuse register first and then are shifted to the repair registers (i.e., registers in the wrappers for storing RRA, RAE, CRA, and CAE data) in normal operation mode. Finally, the repairable RAM can be operated correctly.

EXPERMENTAL RESULTS:

Fig.6 shows the output waveforms of the BIRA module. In this BIRA module it shows the total bits in the bitmap in those bits bit 1 shows the fault information and bit 0 shows fault free information and it also shows the address of the fault row or column according to the given algorithm.

Fig.6.output waveforms of BIRA

Fig.7 shows the output waveforms of the Re BISRmodule. If the signal Bira_enen is asserted, the Re BIRA monitors the signal Fail h which is from the BIST circuitry. If the BIST detects a fault, it asserts the corresponding bit of Fail h signal to 1 and exports the fault information (Address and HS) to the Re BIRA. Also, the Re BIRA sets the Hold l to 1 and the BIST is paused simultaneously.Fig.8shows the output waveforms of the fuse register module. The output register fuse register module stores the repair signature of multiple RAMS in SOC.

Fig.7.output waveforms of Re BISR

Fig.8.output waveforms of fuse register

CONCLUSION: A reconfigurable BISR scheme for repairing multiple re-pairable RAMs with different sizes and redundancy con-figurations has been presented in this paper. An efficient BIRA algorithm for 2-D redundancy allocation has also been introduced. The yield of memory plays major role in SOC designs, the proposed Re BISR effectively increases compare to traditional yield.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

[1] R. Rajsuman, "Design and test of large embedded memories: an overview," IEEE, vol. 18, no. 3, May 2001.

[2] Yu-Ming Jia, Quan-Lin Rao and Chun He "A Memory Built-In Self-Test Architecture for memories different in size," IEEE 2009.

[3] KiamalPekmestzi, Nicholas Axelos, IsidorosSideris and NicolaosMoshopoulos, "A BISR Architecture for Embedded Memories," 14th IEEE International On-Line Testing Symposium 2008.

[4] Muhammad TauseefRab, Asad Amin Bawa, and Nur A. Touba, "Improving Memory Repair by Selective Row Partitioning," 24th

IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2009.

[5] V. Schober, S. Paul, and O. Picot, "Memory built-in self-repair using redundant words," in Proc. Int. Test Conf. (ITC), Baltimore, MD, Oct. 2001, pp. 995–1001.

[6] IEEE 1500 Standard for Embedded Core Test (SECT), IEEE 1500, 2005. [Online]. Available: http://grouper.ieee. org/groups/1500/

[7] IEEE 1149.1 Standard Test Access Port and Bound-ary- Scan Architecture, IEEE 1149.1, May 1990.

[8] T.-W. Tseng and J.-F. Li, "A shared parallel built-in self-repair scheme for random access memories in SOCs," in Proc. Int. Test Conf. (ITC), Santa Clara, CA, Oct. 2008, pp. 1–9, Paper 25.2.

[9] B. Cowan, O. Fransworth, P. Jakobsen, S. Oakland, M. R. Ouellette, and D. L. Wheater, "Onchip repair and an ATE independent fusing methodology," in Proc. Int. Test Conf. (ITC), Oct. 2002, pp. 178–186.0