Reduced Current Harmonics 7 Level ANPC Inverter Using Novel Space Vector PWM

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ABSTRACT

A two-level inverter is one of the widely used multilevel inverter topology for average voltage, high power applications. In this project we proposed 7L-ANPC inverter are operate at fundamental frequency A novel space vector pulse width modulation (SVPWM) scheme for tumbling the common-mode voltage (CMV) in the three-phase seven-level lively neutral-point clamped (7L-ANPC) inverter for the machine drive systems is proposed. This PWM scheme can significantly reduce the common-mode voltage without the augment of switching loss and total harmonic distortion (THD) of the output voltages compared with the conventional one To investigate relationship between the average neutral-point current and zero sequence voltage An finest zero-sequence voltage is calculated to regulate the neutral-point potential. The voltage across the flying capacitor is too regulated by adjusting the switching duty cycles. The DC-link capacitor and flying capacitor voltages can also be restricted for balancing. Each switching period ^operation *time of redundant switch states are varied*

Keywords: Active neutral-point clamp (ANPC), capacitor voltage balancing, multilevel converter, phase-shifted pulse width modulation (PWM), zero-sequence voltage.

I. INTRODUCTION

Multilevel topologies give a clever way of connecting switches in series, thus enabling the processing of voltages that are senior than the device rating. The industry need for medium voltage drive has triggered considerable research in this field, in which most applications consist of drives for pumps, blowers, compressors, conveyors, and the like. In general, multilevel converters are efficient means of reducing harmonic distortion and dv/dt of the output voltages, which makes this technology appropriate to utility interface and drives.

Multilevel converters have turn into popular in recent years due to their high-voltage and high-power ability. They have numerous advantages such as lower harmonic distortion and lower electro-magnetic intrusion (EMI) and reduced stressed of the semiconductor switching devices when compare with the conventional two-level converter. These advantages have complete them particularly attractive for industrial applications such as motor drives, higher static compensators (STATCOMs) high-power high-voltage direct-current (HVDC) power transmission etc. The major multilevel converter topologies are the neutral point clamped (NPC), the brief capacitor (FC) converter and the cascaded H-bridge (CHB) converters.

As the number of levels in the output voltage of a multilevel converter increase, the complexity of the neutral point voltage control of the NPC converter, the stored energy works of the FC converter and the number of isolated power supplies of the

cascaded H-bridge converter increase. This increase in complexity together with the increase in the number of mechanism affects the reliabilityand the efficiency of the converter.

In fresh years, hybrid multilevel converters using different arrangements of conservative multilevel topologies have been introduced. These include the three-level active neutral point clamp converter (ANPC) converter with a FC converter generate a five-level (5L) output waveform, the two-level converter with an H-bridge cell which generates a five-level output waveform plus the three-level NPC converter with an H-bridge cell which generate a seven-level (7L) output waveform.

1.1 Related Works

In [1] Haitham Abu-Rub, Joachim Holtz, Jose Rodriguez, and Ge Baoming et al presents An impression of medium-voltage (MV) multilevel converters with a focus on achieve minimum harmonic distortion and high efficiency at low switching frequency operation. Increasing the power score by minimizing switching frequency while still maintaining sensible power quality is an important requirement and a persistent challenge for the business. Existing solutions are discussed and analyzed based on their topologies, limits, and control techniques. As a preferred option for future research and application, an inverter pattern based on three-level building blocks to generate five-level voltage waveforms is optional. This paper shows that such an inverter may be operated at a very low switch frequency to achieve minimum ON-state and dynamic device losses for highly proficient MV drive applications while maintaining low harmonic distortion. To overcome the limits of semiconductor voltage and current ratings, series and/or parallel connections of plans are being used. Additional measures are then required to balance the voltage distribution at the series connection and the current sharing at the parallel link.

In [2] Seyed Saeed Fazel, Steffen Bernet, Dietmar Krug, and Kamran Jalili et al present The semiconductor loss distribution and the plan of semiconductors and passive components are compared for a medium switching frequency assuming a stable converter efficiency of about 99%. To evaluate the converter individuality in high switching frequency applications, a second comparison is realized for the most switching frequencies assuming a constant cost of semiconductors in all converters. For low- and medium-power industrial applications (e.g., S =

300 kVA to 30 MVA), the majority of drive manufacturer offer diverse topologies of voltage-source converters: two-level voltage-source converters (2L-VSCs) (e.g., Convert am), three-level neutral-point-clamped voltage source converters (3L-NPC VSCs) (e.g., ABB, Convert am, Siemens), four-level flying-capacitor voltage-source converters (4L-FLC VSC) (e.g., Convert am), and series-connected H-bridge voltage-source converters (SCHB VSC) (Siemens). One producer (Allen Bradley) still offers self-commutated current-source inverters (CSIs). To assess the potential of the flying-capacitor topology, 3L-FLC VSC is also measured. A retrofit application demanding an output voltage total harmonic distortion (THD) of fewer than or equal to 5% according to the standard IEEE519-1999 is chosen to assess the quality of the output spectrum and the size of the passive mechanism of an *LC* sine filter

In [3] Makoto Hagiwara, Kazutoshi Nishimura, and Hirofumi Akagi et al presentsThe control and operating presentation of a modular multilevel PWM inverter for a transformer less medium-voltage motor drive. The inverter is important in the modular arm structure consisting of a cascaded stack of many bidirectional chopper-cells. The leading ac-voltage fluctuation with the same frequency as the motor (inverter) frequency occurs crosswise the dc capacitor of each chopper-cell. The magnitude of the voltage fluctuation is inversely relative to the motor frequency. This paper achieves theoretical analysis on the voltage fluctuation, primary to system design. A downscaled model rated at 400 V and 15 kW is intended and built up to confirm the validity and effectiveness of the nine-level (17-level in line-to-line) PWM inverter for a medium-voltage motor drive. Theoretical equations related to ac-voltage fluctuation in both dc capacitor reveal that the ac-voltage fluctuation is proportional to the motor rms existing, and inversely proportional to the motor frequency. Therefore, it is impossible to employ the so-called "volt-per-hertz control" in a range beginning a motor standstill (0 Hz) to a low motor frequency. This paper present the startup method that is suitable but confined to motor drives for energy savings. It can create a startup torque loaded on the motor at a fixed motor frequency, say 30 Hz, bearing in mind the constraints on the motor current and the ac-voltage variation

In [4] Samir Kouro, Mariusz Malinowski, K. Gopakumar, JosepPou et al presents Multilevel

converters have been under explore and development for more than three decades and have found successful developed application. However, this is still a technology beneath development, and many new contributions with new commercial topologies have been reported in the last few years. The aim of this paper is to group and appraisal these recent contributions, in order to establish the present state of the art and trends of the technology, to provide readers with a comprehensive and perceptive review of where multilevel converter technology stands and is heading. This paper first presents a brief impression of well-established multilevel converters strongly oriented to their current state in industrial application to then center the discussion on the new converters that have made their way into the production. In addition, new promising topologies are discussed. Recent advance made in modulation and control of multilevel converters is also addressed. A great fraction of this paper is devoted to show nontraditional applications mechanical by multilevel converters and how multilevel converters are becoming an enable technology in many industrial sectors.

In [5] Zixin Li, Ping Wang, Haibin Zhu, Zunfang Chu et al presents An better pulse width modulation (PWM) method for chopper-cell (or half-bridge) - base modular multilevel converters (MMCs) is proposed. This method can make an output voltage with maximally $2N+1$ (where N is the number of sub modules in the higher or lower arm of MMC) levels, which is as immense as that of the carrier-phase-shifted PWM (CPSPWM) technique. However, no phase-shifted carrier is needed. Compared with the existing sub module united pulse width modulated (SUPWM) method, the level number of the output voltage is approximately doubled and the height of the step in the staircase voltage is reduced by 50%. Meanwhile, the equal switching frequency in the output voltage is twice that of the conservative SUPWM method. All these features lead to much reduced harmonic content in the output voltage. What is additional, the voltages of the sub module capacitors can be well balanced without any close-loop voltage opposite controllers which are mandatory in the CPSPWM schemes. imitation and experimental results on a MMC-based inverter show legality of the proposed method.

II.EXISITING SYSTEM

2.1 3 Level Inverter

The performance is highly dependent on the applied current control strategy and the connected AC network situation. The inverter output turns into a sinusoidal output as the number of levels increases with enlarge the harmonics. The switches are actuated by switching manage signals beginning the control system to selectively couple the AC terminals to one of the DC terminals is choosy are high complexity A first set of switching devices coupled with the DC association and the first AC terminal, the first set operable in one of three state to selectively electrically couple the first AC terminal to one of the first DC terminal, the second DC mortal, and the common node according to a first set of switch control signals, A second set of switching devices coupled with the DC association and the second AC terminal, the second set operable in one of three states to selectively electrically combine the second AC terminal to one of the first DC terminal, the second DC fatal, and the common node according to a second set of switching control signals, and A third set of switch devices coupled with the DC connection and the third AC fatal, the third set operable in one of three states to selectively electrically couple the third AC fatal to one of the first DC terminal, the second DC terminal, and the common node according to a third set of switch control signals
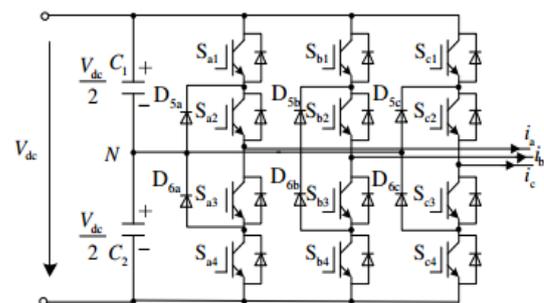
2.2 3 Level Inverter Circuit Diagram

Fig 2.2 Circuit diagram of 3-Level npc inverter

2.3 NPC Converter

There are three generally commercial secret topologies of multilevel converters in the literature as diode clamped converters cascaded Hbridge converters, plus flying capacitor converter. Among the various multilevel converter topologies, the nearly all popular topology in high power industrial application is the three level neutral point clamped (NPC) voltage source inverter (VSI), which was planned by Nabae et al as shown in Fig . 2.2

One advantage of the three levels NPC VSI topology is that the power switch and the dclink capacitors have to endure only one-half of the dc link voltage. As a effect, the converter can deal with double voltage and power value than in a normal two level VSI with the same switching frequency. However, the drawback of this topology are the higher number of power switches, which adds difficulty to the modulation method. In addition the voltage balance of the dclink neutral point is necessary.

III.PROPOSED SYSTEM

3.1 Proposed 7 Level ANPC

The series-connected or high-voltage switch are operated at fundamental frequency and the other switch are controlled with SV-PWM. The voltage balancing of the FCs is also achieved by adjusting the switch duty cycles of two PWM signals 7L-ANPC inverter topology two auxiliary switch are added for the purpose of clamping instead of clamping diodes as in 7L-NPC. These support switches are introduced to ensure the equal voltage allocation between the main and auxiliary switches. Moreover in unlike NPC inverter, in ANPC inverter the DC link capacitor voltage will naturally balance under normal process of inverter. The voltage of flying capacitors can naturally balance to the necessary level in order to generate multilevel waveform
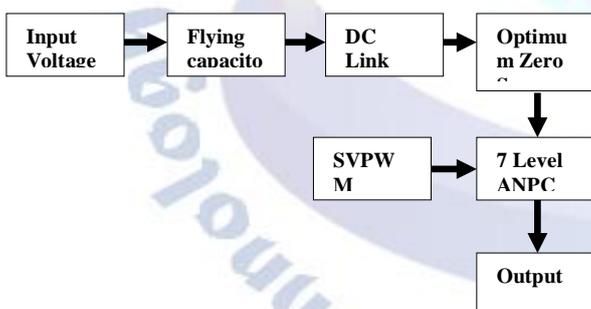
3.2 BLOCK DIAGRAM

Fig3.2 Block diagram of 7-Level ANPC Inverter

3.3 equivalent circuit

The voltage stress crossways the outer ($S1$) switches of the topology is higher compared to the stress crossways the FC cells ($Sc1$–$Sc3$) and the converter requires series connection of switching devices or diverse semiconductor technologies to be used in the configuration, for the converter to reach its full score. In order to minimize the pressure across the outer switches, their switching frequency is selected equal to the basic frequency at the output. The converter operates in two distinct half-periods during a basic period, one at which the upper DC-link capacitor ($C1$) is linked to

a phase and a second where the lower DC-link capacitor ($C2$) is used. During these half-periods, the topology simplify to a four-level FC converter and for which the FC balancing supplies can be identified.
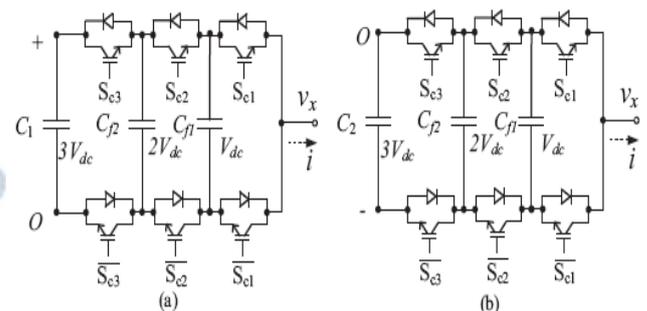

Fig3.3 Equivalent circuits during the half-periods of operation, a) Positive half-periods, b) Negative half-period

The equal circuits for one phase of the converter during the two half-periods of operation are given in Fig. The restriction of fundamental frequency in the outer $S1$ switches of the topology limits the available states of the three-level ANPC to four. This also li mits the numeral of states that generate the zero voltage level to one for every of the half-periods in the waveform. The state that produces NPCthe zero voltage level during the optimistic half period ($V9$) is denoted as (+)0 while the state ($V8$) that generates the zero voltage level throughout the negative half-period is denoted as (−)0. The limitation in the switch states of the three level ANPC, in mixture with the two states of each FC cell, offer a total of sixteen switching states for the seven level ANPC topology
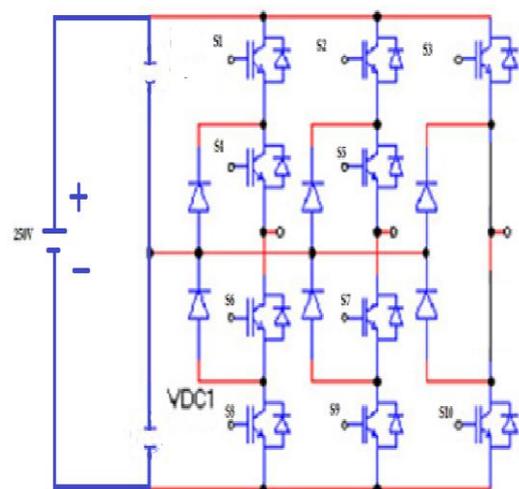
3.4 Circuit Diagram

Fig3.4 Circuit diagram of 7-Level ANPC Inverter

3.5 Switching Process

In order to reduce the switch frequency of the individual components and eliminate needless switching's in the converter, the switching state of the converter is only evaluate and changed when there is a change in the level of the production waveform. The modulator will not change the switch state in case the cell that deviates the most from the reference change within one switching period but will wait to the next switching interval The future generalized modulator requires measurement stage of the converter.

Additionally the output current has to be measured as the division of the current is essential for the modulator. The implementation can be directly used for single-phase configurations and, because the measurements and inputs to the algorithm are not dependent on the residual phases, can be applied per phase for multiphase systems. The voltage complementary of the two DC-link capacitors and hence the NP voltage is natural and can be maintain as the two FC voltages are regulated to their reference. Additionally, a feed forward method making an allowance for the deviation of the DC-link capacitor voltages can be implemented to increase speed the natural balancing process.

3.6 Simulation Result
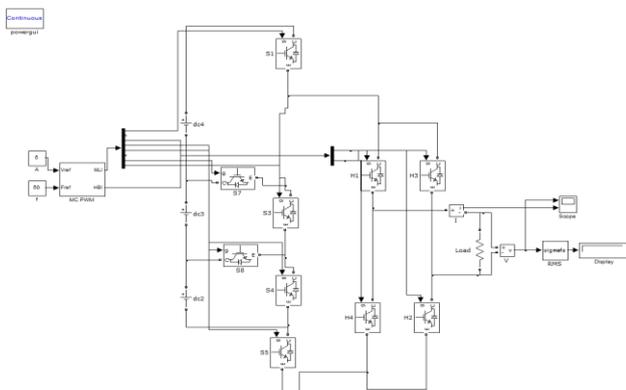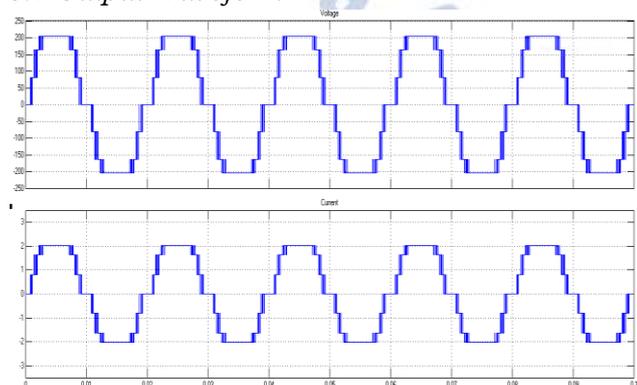

3.7 Output Waveform

Fig.3.7 output waveform of voltage and current

IV.CONCLUSION

A generalized modulator for the seven stage flying capacitor based ANPC converter. The hybrid converter is based on the mixture of a three-level ANPC converter with two flying capacitor cells. The proposed general modulator is applied independently to each phase of the converter and is appropriate for single or multi-phase applications. The modulation procedure is separated into two stages. The first stage utilizes the commands of the controller in order to generate a target waveform for the second stage of the modulator. The second stage select the switching states of the converter based on the target waveform provide by the first stage of the modulator and on the measurements of the FC voltages and the phase present. The hybrid seven-level cascaded ANPC based multilevel converter under selective vocal elimination (SHE) PWM is analyzed in this paper. The topology is based on the cascade connection of a three-level ANPC converter and entity H-bridge sub-modules for each phase of the converter. This configuration offers control of the switching dead across the ANPC switches and provides regulation of the voltages across the floating capacitors. The obtainable utilization of the converter extends the operation range of converters with similar DC-link voltage as the SHE-PWM provides elimination of low order harmonic and maintain the switching frequency of the power semiconductors low. A variable hysteresis band base on the analysis of the floating capacitor voltage ripple is considered to minimize added switching in the converter

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