# FPGA Implementation of Fault Tolerant Parallel Filters Based on Multiple bit Error Correction using Hamming Code

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**ABSTRACT**

*The paper describes about fault tolerant parallel filters based on Hamming Code for multiple bit error correction. This filter is used on the system when is important for reliability. The ECC using in every output bit of the filter and it's correct the error in output. For multiple bit error correction to use the hamming code as a ECC in this paper. This novel scheme of ECC allows more efficient protection. Another name of this technique is soft error correction. From analysis of the architecture the efficiency of the error correction is more compare to existing system and the leakage power is 0.113W.*

***KEYWORDS:*** *Hamming code, error correction codes, filters.*



## I. INTRODUCTION

In the automotive, medical and space applications the present of electronics circuit is increased nowadays so, the devices reliability in this field is very important but the circuits are generate the some degree of fault tolerance. The tolerance of the devices is protected by Error correction codes.

Various methods are used for to protect a circuit from errors. One in the middle of the common techniques which can be used to correct the error is triple modular redundancy (TMR) [1]. The TMR technique attaches auxiliary data by three times in the data. The signal processing circuits for which Sum of Square (SOS) checking methods have been proposed [2]. This is a one of the error detection technique. It's impossible to detect all the faults.

Digital filters utilized as a part are finite impulse response (FIR) filters. As an example, reduced precision repeated data were utilized in FIR filters by reduce the area of implementing modular redundancy [3]. Soft errors possible to change the logical value of a circuit node creating a temporary error that can affect the system function. To ensure that soft errors do not affect the function of a circuit, a more different of techniques can be used [4]. Be classified among options is to design basic circuit blocks to minimize the probability of soft errors.

In this paper to introduce related work of the paper in section II. Then, in section III, we are discussed proposed system and hamming code. Section IV presents the simulation result of the paper. Finally Section V presents the conclusion of the paper.

## II. RELATED WORK

### A. *The same response based parallel filter*

A discrete time based filter implements the following equation:

$$y[n] = \sum_{l=0}^{\infty} x[n-l].h[l] \quad (1)$$

Where $x[n]$ - input signal,

$y[n]$ - output,

$h[l]$ - impulse response of the filter.

When the impulse response $h[l]$ is nonzero, only for the samples are finite number, the filter is known as a FIR filter, otherwise the filter is an infinite impulse response (IIR) filter. There are several structures to implement both finite and infinite impulse response filters. In the following, a set of $k$ parallel filters with the similar response and divergent input signals are considered. These parallel filters are illustrated in Fig. 1. This kind of filter is found in some communication systems that use several channels in parallel. In data acquisition and processing applications is also common to filter several signals with the similar response. An interesting property for parallel filters is that the sum of any combination of the outputs $y_i$ [$n$] can also be obtained by summing the corresponding inputs $x_i$ [$n$] and filtering the resulting signal with the similar filter h.

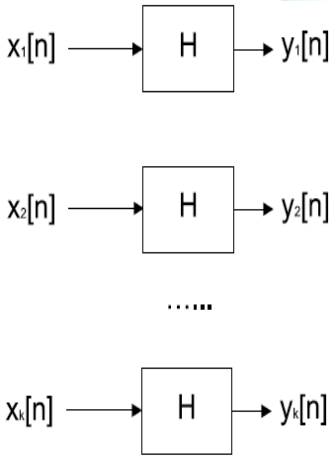


**Fig. 1. Parallel filters with the similar response.**

## III. PROPOSED SYSTEM

In proposed design to use the Hamming code for multiple bit error correction technique. The architecture for proposed system is show in figure 2. This is consists of the coding block, general block and redundant block. The redundant block is sum the input with different format for detect and correct the error in the output of the filter.

The data are given to the original module and coding block. The original module is generating the respective output for filter. The coding is sum the given signal and pass to the redundant block. The output of the original module (y1,y2,y3,y4) and redundant module (z1,z2,z3) is pass to the multiple bit error correction block, then the errors are detect and corrected in the multiple bit error correction block by using the hamming code.

### *A. Hamming code*

The new technique is based on the uses of the ECCs. A simple ECC takes a block of k bits and produces a block of n bits by adding n−k parity check bits. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. As an example, let us consider a simple Hamming code with k = 4 and n = 7. In this case, the three parity check bits p1, p2, p3 are computed as a function of the data bits d1, d2, d3, d4 as follows:

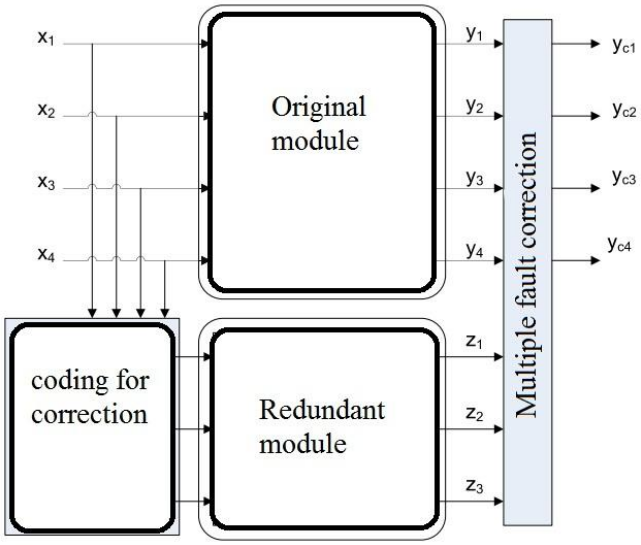


**Fig. 2. Proposed system architecture.**

p1 = d1 XOR d2 XOR d3

p2 = d1 XOR d2 XOR d4

p3 = d1 XOR d3 XOR d4. (1)

The data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by re-computing the parity check bits and comparing the results with the values stored. In the example considered, an error on d1 will cause errors on the three parity checks; an error on d2 only in p1 and p2; an error on d3 in p1 and p3; and finally an error on d4 in p2 and p3.Therefore, the data bit in error can be located and the error can be corrected. This is commonly formulated in terms of the generating G and parity check H matrixes.

Generating and parity check matrixes of the Hamming code is given below

$G$ =
1 0 0 0 1 1 1
0 1 0 0 1 1 0
0 0 1 0 1 0 1
0 0 0 1 0 1 1
$H$ =
1 1 1 0 1 0 0
1 1 0 1 0 1 0
1 0 1 1 0 0 1

Encoding is successfully processed based on y = x XOR G and error detection is successfully processed based on s = y XOR $H^T$. Correction is done using the vector s, known as syndrome, to identify the bit in error. Once the erroneous bit is identified, it is corrected by simply inverting the bit.

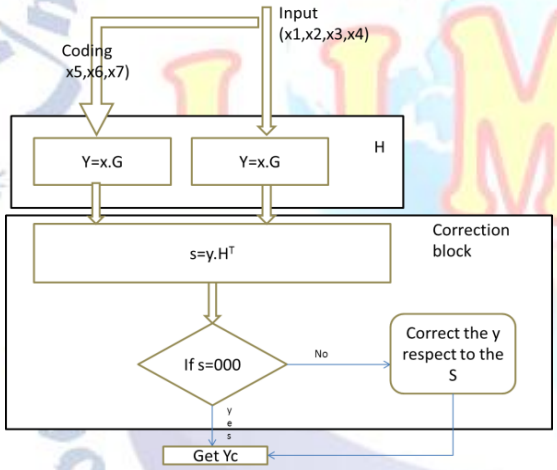


**Fig. 3. Multiple bit error correction flow.**

## IV. SIMULATION AND RESULT

The simulate the proposed system architecture in Modelsim and to analysis the area, power, and delay of the proposed system in Spartan 6 by using Xilinx software. The simulation result for the filter is shows in figure 4. The synthesis report of the proposed system is shown in fig 5. Finally the comparison of the proposed system is detailed in table I.

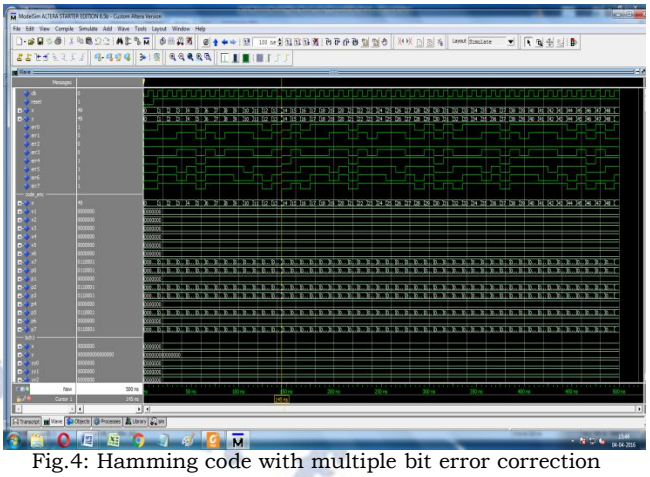

Fig.4: Hamming code with multiple bit error correction simulation result

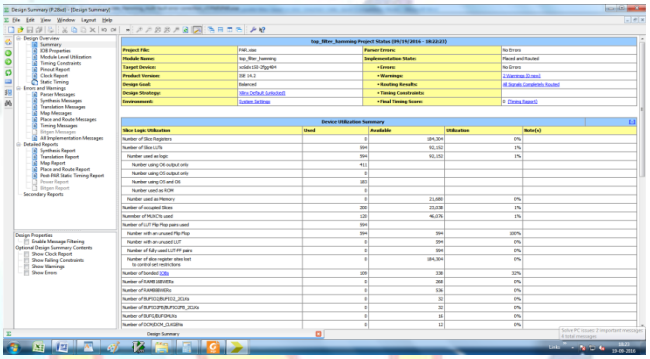

**Fig.5: Hamming code with multiple bit error correction synthesis report**

**Table 1: comparison**

| | Existing system | Proposed system |
|---|---|---|
| **Area** | 48 | 743 |
| **Power (W)** | 0.10 | 0.113 |
| **Delay(ns)** | 12.05 | 41.05 |

## V. CONCLUSION

This brief has presented a novel scheme to protect parallel filters. The design of the fault error correction based filter using hamming codes is gives the efficient error correction. So finally we are design an efficient architecture design for Error correction. In future to use the others ECC's for the multiple bits error correction.

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