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Area Efficient Pulsed Clock Generator Using Pulsed Latch Shift Register

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ABSTRACT

Shift Registers are building blocks used for the storage of data in many devices. Currently, Flip flops which have been used in Shift Registers consume more Power and impose a heavy load on Clock distribution networks. The Proposed work overcomes the Power consumption and reduces the delay by using the Pulsed Latches instead of the Flip flops. Conventional Latches-Static differential Sense Amplifier Shared Pulse Latch (SSASPL) has been used where the number of Transistors has been reduced. Trigger generator is used to give non overlap clock signals to the memory elements, which reduced the delay and produced the fast implementation of the data. The Power consumed reduces by 27% and delay reduces by 21% when compared to the Shift Registers using Flip flops.

KEYWORDS: Area efficient, pulsed clock generator, pulsed latch, shift register.

I. INTRODUCTION

Low power circuit design has emerged as a principal theme in today's electronics industry. In the past, major concerns among researchers and designers for designing integrated circuits were on area, speed, and cost; while secondary importance was paid to power dissipation. In recent years, however, this scenario has changed and now developing of different circuit techniques for low power circuit design is an important research area. On designing any combinational or sequential circuits, the power consumption, implementation area, speed, voltage leakage, and efficiency of the circuit are the important parameters to be considered initially. These parameters are inter related to each other so in order to obtain few parameters remain may have less preference. Shift register have several type of applications like data conversion between parallel to serial or serial to parallel, counters, parity generator, etc. Coming to the real time applications like image processing ICs [4]-[6], digital filters [1] and communication receivers [3] also we are using shift registers. Let consider the shift register application in image processing. As the size of the image data continues to increase due to the high demand for High quality image data, the word length of the shifter register increases to process large image data in image processing ICs [3]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. Our proposed project is to reduce the power and area of the circuit by replacing the flip-flops with the latches in the shift register.

Technology has invaded into the life of human beings to such deep extent that today everyone has a wish for smaller faster fancier gadgets. This wish

has been granted to them by the technological developments in the field of VLSI technology. A SHIFT register is the basic building block in a VLSI circuit. Shift registers find them to be use full commonly in many applications, such as digital filters, communication receivers, and image processing ICs. Now a days, as there is high demand of images with utmost clarity the size of the image data continues to increase, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

The designing of a shift register is quite simple. An n bit shift register is composed of series connected N data flip-flops. The speed of the flip flops is of no major constraint here as there are no connections between the shift registers and flip flops. The smallest flip flop is enough to drive the requirement of the shift register and for this same reason the pulsed latches have replaced the flip flops as they are much smaller in size Vis a Vis the flip flops there by reducing power consumption. Although there are some drawbacks like that of the timing problem, which is easy to overcome by the use of multiple clocked pulses instead of a simple single pulsed clock. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bi stable multi vibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. Flip-flops and latches are used as data storage elements. A flip-flop stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

II. Related Work

In conventional method shift register is designed by serial connection of the master-slave flip flops. The following figure shows the master slave flip flop.

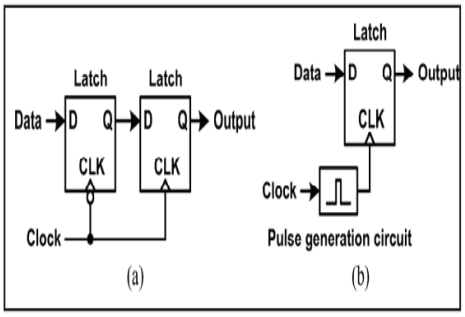

Fig. 1: Master Slave Flip Flop

The PowerPC master–slave latch(Fig. 1), presented in [2], is one of the fastest classical structures. Its main advantages are a short direct path and low-power feedback. But one has to keep in mind another aspect of this structure is its large clock load [5], which greatly influences the total power consumption on-chip.

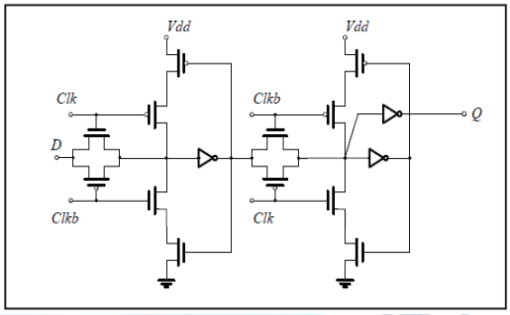

Fig. 2: PPCFF

Hybrid-latch flip-flop (HLFF) (Fig. 3), presented in [8], and is one of the fastest structures presented. It also has a very small PDP. The major advantage of this structure is its soft-edge property, i.e., its robustness to clock skew. One of the major drawbacks of the hybrid design in general is the positive hold time. Due to the single-output design, the power consumption range of the HLFF is comparable to that of the static circuits. However, depending on the power distribution, pre charged structures can dissipate more than static structures for data patterns with more “ones”. Hybrid design appears to be very suitable for high-performance systems with little or no penalty in power when compared to classical static structures [7].

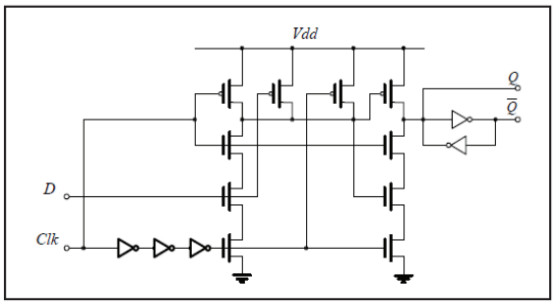

Fig. 3: HLFF

Another interesting approach to hybrid design is the semi-dynamic flip-flop (SDFF) structure (Fig. 4) presented in [10].It is the fastest of all the presented structures. The significant advantage over HLFF [9] is that there is very little performance penalty for embedded logic functions. The disadvantages are bigger clock load and larger effective pre charge capacitance, which results in increased power consumption for data patterns with more "ones." This is still the most convenient structure or applications where speed is of primary importance, without a big penalty in power consumption.

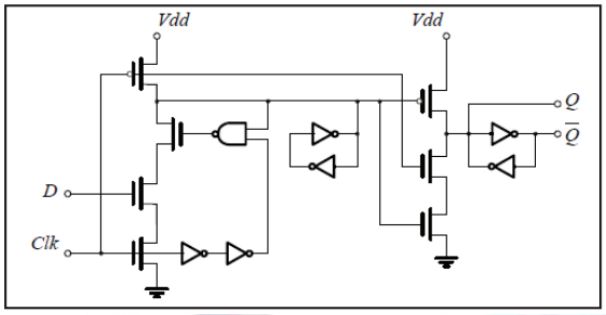

Fig. 4. SDFF

Optimized shift register designs are not achieved with the use of master-slave flip flops. Performance parameters such as area and power can be reduced with use of pulsed latches. Hence master-slave using two latches are can be replaced by pulsed latch consisting of latch with pulsed clock signal [7] which is shown in fig. 5.

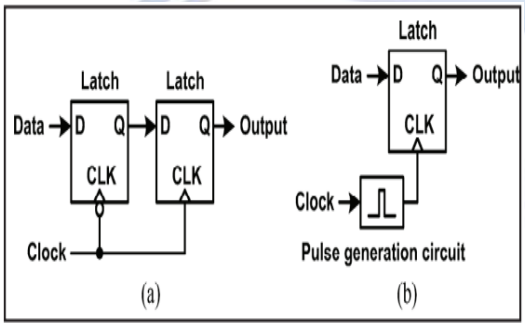

Fig. 5: Pulsed Latch

III. IMPLEMENTATION

Proposed work is a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch cannot be used in shift registers due to the timing problem occurred in latch. The following figures show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the inputs signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

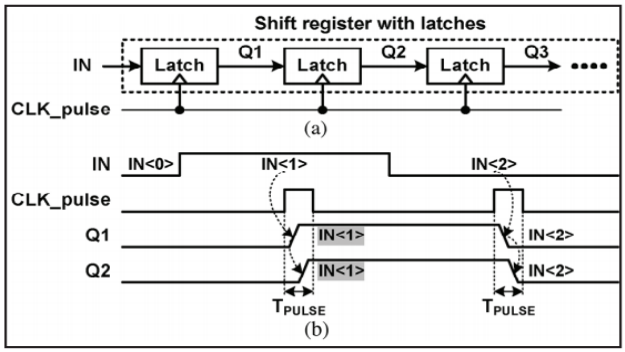

Fig. 6(a): Series Connection of Latches (Shift Register) (b) Timing Problem in Latches.

This timing problem can be overcome with the use of multiple non overlapped delayed pulsed clock signals. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. Below figure shows an example the proposed shift register. The proposed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK _pulse<1:4> and CLK _pulse<T>). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Five non-overlaps delayed pulsed clock signals are generated by the delayed pulsed clock generator. The operations of the other sub shift

registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

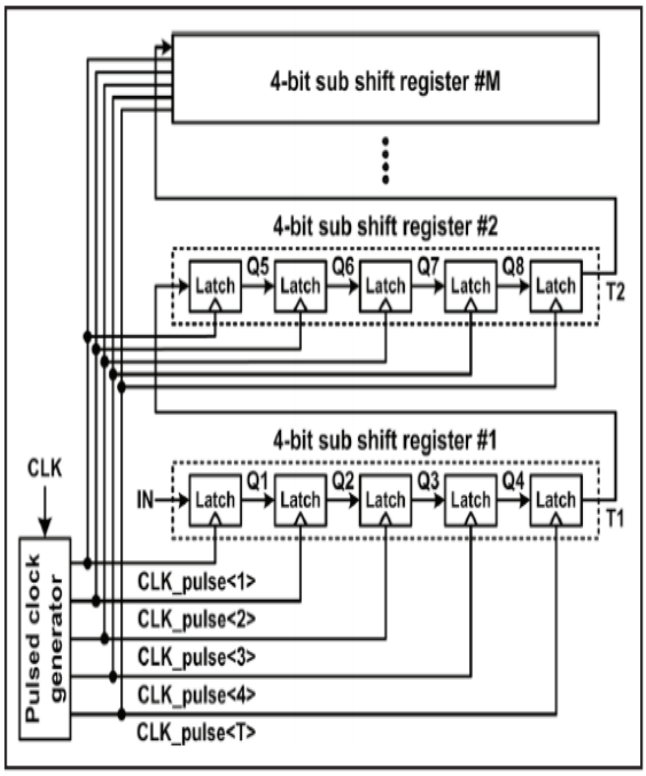

Fig. 7: Proposed Shift Register

When an N-bit shift register is divided into K-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1latches requires K+1 pulsed clock signals. The number of sub shift registers M becomes N/K, each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches. A 64-bit shift register with sub shift register size 4 (K=4) requires 16 sub shift registers. And each sub shift register consist of 5 latches. Below figure is the pulse clock generator. Which gives the multiple non overlap delayed pulse clock signals for K-bit sub shift register.

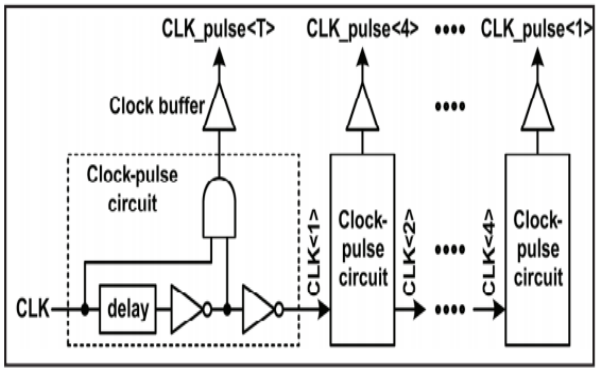

Fig. 8: Non Overlap Clock Pulse Generator

IV. Experimental Results

To compare the performances of the proposed shift register with the flip-flop based shift register, each circuit was designed using 180nm technology with VDD=1.8V, fCLK=100MHz, Temp=250Cand simulated with HSPICE. The Avan waves for the three comparators are shown below.

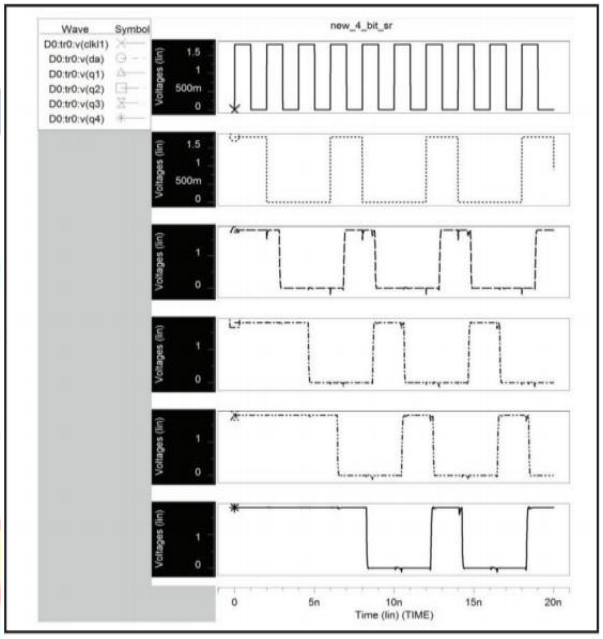

Fig. 9. Simulated waveforms for SSASPL four bit shift register

Table 1 shows the performance comparisons of shift registers. The conventional shift register using flip-flops was implemented with the PPCFFs. The proposed shift register using pulsed latches were implemented with the SSASPLs. The proposed shift register achieves a small area and low power consumption compared to the conventional shift register as the numbers of transistors are less.

Table 1

Size of SR	Shift Register using SSAPL (Pulsed Latch)		Shift Register using PPCFF (Flip-Flop)	
	Total No. of transistors	Power (mW)	Total No. of transistors	Power (mW)
4-BIT	103	0.227	64	0.140
8-BIT	138	0.241	128	0.224
16-BIT	208	0.274	256	0.343
32-BIT	348	0.311	512	0.373
64-BIT	628	0.313	1024	0.422

V. Conclusion

The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. A 64-bit shift register was implemented

using a 0.18 um CMOS technology with vdd=1.8V at clock frequency of 100 MHz. which consumed the power and area compared to conventional method that is shift register using flip flops.

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

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