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Average Phase-Leg Technique on Coupling Impedance Impact Modular Inverter Parallel Connection Performances

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ABSTRACT

The modular multilevel converter (MMC) is an emerging and highly attractive multilevel converter topology for high-voltage and high-power applications. This paper proposes the control method of parallel-connected modular multilevel converters (parallel-MMCs), which assumes that the multiple MMCs are directly connected at both ac and dc sides to effectively enhance the power rating as expected. Two key problems were first solved for the parallel-MMCs under the normal operation conditions: voltage balancing of sub modules and mitigation of circulating currents, where the novel transformed third-order harmonic resonant controller in the synchronous reference frame was employed to mitigate the dominant second-order and fourth-order circulating currents and a sixth-order harmonic resonant controller is used to attenuate the zero-sequence sixth-order circulating current existed in all phase currents per MMC. Considering the high risk of switches fault in the parallel-MMCs, the fault-tolerant operation schemes were then proposed in this paper to address the major concerns of open-circuit and short-circuit switch fault in a sub module, respectively. Carefully controlling the healthy sub modules and the corresponding phase arms, the parallel-MMCs can successfully maintain their balanced capacitor voltages and mitigate the circulating currents with the qualified output waveform obtained. In addition, the parallel configuration of MMCs provides the unique solution for the short-circuit switch fault operation which was seldom discussed in the published literature works with respect to the MMC fault-tolerant operation schemes. MATLAB simulations and the constructed experimental prototype have verified the performance of the proposed control strategy.

KEYWORDS: *Average phase-leg technique, Coupling Impedance Impact Modular inverter Parallel connection Performances*

I. INTRODUCTION

The modular multilevel converter (MMC), which has been originally presented in [1] and [2], is suitable for the applications of high-voltage dc (HVDC) power transmission [3]–[5],adjustable speed motor drives [6], reactive power compensation[7], etc., mainly due to its inherent advantages of the modular structure and the low output voltage/current harmonics. Inside the MMC, every half-bridge converter is considered as a sub module (SM) as shown in Fig. 1, which can be simply cascaded to increase the dc-link voltage to a desired value. However, as the power increases or in other words when the MMC has to handle the high current, a single MMC is increasingly viewed as inappropriate, restricted mainly by the present semiconductor manufacturing technology without any immediate solution. One intuitive solution is to assume the compact integrated parallel-connected semiconductor switches in each SM, which however need a complicated gate driver to guarantee the simultaneous turning ON/OFF of parallel switches. Besides, as suminga single module with more than two switches connected in parallel would be impractical since the uneven loss distribution, which cannot be simply solved by the gate driver [8], would cause operational failure especially under the high-power high current application conditions. Otherwise, an overdesigned heat dissipation system should be employed, which

unfortunately will increase the system cost significantly. Another solution is to assume the parallel-connected setups to equally divide the

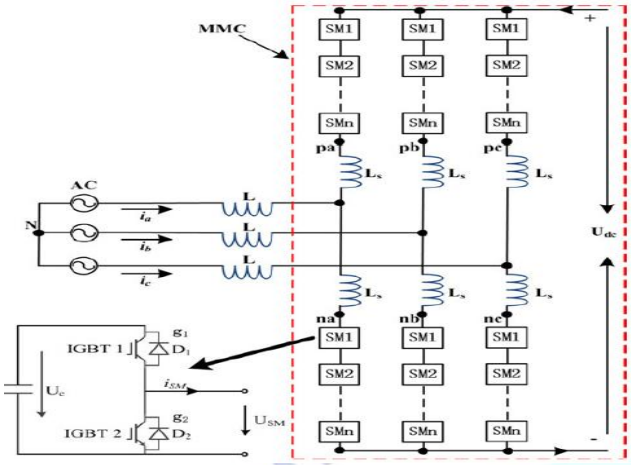

Fig. 1. Topology of the MMC.

Processed current into each setup, where the dc-link and the ac output terminals are directly connected together. The latter has been widely implemented in two-level converters [9]–[11].Assuming that the parallel-connected MMCs (parallel-MMCs)will not only effectively increase the power rating as normally expected, but also significantly enhance the operational reliability by both reducing the thermal design burden and providing the unique solutions for semiconductor fault-tolerant operation. However, the parallel configuration of the MMC has been less reported.

In order to successfully implement the parallel-MMCs, two keys issues should be carefully addressed. One is the mitigation of internal and external circulating currents introduced in each phase and between the parallel-MMCs, respectively. Another is the switch fault-tolerant operation scheme without using the expensive redundant hardware to enhance the operational reliability, which is deemed as necessary in a complex multilevel power conversion system. Putting two MMCs in the parallel operation as shown in Fig. 2 would face the situation of cross coupling between the parallel-MMCs because when two MMCs are connected to the same dc bus and ac source/load, the extra zero-sequence circulating current (ZSCC) will result in the unexpected current distortion and the unbalanced load sharing, which would consequently result in the operational failure. Traditionally, in order to avoid this problem, transformers are used in an ac source/load side to isolate the direct current flow. However, the transformer is costly and bulky. As reported

In [12]–[15], the parallel-connected converter can assume a specific control method to attenuate the ZSCC. However, when this method is assumed in the parallel-MMCs, both MMCs should first maintain their dc capacitor voltages of all SMs to be equal. When the voltages of all SMs are balanced, the dc-link voltage can be treated as a constant value when assuming a proper modulation method, thus the parallel-MMCs can be simplified as the two-level converters to attenuate the external ZSCC. Besides, the internal circulating currents should be minimized to reduce the losses. Many papers have reported the internal circulating current control methods [16]–[21], which in principle, control the second-order harmonic current flowing through the phase arms or in addition control the higher order fourth-, sixth-, and eighth-harmonic currents as the added control targets to smooth the internal circulating current, where the well-known resonant controllers are assumed to attenuate each order harmonics. Zhang *et al.* [22] assumed the repetitive controller to attenuate the circulating current. In order to reduce the calculation burden, this paper proposes a transformed third-order harmonic resonant controller in the synchronous reference frame to attenuate both dominant second- and fourth-order circulating harmonics per phase and additionally assumes a generalized sixth-order resonant controller to control the zero-sequence sixth-order circulating harmonic current in all phases per MMC.

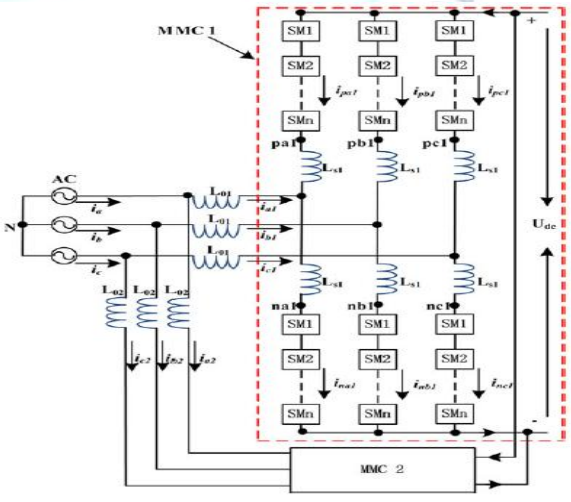

Fig. 2. Topology of the parallel-MMCs.

The high risk of semiconductor switching failure induced by the open-circuit or short-circuit fault in parallel-MMCs cannot be ignored, whose most direct solution is to install a redundant phase-leg connected to the output terminals of normal phase-legs using the triacs the same as that

assumed in the low-level power conversion system. Such hardware redundant configuration is expensive and seldom adopted in a high-voltage multilevel converter. The alternative solutions by adjusting the redundant pulse width modulation (PWM) signals in multilevel converters were presented in literature works to compensate the output performance [23]–[26]. The unique configuration of the MMC, however, is not suitable for the one fold PWM compensation scheme under the switch fault-tolerant operation conditions since the dc capacitor in a failure SM has to be inserted

$p = 2k - 1$.

in the arm current flowing loop in most of the switching failure cases resulting in the dangerous overvoltage operation. Therefore, before assuming the PWM compensation scheme,

The faulty SM should be bypassed first by using an additional bypass switch connected between the output terminals per SM as suggested in [27]. Using the bypass switch can only effectively solve the switch open-circuit failure problem, leaving the case of upper semiconductors (IGBT1 or D1 in Fig. 1) short-circuit failure per SM unsolved. But thanks to the parallel configuration, the parallel-MMCs can ride through all open-circuit and short-circuit semiconductor failure operation conditions using the proposed PWM compensation scheme and the revised control method in this paper without any additional assisted hardware; meanwhile, the proposed control scheme can effectively attenuate all circulating currents as well without sacrificing the output performance.

II. Multilevel Inverter

2.1 Multilevel Concept:

This paragraph has the aim to introduce to the general principle of multilevel behavior. Figure 3.1 helps to understand how multilevel converters work. The leg of a 2-level converter is represented in Figure 3.1a) in which the semiconductor switches have been substituted with an ideal switch. The voltage output can assume only two values: 0 or E. Considering Figure 3.1b), the voltage output of a 3-level inverter leg can assume three values: 0, E or 2E . In Figure 3.1c) a generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, and then the voltage levels can be different. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following.

A three-phase inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is n. The number k of the line-to-line voltage levels is given by

$k = 2n - 1$.

Considering a star connected load, the number p of phase voltage levels is given by.

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels.

Higher is the number of levels better is the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 2-level inverter.

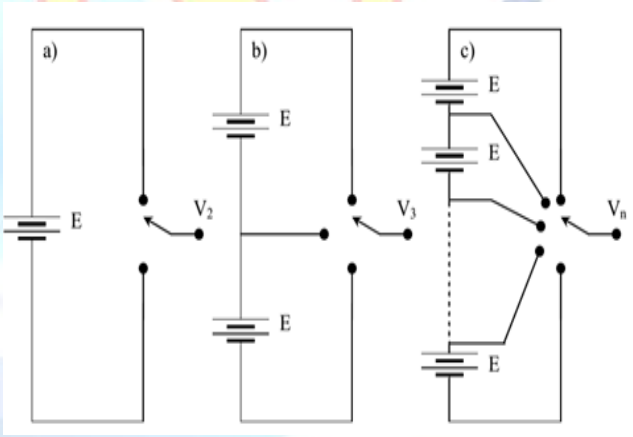

Figure 2.1: Inverter phases. a) 2-level inverter, b) 3-level inverter, c) n-level inverter.

2.2 Multilevel Inverter Performance

The limit of standard three-phase converters is related to the maximum power. Which can be delivered to the load, which is related to the maximum voltage and current of a component? Furthermore, higher is the power of a switch lower is the switching frequency. An initial solution to overcome this problem was to connect several switches in series or in parallel. The series connection of two or more semiconductor devices is really difficult due to the impossibility to perfectly synchronize their commutations. In fact, if one component switches off faster than the others it will blow up because it will be subjected to the

entire voltage drop designed for the series. Instead, parallel connection is slightly less complicated because of the property of MOSFETs and more recent IGBTs to increase their internal resistance with the increment of junction temperature. When a component switches on faster than the others, it will conduct a current greater than the current it was designed for. In this way, the component increases its junction temperature and its resistance, so it limits the current which flow through it. This effect makes possible to overcome the problems coming from a delay among gate signals or from differences among real turn on time of the components. Anyway, parallel connection of the switches requires an accurate design of the board.

A modular solution is preferred to increase the power a converter can drive. In this way, a standard three-phase converter is designed with a relatively low power. Then, several converters are paralleled through decoupling inductances to reach the desired power. Even in this system a quite good synchronization among the controls of the converters is required.

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, multilevel converters present several other advantages. First of all, multilevel converters generate better output waveforms with a lower $\frac{dv}{dt}$ than the standard converters. Then, multilevel converter can increase the power quality due to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses. Furthermore, multilevel converter can operate with a lower switching frequency than 2-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Furthermore, multilevel converters can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less electromagnetic interference, and lower harmonic content .The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources

2.3 Diode-Clamped

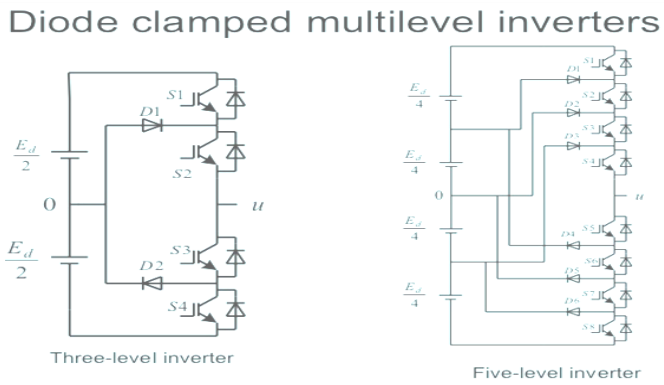

Fig2.2 diode clamped multilevel inverters

III. IMPLEMENTATION

3.1 Illustration of the parallel-MMC and its voltage Balancing control method:

Fig. 2 shows the circuit topology of the presented parallel-connected MMCs. The configuration of both MMCs is identical, where each MMC consists of six converter arms, which are constructed by a cascaded connection of SMs with a buffer inductor connected in series. As shown in Fig. 1, a half-bridge converter and a dc capacitor constitute the SM, where the terminal between two switches (IGBT1 and IGBT2) and the negative dc-rail terminal will connect to the adjacent SMs to form the aforementioned cascaded connection of single converter arm. And one phase leg consists of two arms, which are named as the positive arm and the negative arm, respectively. The buffer inductors L_s limit the circulating currents among six phase-legs in the parallel-MMCs.

The general control diagram of parallel-MMCs for grid-tied applications is illustrated in Fig. 3, where the general control function is realized by the voltage-balancing control blocks and circulating current suppression control (CCSC) blocks for MMC 1 and MMC 2 and the external ZSCC control block. The de-coupled current control block is assumed to generate the fun-demented control reference in the grid-tied applications, which may vary depending on the application cases. A general three-phase PLL is assumed to obtain the phase angle, which is not drawn in Fig. 3. In what follows, we will illustrate the capacitors voltage balancing control method in detail, whose control principle is suitable for the parallel-MMCs operated under both the normal operation condition and the switch fault-tolerant op-elation conditions.

In general, the voltage-balancing control method of the MMC can be divided into the following two specific control blocks [28]–[31]:

1) individual voltage control;

2) average voltage control

A. *Individual Voltage Control*

Fig. 4(a) shows the control diagram of individual voltage control per SM, where u^j_{pxi} and u^j_{nxi} ($i = 1, 2, \ldots n$, $x = a, b,$

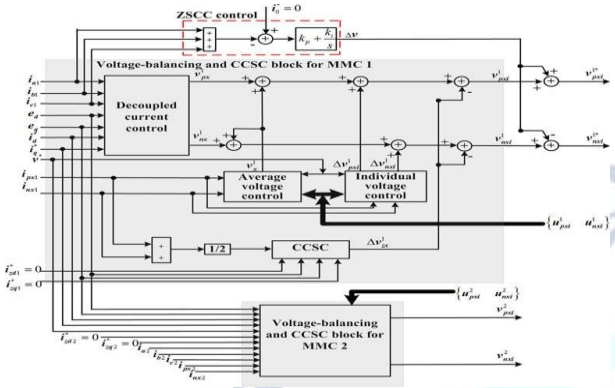

Fig. 3. General illustration of the control method of parallel-MMCs.

B. *Average Voltage Control*

The principle of average voltage control is to control the averaged phase voltage by regulating he circulating current, whose control diagram is illustrated in Fig. 4(b), where $\bar{v}jx$ and $izxj$ are the averaged dc voltage and circulating current per phase calculated as follows:

$$\begin{cases} \bar{v}_x^j = \dfrac{1}{2n}\left(\sum_{i=1}^{n} u_{pxi}^j + \sum_{i=1}^{n} u_{nxi}^j\right) \\ i_{zxd} = \dfrac{1}{2}(i_{pxj} + i_{nxj}) \end{cases} \quad (2)$$

After a fine-tuned PI controller, the error between the averaged dc voltage and the dc voltage reference will be amplified as the dc-loop current reference between the positive arm and the negative arm per phase. Doing so, the measured circulating current per phase can follow this generated reference to tune the averaged dc voltage $\bar{v}jx$ through the second PI controller.

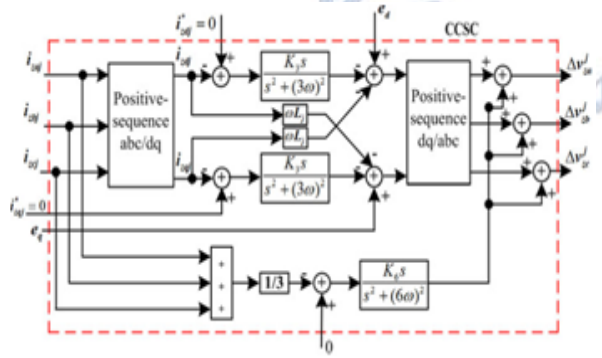

Fig. 5. Block diagram of internal CCSC.

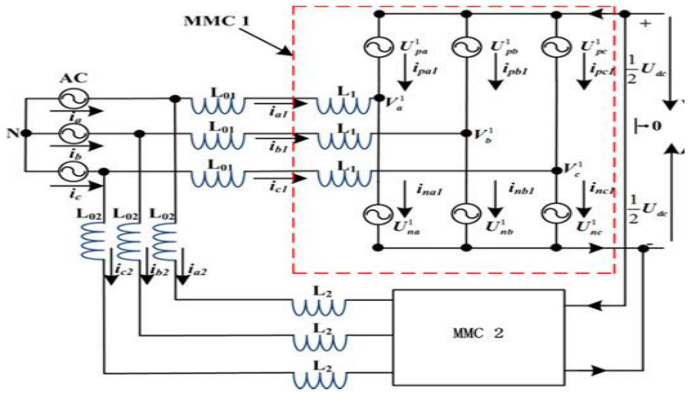

Fig. 7. Equivalent simplified circuit model of parallel-MMCs.

IV. Experimental Work

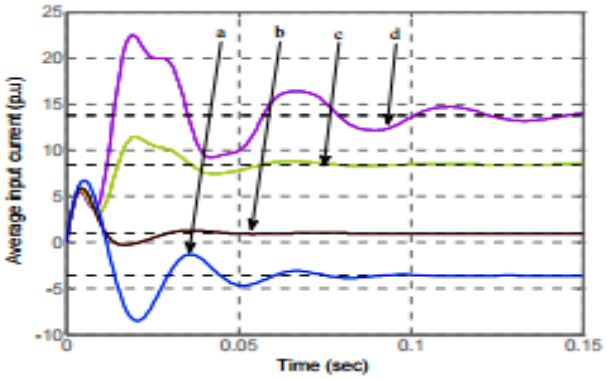

Figure 8. Step response of the average input current (p.u) for two parallel-connected inverters with null grid resistance and different values of line resistance: Ω 0.05– , d Ω 0.1– , c Ω 0.2– , b Ω 0.5–a

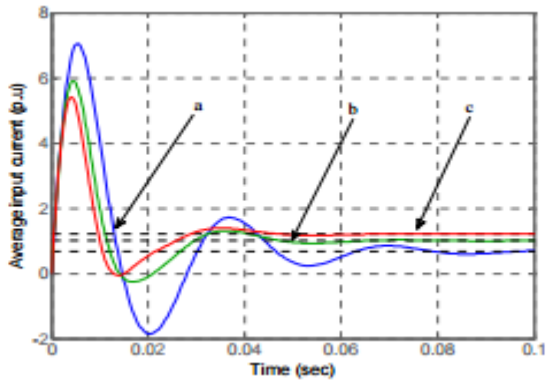

Figure 5. Step response of the input current (p.u) for a given number of parallel-connected inverters: n =1; b- n=2 and c- n=3.

V. Conclusion

This paper presents the control methods of parallel-connected MMCs under both normal and switch fault-tolerant operation conditions. In order to reduce the calculation burden meanwhile increase the control accuracy of the internal circulating current suppression method; the resonant controllers are assumed in the synchronous reference frame to suppress the dominant second and fourth-order circulating

current harmonics, and a sixth-order resonant controller is employed to suppress the zero-sequence internal circulating current. In addition, when the capacitor voltages are balanced as expected by using the voltage balancing control method, the external ZSCC can then be precisely controlled by treating the MMC as a simple two-level converter. This paper also proposes the fault-tolerant operation schemes as the switch in an SM suffers the open- or short-circuit failure. In principle, the fault-tolerant operation schemes will not influence the output quality by either adjusting the corresponding PWM schemes or the closed-loop control method. MATLAB simulations and the constructed experimental prototype verified the performance of proposed control method.

REFERENCES

[1] R. Marquardt and A. Lesnicar, "A new modular voltage source invertertopology," in Proc. Eur. Power Electron. Conf., 2003, pp. 2–4.

[2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. IEEE PowerTech. Conf., 2003, vol. 3, pp. 1–6.

[3] R. Marquardt, "Modular multilevel converter: An universal concept forHVDC-networks and extended DC-bus-applications," in Proc. Int. PowerElectron. Conf., 2010, pp. 502–507.

[4] E. Solas, G. Abad, J. A. Barrena, A. Carcar, and S. Aurtenetxea, "Modulation of modular multilevel converter for HVDC application," in Proc.14th Int. Power Electron. Motion Control Conf., 2010, pp. T2-84–T2-89.

[5] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Amir, J. Vannier, andM. Molinas, "An energy-based controller for HVDC modular multilevelconverter in decoupled double synchronous reference frame for voltage oscillations reduction," IEEE Trans. Ind. Electron., vol. 60, no. 6, pp. 2360–2371, Jun. 2013.

[6] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltagedrives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec.2007.

[7] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of atransformerless cascade PWM STATCOM with star configuration,"IEEE Trans. Ind. Electron., vol. 43, no. 4, pp. 1041–1049, Jul./Aug.2007.

[8] X. S. Wang, Z. M. Zhao, and L. Q. Yuan, "Current sharing of IGBT modules in parallel with thermal imbalance," in Proc. IEEE Energy Convers.Congr. Expo., 2010, pp. 2101–2108.

[9] Z. Ye, D. Boroyevich, J. Y. Choi, and F. C. Lee, "Control of circulatingcurrent in two parallel three-phase boost rectifiers," IEEE Trans. PowerElectron., vol. 17, no. 5, pp. 609–615, Sep. 2002.

[10] S. K. Mazumder, "A novel discrete control strategy for independent stabilization of parallel three-phase boost converters by combining spacevector modulation with variable-structure control," IEEE Trans. PowerElectron., vol. 18, no. 4, pp. 1070–1083, Jul. 2003.

[11] G.-T. Pan and Y.-H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," IEEE Trans. Ind.Electron., vol. 54, no. 2, pp. 825–838, Apr. 2007.

[12] C. T. Pan and Y. H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," IEEE Trans. Ind.Electron., vol. 54, no. 2, pp. 825–838, Apr. 2007.

[13] C. T. Pan and Y. H. Liao, "Modeling and control of circulating currents for parallel three-phase boost rectifiers with different load sharing," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2776–2785, Jul.2008.

[14] X. Sun, Y. Lee, and D. Xu, "Modeling, analysis, and implementation ofparallel multi-inverter systems with instantaneous average current sharingscheme," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 844–856, May2003.

[15] T. Chen, "Zero-sequence circulating current reduction method for parallelHEPWM inverters between ac bus and dc bus," IEEE Trans. Ind. Electron.,vol. 59, no. 1, pp. 290–300, Jan. 2012.

[16] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation andcirculating current suppression for modular multilevel converters," IEEETrans. Power Del., vol. 26, no. 3, pp. 2009–2017, 2011.

[17] K. Ilves, A. Antonopoulos, L. Har Nefors, S. Norra, and H. P. Nee,"Circulating current control in modular multilevel converters with fundamental switching frequency," in Proc. IEEE Power Electron. MotionControl Conf., 2012, pp. 249–256.

[18] S. Xu and A. Huang, "Circulating current control of double-star choppercell modular multilevel converter for HVDC system," in Proc. IEEE Ind.Electron. Soc., 2012, pp. 1234–1239.