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Power Reduction in Logic Circuits using Power Gating in Deep Submicron Circuits

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ABSTRACT

The increase in sub-threshold leakage current due to voltage scaling presents a significant challenge in CMOS integrated circuit design, as it results in higher power consumption. The majority of power consumption comes from leakage power dissipation, which is growing exponentially in integrated devices. Therefore, reducing leakage power is crucial for low-power applications. This paper presents a logic circuitry design with low area and low power by proposing a new power gated sleep technique called "Novel Dual Stack using Transmission Gates" and comparing it with existing techniques. The proposed power gated sleep circuit combines stacked sleep transistors, offering several benefits such as reduced power supply fluctuations during sleep mode and achieving the same effect as high threshold devices with normal threshold devices.

The proposed technique is simulated and compared to existing architectures using DSCH for schematic design and Microwind for layout and power simulation.

KEY WORDS: sub-threshold leakage, leakage power, DSCH, and Microwind.

1.INTRODUCTION

CMOS circuits aim to reduce power consumption while improving performance and density. However, with the reduction in characteristic size and supply voltage, the sub-threshold leakage current increases, leading to undesirable power consumption. To control power consumption, the supply voltage (VDD) is reduced while maintaining the threshold voltage (Vth) to ensure high current drive and performance. Voltage scaling leads to an increase in sub-threshold leakage current.

To reduce power dissipation, it is essential to develop methods for reducing power consumption in transistors that determine power utilization in a CMOS circuit. The power consumption in a CMOS circuit is mainly dynamic, which includes power sources scattering (Pdyn) and dynamic scattering (Psc), and static scattering (Pstatic).

The dynamic scattering in a CMOS circuit during signal transmission from 1 to 0 and from 0 to 1 is due to both systems of CMOS circuit (i.e., PMOS and NMOS) being on for some time. It leads to power dissipation Psc, which is given by the equation:

$$Psc = Isc * Vdd * ts * fsw$$

whereIsc is the short-circuit current, ts is the switching delay, and fsw is the dynamic switching frequency.

Static scattering is due to leakage current that flows when the inputs and output states are changing their state. It comprises sub-threshold leakage, channel intersection leakage, and gate leakage. The static scattering is of small magnitude and is given by:

Pleak = Ileak * Vdd

whereIleak is the leakage current.

The total dynamic power consumption in a CMOS circuit is given by the equation:

Pdynamic = K * C * Vdd^2 * fsw

where K is the technology factor, C is the switching capacitive nodes, Vdd is the supply voltage, and fsw is the dynamic switching frequency.

The expression for the total power consumption in a CMOS circuit is as follows:

Ptotal = Pdynamic + Pstatic + Psc

Flip-flops are primary building blocks in digital devices and are widely used in computational logic circuits. They store the logical state of input signals in response to a clock pulse. To achieve low area and low power, various D-flip-flops have been designed and compared based on performance metrics such as power, area, and delay. The proposed method is presented in a paper.

2. Parameters for Power Gating

To ensure successful implementation of power gating, several parameters need to be carefully considered and chosen. Timing closure implementation also requires additional considerations when it comes to power gating. The parameters that need to be considered, along with their values, include:

2.1 Power gate size
2.2 Gate control slew rate
2.3 Simultaneous switching capacitance
2.4 Power gate leakage

2.1 Power gate size

When choosing the size of a power gate, the most important factor to consider is its ability to handle the amount of current switching at any given time. The gate should be large enough to prevent any significant voltage drop (IR) due to the gate. As a general rule, the gate size should be around three times that of the switching capacitance. Designers can choose between pull-up gates (P-MOS) or pull-down gates (N-MOS), with pull-down gates typically being smaller for the same switching current.

Accurate measurement of the switching current can be achieved using analysis tools for dynamic power, which can then predict the appropriate size for the power gate. By carefully selecting the size of the power gate, designers can ensure that it effectively addresses the power consumption requirements of the system.

2.2 Gate control slew rate

The gate control slew rate is a crucial factor in determining the efficiency of power gating. If the slew rate is too large, it can significantly increase the switching time for turning the circuit on or off, which can negatively impact the power gating efficiency. To control the slew rate, designers often buffer the gate control signal to achieve the desired speed and optimize power consumption.

2.3 Simultaneous switching capacitance

Simultaneous switching capacitance is a significant factor that determines the amount of the circuit that can be switched at the same time without compromising network integrity. If a large portion of the circuit is switched simultaneously, it can lead to a rush current that can compromise the power network's integrity. To prevent this, the circuit must be switched in stages.

2.4 Power gate leakage

To achieve maximum power savings, it is important to consider reducing leakage in power gates as they are composed of active transistors.

3. Existing Techniques for Reducing Current Leakage

There are several techniques available to reduce current leakage, but each method has its own limitations. In this paper, we compare our proposed strategy with previous circuit methods such as Sleep, Stack, and Dual Stack techniques for reducing sub-threshold current leakage.

The comparison is done based on their area and power consumption.Previous techniques are as follows:

3.1 SleepTechnique

3.2 Stack Technique

3.3 Dual stack Technique

3.1 SleepTechnique

The most commonly used technique for reducing leakage power in a circuit is to incorporate sleep transistors. To implement this technique, a sleep pMOS transistor is placed between the pull-up system and Vdd, while a sleep nMOS transistor is placed between the pull-down system and ground, as illustrated in Figure 1. When the circuit is active, the sleep transistors are turned on, and they are turned off when the circuit is idle. By cutting off the power supply, this technique can effectively reduce the leakage power.

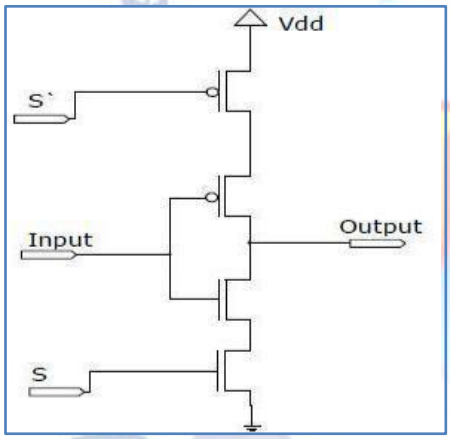

Figure 1: Sleep Circuit

3.2 Stack Technique

The stack approach is a method used to reduce leakage power in transistors. This technique involves dividing a single transistor into two transistors, creating a stack effect. However, this can increase delay significantly and may limit the effectiveness of this approach, as depicted in Figure 2.

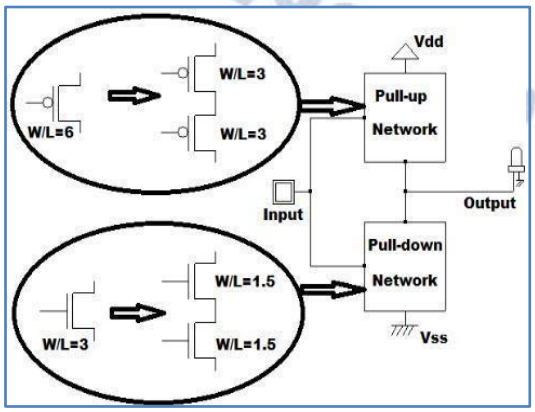

Figure 2: Stack Circuit

3.3 Dual stack Technique

The technique of using stacked sleep transistors involves using two stacked sleep transistors in Vdd and two stacked sleep transistors in ground, as illustrated in Figure 3. This approach achieves leakage reduction in two ways: firstly, due to the stack effect of the sleep transistors, and secondly, due to the sleep transistor effect. Since pmos transistors are not efficient in passing ground and nmos transistors are not efficient in passing Vdd, the stacked sleep technique uses a pmos transistor in ground and an nmos transistor in Vdd during sleep mode to maintain the logic state. To maintain the logic state during sleep mode, two additional transistors are designed.

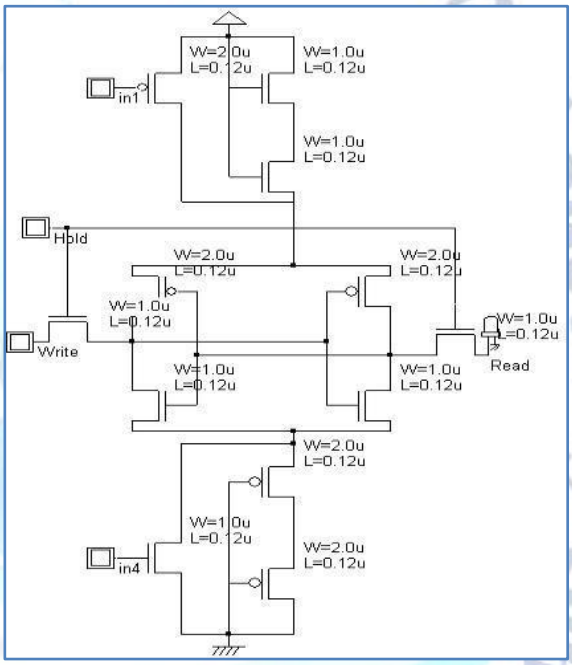

Figure 3: Dual stack Circuit

4. PROPOSED LEAKAGE CURRENT REDUCTION TECHNIQUE

The Proposed power gating technique is as shown in figure 4.The Proposed Sleep Circuit has three modes of operation: Active mode, Standby mode, and Sleep to Active mode transition. In Active mode, the transistor sleep signal is set to logic 1, and both sleep transistors M2 and M1 remain ON. This results in very low resistance, and the VGND node potential is pulled down to ground potential, making the logic difference between the logic circuit and virtual ground (VGND) node potential approximately equal to the supply voltage.

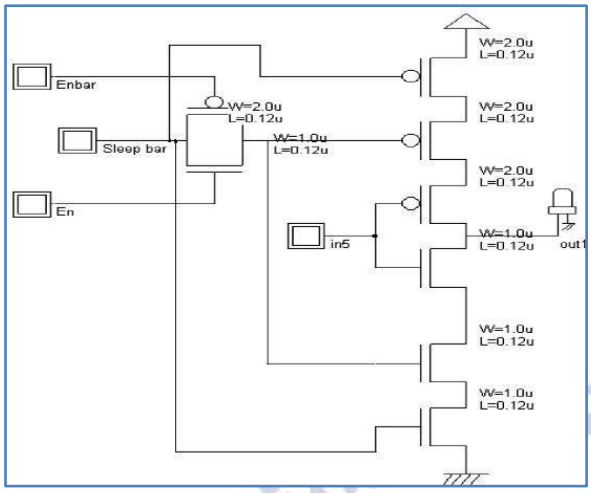

Figure 4: Circuit chart of proposed method

Combining stacked sleep transistors offers several benefits. First, the magnitude of power supply fluctuations during sleep mode transitions is reduced because the transition is gradual. Second, using a stacked sleep structure with a normal threshold device achieves the same effect as using a high threshold device in conventional power gating techniques to minimize leakage.

In Active mode, the sleep signal to the transistor is set to logic 1, and both NMOS1 and NMOS2 remain ON. When the control transistor is turned OFF by giving logic 0, both transistors offer very low resistance, pulling the VGND node potential down to ground potential. This reduces leakage current through the stacking effect, which turns off transistors NMOS1 and NMOS2, and vice versa for the header switch.

When there is a positive potential at the intermediate node, several effects occur. First, the gate-to-source voltage for NMOS1 becomes negative. Second, the negative body-to-source potential (Vdsl) for NMOS1 decreases, resulting in less drain-induced barrier lowering.Third, the drain-to-source potential (VdNMOS2) for NMOS2 is less than that for NMOS1 because most of the voltage drops across NMOS1 in sleep mode. As a result, drain barrier lowering is significantly reduced.

Sleep mode occurs when the circuit switches from sleep to active mode and vice versa. In the first stage, the sleep transistor (NMOS1) works as a diode on the control transistor MI, which is connected across the drain and gate of the sleep transistor. Due to the quadratic drop in the drain-to-source current of the sleep transistor, this reduces voltage fluctuations on the ground and power net and reduces the circuit wakeup time.

During sleep to active mode switching, the transistor NMOS1 is turned on initially, and after a small duration of time, NMOS2 is turned on to reduce the GBN. The control transistor in the second stage is off, allowing the sleep transistor to work normally. During sleep to active mode switching, the transistor NMOS1 is turned on first, and then NMOS2 is turned on after a short duration of time. Isolation is done for the logic circuit and the ground for a short duration as NMOS2 transistor is turned off. In this duration, the reduction of GBN can be greatly controlled by the intermediate node VGND2 voltage and operating the transistor NMOS2 in triode region.

The intermediate node voltage (VGND2) can be controlled by inserting a proper amount of delay that is less than the discharging time of the NMOS1 transistor and with proper selection of capacitance C2. Leakage current is reduced by the stacking effect, turning both NMOS1 and NMOS2 sleep transistors OFF. This raises VGND2, the intermediate node voltage, to positive values due to a small drain current. The positive potential at the intermediate node has several effects, as mentioned earlier.

5. Area and Power Analysis

We utilized DSCH software to perform logic design. Using primitives, we constructed a hierarchical circuit, which was then simulated. At the layout level, we utilized Micro Wind, a tool that enabled us to design and simulate circuits. The program offers a range of editing features such as copy, cut, paste, duplicate, and move, as well as different views such as MOS characteristics, 2D cross section, and 3D process viewer, along with an analog simulator. With Microwind, we were able to design and simulate an integrated circuit at the physical description level. The Experimental Methodology is depicted in Figure 5.

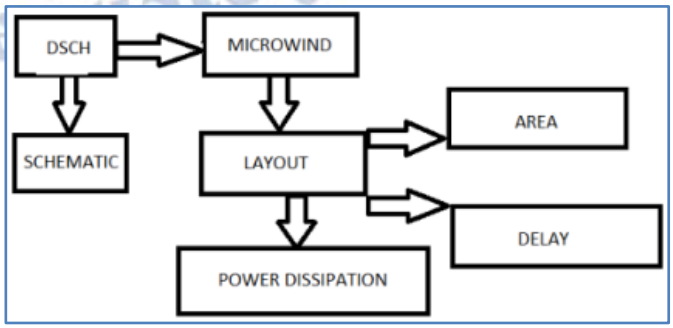

Figure 5: Experimental Methodology

Based on the schematic design created using DSCH, the circuit is evaluated through testing. Afterwards, Verilog code is generated in DSCH and then compiled in Microwind. The paper aims to estimate the power dissipation for four different design techniques.

5.1 Simple Flipflop

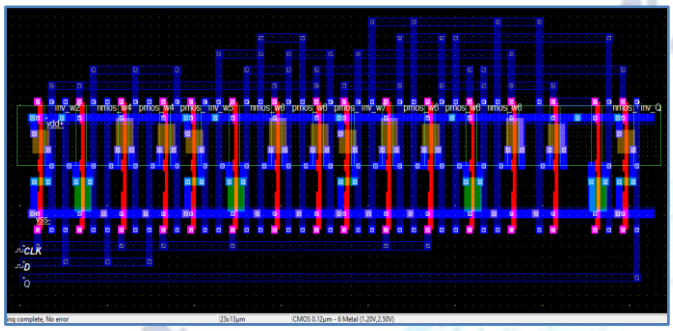

Figure 6: Simple flip flop circuit Layout

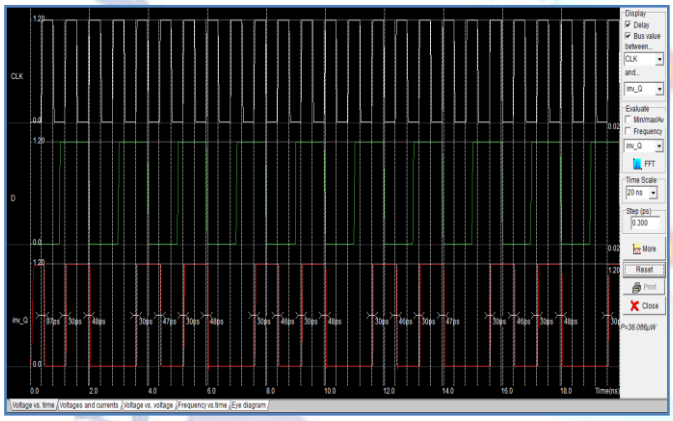

Figure 7: Simple flip flop circuit Power analysis

5.2 Stack Technique

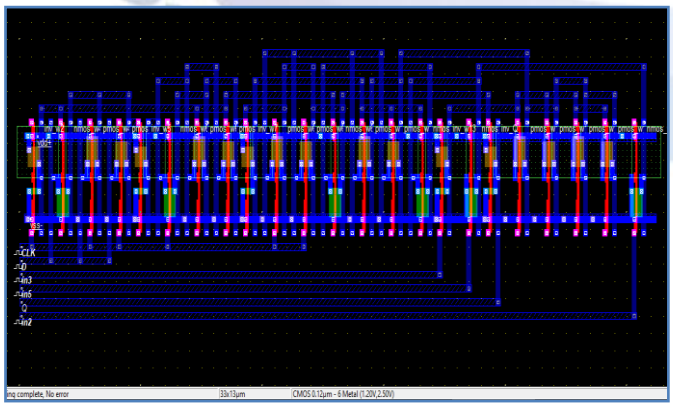

Figure 8: Stack technique Layout

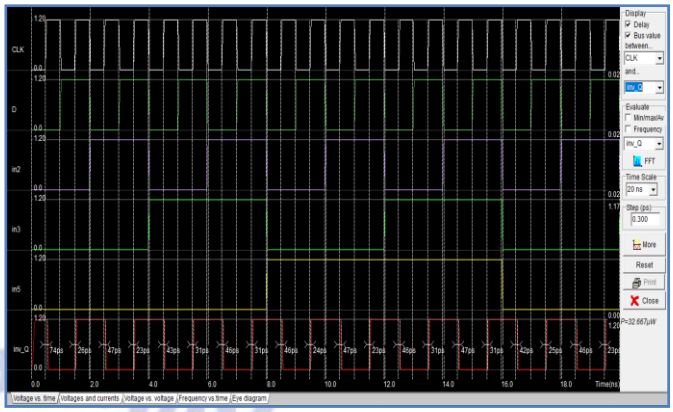

Figure 9: Stack Technique Power Analysis

5.3 Dual Stack Technique

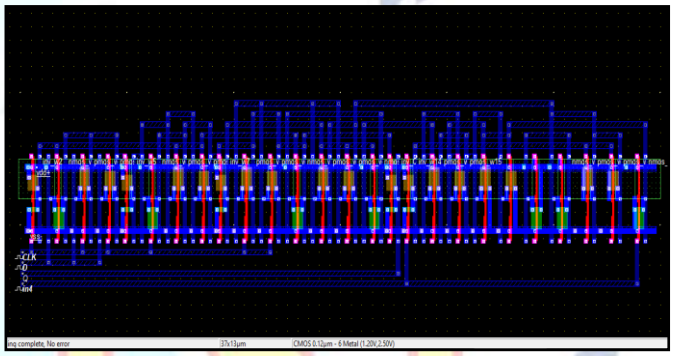

Figure 10: Dual Stack technique Layout

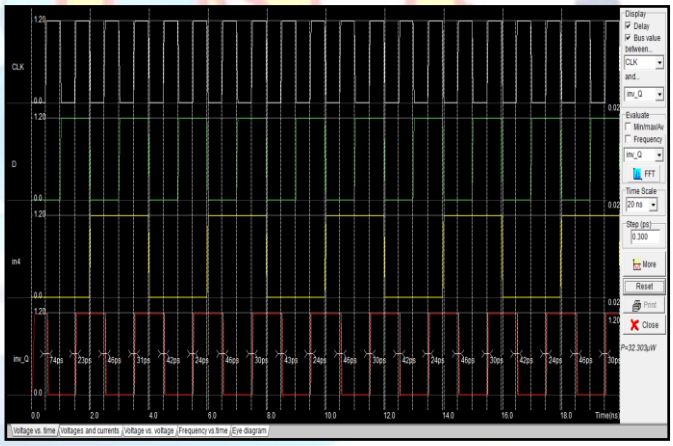

Figure 11: Dual Stack Technique Power Analysis

5.4 Proposed Technique

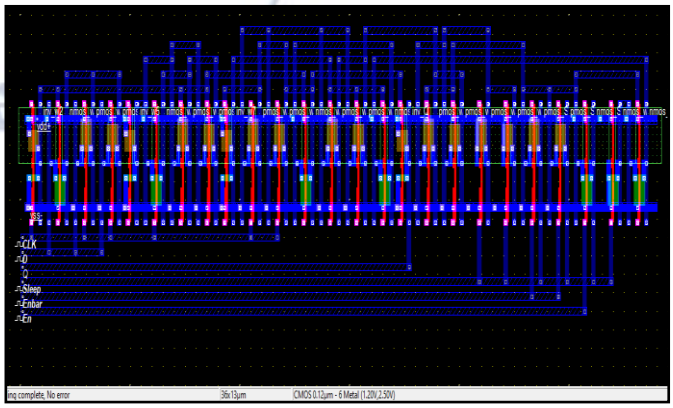

Figure 12: Proposed technique Layout

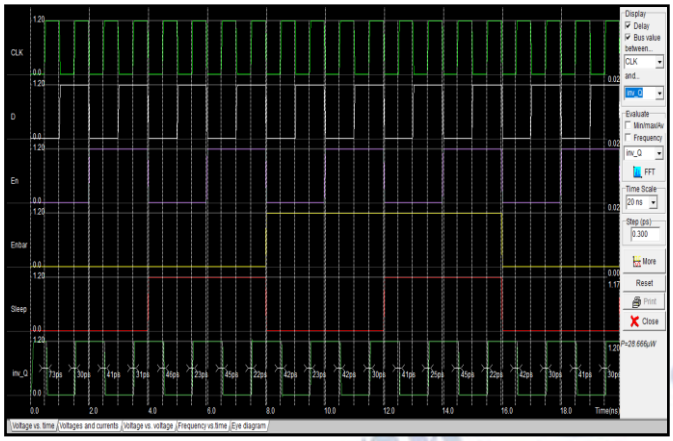

Figure 13: Proposed Technique Power Analysis.

S.No	Method	Area	Power
1	Simple Flip-flop	23x13 µm	36.086 µW
2	Stack Technique	33x13 µm	32.667 µW
3	Dual Stack Technique	37x13 µm	32.303 µW
4	Proposed Technique	36x13 µm	28.666 µW

Table 1: Power & Area Analysis of Flip Flop in Different Power Gating Methods

6. Conclusion

Reducing subthreshold leakage power consumption in CMOS technology presents a significant challenge, and while there are several effective techniques available, no perfect solution has been identified. Consequently, designers select techniques based on their design criteria and technology. This paper proposes a new circuit structure for dual stack, which offers a new solution to the designer's static and dynamic power consumption concerns. Unlike the sleep transistor technique, the dual stack technique maintains the original state while delivering ultra-low leakage power consumption. Additionally, the dual stack approach has the least speed power product compared to other methods, making it an excellent choice for designers who prioritize power efficiency over speed. Overall, the dual stack technique has promising applications for future integrated circuits, particularly for area and power efficiency.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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