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# A HDL Based Synthesis of Combinational Circuit Using Reversible Design

**Dr. P. Sreenivasulu | P. Baby Aparna | Sk. Nayima Kousar | V. Anitha | N. Srivallika**

Department of ECE, Narayana Engineering College, Gudur, AP, India

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## ABSTRACT

***Reversible logic allows the system to be run both forward and backward. This means that reversible computations are able to generate inputs from outputs and can be interrupted and reversed at any moment. In VLSI design, energy dissipation is a key factor. The first time reversible logic was connected to energy was when Landauer stated that information loss due to function leads to irreversible energy loss. Many possible new technologies, such as quantum computing, low power/area, and encoder/decoder devices, depend on reversible circuits as their base. The scalable synthesis of such circuits has gained significant attention in recent years. A combinational circuit is a digital logic circuit in which the output is dependent on the current combination of inputs irrespective of their previous states. The digital logic gate is a fundamental component of combination circuits***

***KEYWORDS: Combinational Circuit,Reversible gates.***

## INTRODUCTION

VLSI design is focused on low power design. For low power VLSI design, reversible logic circuit is one of the approaches receiving the most attention from researchers. Using reversible logic gates, this technique achieves logical reversibility [1]. In VLSI design, energy dissipation is a crucial factor. Landauer was the first to relate reversible logic to energy when he stated that information loss owing to function irreversibility results in energy dissiption. Bennett further supports this principle by stating that zero energy dissipation is only possible when the circuit has reversible gates. When the input vector cannot be uniquely recovered from its output vectors, information is lost [2]. In a reversible logic, each input vector can be uniquely reconstructed from its output vectors, therefore no information is lost and reversible logic circuits are highly immune to overheating. According to [2], zero energy dissipation is only achievable if the network's gates are reversible. Hence, reversibility will become an important element in the futuredesign of circuits. Reversible circuits are especially intriguing since information loss implies energy loss [2].

The ability of reversible logic gates to reduce power dissipation is the primary need for low power VLSI architecture. It has numerous applications in low-power CMOS and optical information processing, DNA computing, quantum computing, and nanotechnology. As long as a system supports the reproduction of I nputs from observable outputs, energy will not be lost from the

system. Reversible logic enables the system to be executed both forwards and backwards. This implies that reversible computations can produce inputs from outputs and can stop and reverse at any time in the history of the computation. A circuit is reversible if the input vector can be uniquely inferred from the output vector and there is a onetoone correlation between its input and output assignments. Reversible Gates are circuits in which the number of outputs is equal to the number of inputs and the vector of inputs and outputs have a one-to-one correspondence [3]. Not only does it help us determine the outputs from the inputs, but it also helps us recover the inputs from the outputs in a unique manner [3].

## REVERSIBLE LOGIC GATES

Reversible computing reduces the complexity of digital circuits by employing reversible Reversible computing reduces the complexity of digital circuits by employing reversible processes. A function is deemed reversible if it satisfies two conditions: 1) It must have an equal number of inputs and outputs; and 2) It must be able to be reversed. ii) Each input must relate to a unique output. Some many sorts of research introduce many forms of reversible logic gates. These gates are used to create sequential and combinational circuits [4]. There is a one-to-one mapping between the number of inputs and the number of outputs in a reversible circuit architecture. With a reversible circuit, time slices are discrete and the depth is the sum of all time slices. In addition, it has no fan-out [5]. They are many gates Present in the Reversible Logic, but mainly few gates are important these gates are also called as Universal gates. They are

1) NOT Gate
2) Feynman Gate
3) Fredkin Gate

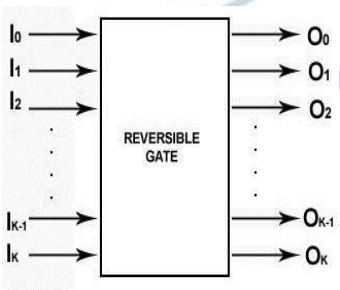
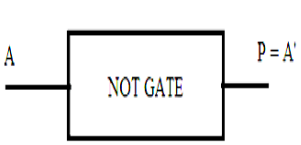



Fig. 1. Reversible Logic

**A.NOT Gate:**

A NOT gate is the only Reversible Logic gate. This component is an 11 Reversible Logic Gate. NOT gate outputs are denoted as P=A′ and NOT gate quantum cost is zero [5].

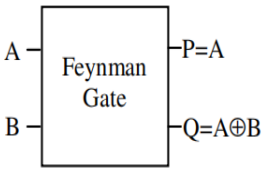



| A | P |
|---|---|
| 0 | 1 |
| 1 | 0 |

Fig. 2. NOT Gate

**B. Feynman Gate:**

I (A, B) is the input vector, while O is the output vector (P, Q). The outputs are defined by the equations P=A and Q=AB. 1 is the quantum cost of a Feynman gate is 1.

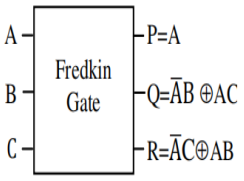



| A | B | P | R |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Fig.3. Feynman Gate

**C. Fredkin Gate:**

Fredkin Gate is a three-by-three reversible gate. Fredkin gate outputs are denoted as P=A, Q=A′B XOR AC, and R=A′C XOR AB.

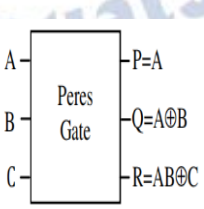



| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Fig.4.Fredkin Gate

**D. Peres Gate:**

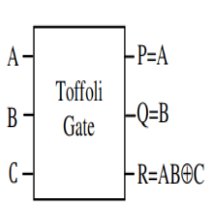
It is also called as 3X3 reversible gate. The output is defined as P = A, Q = A XOR B and R=AB XOR C.




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

Fig.4. Peres Gate

**E. Toffoli Gate:**




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

Fig.5.Toffoli Gate:

**LITERATURE SURVEY**

A. Combinational circuits implemented using Reversible Gates:

Reversible logic is an emerging academic subject in the modern period. This study aims to build many types of combinational circuits, including full-adder, full-subtractor, multiplexer, and comparator, utilizing a reversible decoder circuit with minimal quantum cost. A reversible decoder is built with minimal quantum cost utilizing Fredkin gates. Many reversible logic gates exist, including Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Feynman Gate, and many others [6]. This can be done using techniques such as Karnaugh maps, Boolean algebra, or truth tables. Once we have expressed the Boolean function in terms of reversible gates, we can then construct the corresponding circuit using the reversible gates. The resulting circuit will be reversible, meaning that it can be run backward to obtain the original inputs from the outputs. Reversible circuits have important applications in quantum computing, where the loss of information due to irreversible operations can lead to errors. By using reversible gates to implement combinational circuits, we can minimize the loss of information and improve the overall accuracy of quantum computations.

***Designing of Reversible Multiplexer***

In the Reversible Multiplexers, Fredkin Gates made a proposal. In this design, the gate count, quantum cost, and garbage outputs for several types of multiplexers are calculated [7]. In this design, reversible multiplexers are constructed using a Multiplexer-capable RMUX1 reversible logic gate. As demonstrated in Figure, a single RMUX1 Gate can function as a 2 to 1 Multiplexer. Y is the output expression of the Reversible 2x1 Multiplexer.

- Y = SI0+ SI1
- Where S = selectline
- I0,I1 = Inputs,
- Y = output

As shown in Figure, three 2x1 Reversible Multiplexers are required to create a 4x1 Reversible Multiplexer. This

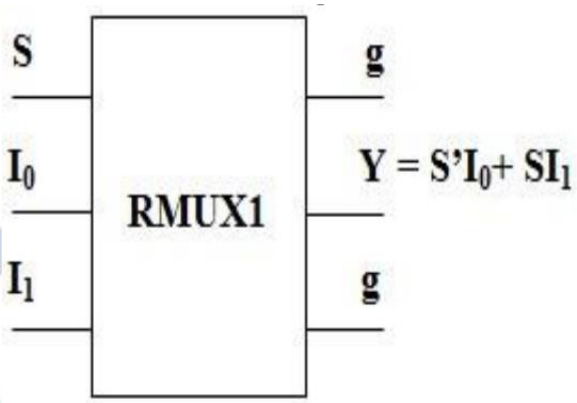



Fig. 7. Rmux1-gate-as-a-reversible-2x1-multiplexer

design has a twelve-quantum-cost and five trash outputs. Using the following equation [6], the Reversible 4x1 Multiplexer is implemented.

Y = S1S0I0 + S1S0I1 + S1S0I2 + S1S0I3 (5)

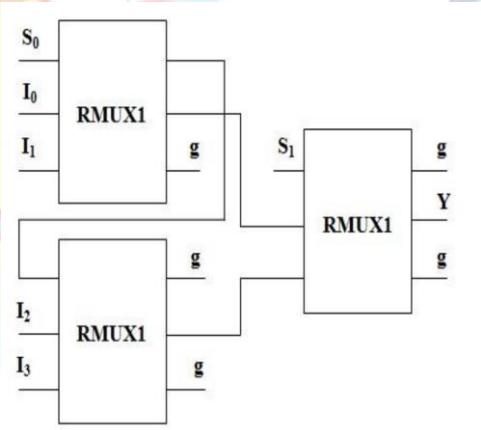



Fig. 8. Reversible-4x1-multiplexer-using-rmux1-gates

**Basic Decoder 2x4:**

The 2 to 4 Decoder has two inputs (A1 and A0) and four outputs (Y3, Y2, Y1, and Y0) [8]. The block diagram of a 2 to 4

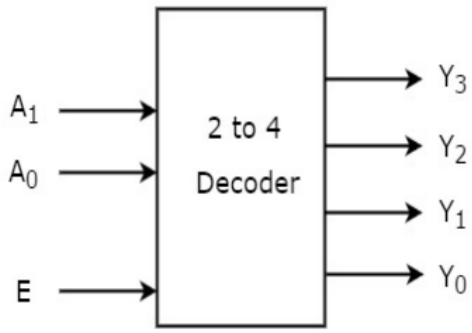



Fig. 9. Block-diagram-for-decoder-2-to-4

4 decoder is represented in the image below. When enable, E s "1", one of these four outputs will be "1" for each combination of inputs. The decoder for the Truth table of 2 to 4 is shown in table. Using the Truth table, we may derive the Boolean functions for each output, as each output has a product term. Hence, there are a total of four product terms. These four product terms can be implemented using four AND gates with three inputs each and two inverters. Figure depicts the circuit diagram of a 2-to-4 decoder. Hence, the outputs of a 2-to-4 decoder are the minimum of two input variables A1 and A0, and when enabled, E equals one. If enable, E is equal to zero, then all decoder outputs will equal zero. Similar to the 3 to 8 decoder, the 4 to 16 decoder outputs sixteen min terms for the four input variables A3, A2, A1, and A0.

| Enable | Inputs | | Outputs | | | |
|---|---|---|---|---|---|---|
| E | $A_1$ | $A_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | x | x | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

Fig. 10. Truth-table-for-decoder-2-to-4

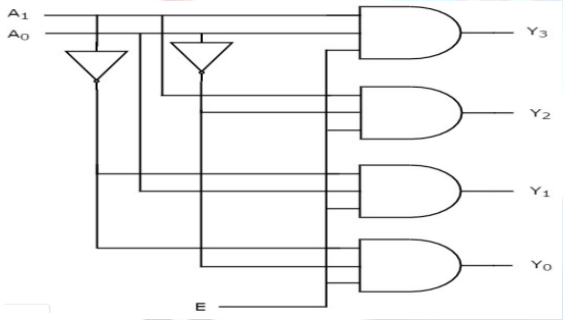



Fig. 11. Logic-diagram-for-decoder-2-to-4

***Designing of Reversible Encoder:***

This depicts the proposed 4:2 Reversible Encoder. It consists of three Feynman gates (FG) and one Fredkin gate (FG) (FRG). It features four inputs A,B,C,D, two outputs Y1 and Y2, and two garbage outputs g1 and g2. The circuit's operation is detailed in Table [9]. Reversible decoder is designed using

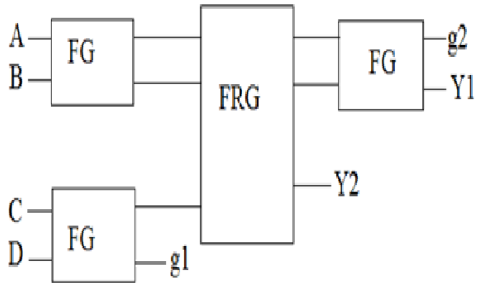



Fig. 12. Reversible-encoder

Fredkin gates with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and many more.

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| A | B | C | D | Y1 | Y2 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |

Fig. 13. Truth-reversible-encoder

***Designing of Reversible Comparator:***

A reversible comparator is an electronic device used to compare two input signals and determine which one is greater or whether they are equal. It is called "reversible" because it can also determine which input is smaller by simply reversing the polarity of the inputs. A reversible comparator typically has two input terminals and one output terminal. The inputs are compared and the output will be either high or low depending on which input is greater. If the inputs are equal, the output will be in an undefined state. In addition to comparing the inputs, a reversible comparator may also have other features, such as hysteresis or built-in reference voltages. Hysteresis is a technique used to provide a stable output even when the input signals are noisy or fluctuating. Built-in reference voltages can simplify the design by providing a stable reference against which to compare the inputs. Reversible comparators are commonly used in applications such as voltage monitoring, threshold detection, and analog-to-digital conversion. They are wide The proposed BJSS gate can

be used as an AL-bit comparator to detect if A equals B (AEB (A = B)), A is less than B (ALB (A B), or A is larger than B (AGB (A ¿ B)). The truth table for the I-bit comparator is shown [10]. As inputs A and B, this logic gate receives I-bit binary integers coupled with two constant inputs. Figure 1 depicts a one-bit comparator gate with three AEB, ALB, and AGB outputs and one trash output [10]

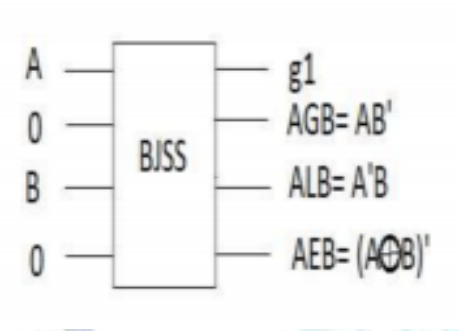



Fig. 14. Bit-comparator

***Designing of Reversible Full-Adder:***

Fredkin gates cannot form a complete set on their own. Fredkin gates are controlled SWAP gates whose number of ones does not change. We can create a tiny reversible fulladder by combining Fredkin, Toffoli gates with controlled NOT gates. By mixing an endless number of Toffoli gates, any boolean function with an infinite number of inputs can be implemented using the Toffoli gate. Toffoli gate and Fredkin gate are known as universal reversible gates due to their crucial universally primal attribute.

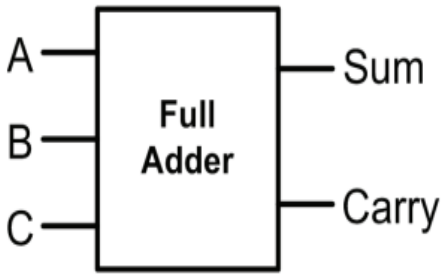



Fig. 15. Conventional-full-adder

In addition to using inputs and their complements, reversible logic also produces outputs and their complements. This paper just displays inputs and outputs to avoid complexity [11]. Avoiding the complements of inputs and outputs. For a full adder as depicted in Fig, the Sum and Carry expressions are

Sum = ABC and Carry = ABC.

Carry = C(AB)plus(AB).

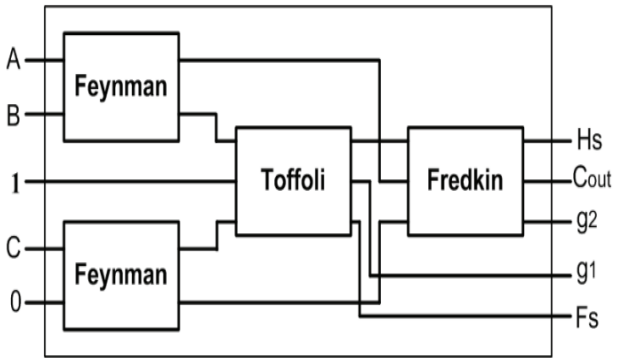



Fig. 16. Architecture-of-proposed-full-adder

The realization of the topology takes only 48 transistors. Moreover, the proposed architecture produces the Sum expression of the half-adder. Hence, the suggested architecture can function as both a full adder and a half adder. A reversible full adder is a circuit that performs addition of two bits in a reversible manner. Reversible computing is a type of computing that allows the computation to be run backwards, so that the original inputs can be recovered from the outputs.

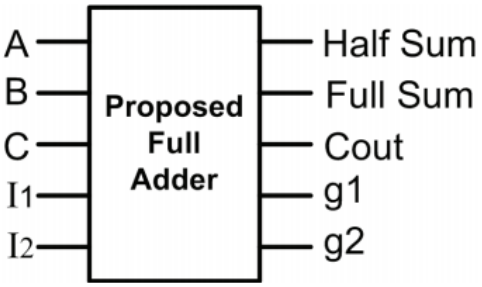



Fig. 17. Symbol-of-proposed-full-adder

**EXISTING SYSTEM**

Various proposals are given for the design of combinational circuits in ongoing research. In existing method some combinational circuits like Full adder, multiplexer, comparator are designed using various methods. One of the outgoing research in VLSI Design Implemented all the Combinational Circuits using CMOS gates and some researches in VLSI design implemented using irreversible method. Ripple carry adder, Full adder, Full Subtractor, Half adder, Half

subtractor circuits are existing in Reversible method by using the Reversible gates.

## PROPOSED SYSTEM

This proposed system for HDL based synthesis of combinational circuits using reversible design involves specifying the required functionality, designing the circuit using reversible logic gates, performing high-level synthesis, optimizing the circuit, simulating the circuit, and verifying the design. This system can lead to the development of efficient and power efficient reversible circuits.

- TO Overcome the problems, present in the Existing system, here we introduced the Reversible logic method.
- The Problem Present in the CMOS Method i.e., using a greater number of gates, so that the complexity of the system will increase and also power dissipation is more.
- The Problem Present in the irreversible method is the no. of input bits are lost once the logic block generates the output and input bits cannot be restored.
- "In Proposed method all the problems can be solved because of inputs and outputs have a one-to-one mapping and also power dissipation and complexity will be reduced".

### A.Proposed Block Diagram

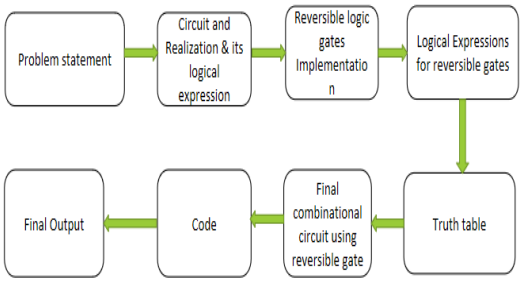



Fig.18.Block Diagram

### B. Introduction to Full Adder

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. we use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results.

Software tool

There are mainly two software tools are used in this project .They are

- SyReC
- Xilinx 14.1 version

Programming Language

- For SyReC, Python Programming Language is used
- For Xilinx, VHDL Language is used

## SIMULATION RESULTS

A full adder is a digital circuit that performs addition of three binary digits: A, B, and C-in (where C-in is the carry-in from a previous addition). The circuit produces a sum output (S) and a carry output (C-out) which is used as the carry-in for the next addition. Reversible logic is a type of logic gate operation where the inputs and outputs can be reversed without any loss of information, meaning the operation is reversible. One commonly used reversible gate is the Peres Gate, which has three inputs and three outputs.

**final Circuit**

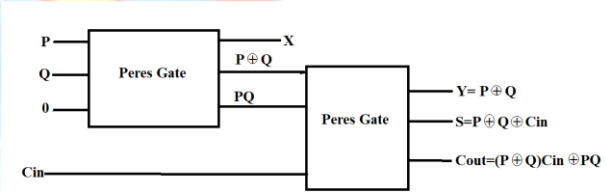



Fig. 19. Final circuit

**Simulation Outputs**

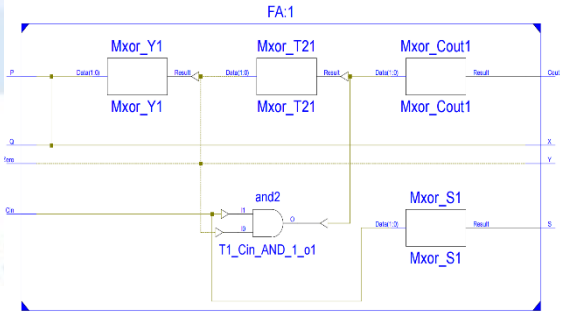



Fig.20.Full adder RTL

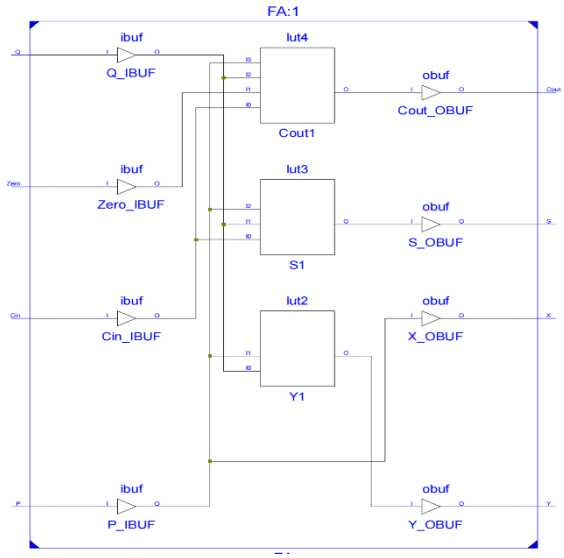



Fig. 21. Full Adder Schematic

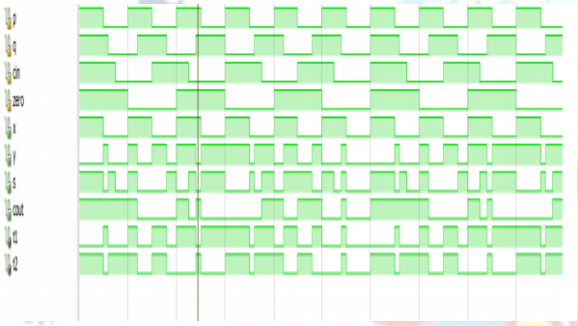


Fig. 22. Full Adder Graph

• These are all helps to reduce the Power Dissipation in the VLSI circuits and its size which are compared with the help of existing system.

•The Final Result of this project is to reduce the Number of Gates, quantum cost ,circuit Complexity, Garbage outputs .

| | Existing system [1] | Existing system [2] | Proposed system |
|---|---|---|---|
| No.Of Gates used | 3 | 3 | 2 |
| Quantum cost | 10 | 9 | 8 |
| Garbage Outputs | 4 | 5 | 2 |

Fig. 23. Comparision Table

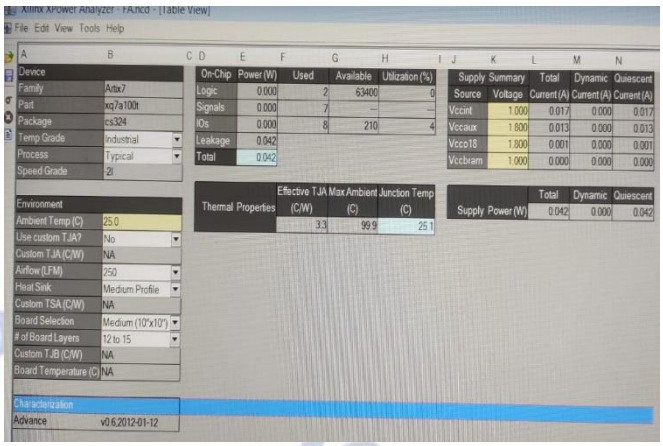


Fig. 24. Power Output

## CONCLUSION

We've made it easier to understand Multipurpose binary reversible gates by giving a way to think about them. With more straightforward electronic circuits, these gates can be utilised to absorb Boolean functions. In a similar fashion, there is a possible approach to construct multi-valued reversible gates, and these gates share comparable features. The asynchronous design that was suggested. There are applications in digital circuits like timers and counters; this is the work that goes into constructing reversible ALUs and processors, among other things. An essential part of the process of constructing a lengthy and intricate reversible sequential circuit

## FUTURE WORK

In future, by using these gates, a designer can design any of these combinational circuits with numerous advantages over conventional gates such as, low power, low complexity, less delay, high speed etc. Reversible computing has become a new emerging area for researchers in recent years in fields like Quantum Computing, Nanotechnology, Low Power CMOS

## Conflict of interest statement

Authors declare that they do not have any conflict of interest.

## REFERENCES

[1] Varvadekar, J. Convolutional Encoder using Reversible Logic Circuits.

[2] Ali, M. B., Hossin, M. M., Ullah, M. E. (2011). Design of reversible sequential circuit using reversible logic

synthesis. International Journal of VLSI Design and Communication Systems, 2(4), 37.

[3] Mamataj, S., Das, B., Saha, D., Banu, N., Banerjee, G., Das, S. (2014). Designing of efficient adders by using a novel reversible SDNG gate. International Journal of Computer Science Issues (IJCSI), 11(3), 51.

[4] Swathi, M., Rudra, B. (2021, January). Implementation of reversible logic gates with quantum gates. In 2021 IEEE 11th annual computing and communication workshop and conference (CCWC) (pp. 1557-1563). IEEE.

[5] Gaikwad, A., Patil, S. (2019). Design and implementation of combinational circuits using reversible gates. International Research Journal of Engineering and Technology (IRJET), 6(03).

[6] Naguboina, G. C., Anusudha, K. (2017, January). Design and synthesis of combinational circuits using reversible decoder in Xilinx. In 2017 International Conference on Computer, Communication and Signal Processing (ICCCSP) (pp. 1-6). IEEE.

[7] Gopal, L., Raj, N., Gopalai, A. A., Singh, A. K. (2014, November). Design of reversible multiplexer/de-multiplexer. In 2014 IEEE International Conference on Control System, Computing and Engineering (ICCSCE 2014) (pp. 416-420). IEEE.

[8] Vinod, G. V., Kumar, D. V., Ramalingeswararao, N. M. (2022). An Innovative Design of Decoder Circuit using Reversible Logic. Journal of VLSI circuits and systems, 4(01), 1-6.

[9] Kaur, S., Singh, A. (2015). Design and Performance Analysis of Encoders using Reversible logic gates. International Journal of Scientific Engineering Research, 6(6), 327-332.

[10] Vishal Nayak, V. S. P., Prasad, G., Chowdary, K. D., Chari, K. M. (2015, December). Design of compact and low power reversible comparator. In 2015 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT) (pp. 17-21). IEEE.

[11] Aditya, M., Kumar, Y. N., Vasantha, M. H. (2016, January). Reversible full/half adder with optimum power dissipation. In 2016 10th International Conference on Intelligent Systems and Control (ISCO) (pp. 1-4) IEEE