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Multi-Level Inverter for 5-Level 8-Switches

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ABSTRACT

This paper presents the design and implementation of a 5-level multilevel inverter using only 8 switches, aimed at reducing switch count while maintaining performance and power quality. Multilevel inverters are widely used in medium and high-power applications due to their ability to produce output voltages with low harmonic distortion. The proposed topology reduces circuit complexity and switching losses, making it suitable for compact and efficient power electronic converters. Simulation and experimental validation show promising results in terms of waveform quality, efficiency, and control simplicity.

KEYWORDS: Multilevel inverter, 5-level inverter, 8-switch topology, PWM, power electronics.

1. INTRODUCTION

Multilevel inverters (MLIs) play a pivotal role in the conversion of direct current (DC) to alternating current (AC), particularly in renewable energy systems. Compared to conventional inverters, MLIs offer superior output waveform quality and significantly reduced harmonic distortion, making them well-suited for applications involving solar and wind energy sources [1].

Recent advancements in MLI research have been driven by the need to optimize performance while minimizing system complexity and cost. One notable development is a 15-level inverter topology that achieves high performance using only eight switches and a single DC source, making it especially attractive for renewable energy integration [1]. Similarly, a compact 5-level inverter configuration has been proposed, employing four power switches, two diode clamps, and a single capacitor to deliver cost-effective operation compared to conventional topologies [2].

Further innovation in MLI design includes a simplified 5-level inverter developed specifically for solar energy applications, which reduces the number of switches without compromising performance [3]. Additionally, a novel 29-level MLI architecture featuring an H-bridge module and sub-switch technology has been introduced. This design not only enhances efficiency and output waveform quality but also reduces the physical size of the system, addressing key concerns in renewable energy deployment [4].

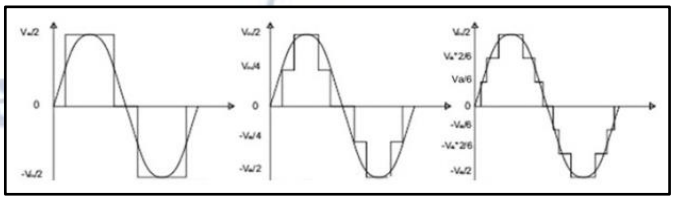

Fig. 1: 3, 5, 7 level output waveform of multilevel inverter at fundamental frequency

II. LITERATURE REVIEW

Recent advancements in multilevel inverter (MLI) technology have concentrated on minimizing the

number of components required, particularly power switches and DC sources, while ensuring the retention of desirable output characteristics such as high power quality and efficiency. Traditional MLI configurations, though effective in reducing harmonic distortion, often suffer from drawbacks including a high switch count and complex control mechanisms, which can increase both the cost and implementation difficulty [5].

To address these challenges, researchers have proposed several innovative topologies. Ramya and Vaidehi (2018) introduced a seven-level inverter design utilizing only eight switches, significantly reducing circuit complexity without sacrificing performance [6]. Similarly, Omer et al. (2018) presented a cascaded MLI configuration that incorporates fewer DC sources and switching devices. This design offers additional benefits such as lower voltage stress across switches and the introduction of redundant switching states, enhancing system reliability [7].

Gupta et al. (2016) conducted a comprehensive review of low switch count MLI topologies, emphasizing both their benefits—such as reduced cost and simplified control—and the technical challenges they present [8].

III. METHODOLOGY

The proposed inverter architecture is based on two cascaded H-bridge modules, configured to operate under a modified pulse width modulation (PWM) control strategy. This configuration enables the generation of five distinct voltage levels, while utilizing only eight power switches. The reduced component count not only simplifies the overall circuit structure but also contributes to improved reliability and lower implementation costs.

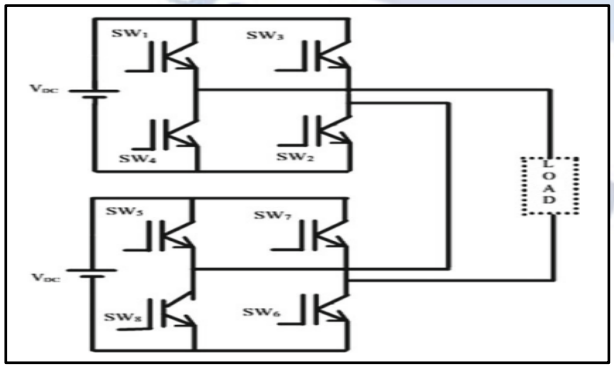

Fig. 2. Single-phase five-level multilevel inverter

A customized PWM technique is employed to optimize the switching pattern. Specifically, a level-shifted multicarrier PWM scheme is adopted and programmed into a microcontroller unit. This approach is designed to minimize the total harmonic distortion (THD) of the output waveform while ensuring efficient and balanced switching across all devices.

The inverter topology is modeled and validated using MATLAB/Simulink to analyze performance characteristics under various operating conditions. For hardware implementation, insulated-gate bipolar transistors (IGBTs) are selected due to their suitability for medium-power applications, offering fast switching and thermal robustness. Gate driver circuits are integrated to interface the microcontroller with the IGBTs, ensuring proper signal timing and electrical isolation.

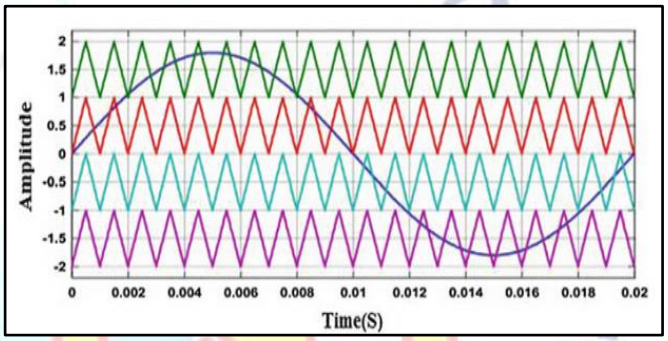

Fig. 3. Reference and carrier wave for a five-level cascaded H-bridge multilevel inverter with PD-PWM

IV. RESULTS AND DISCUSSION

The simulation and analysis of the proposed multilevel inverter confirm its effectiveness in generating an output voltage waveform that closely approximates a pure sine wave. By employing a five-level topology with appropriately modulated pulse widths, the inverter demonstrates a significant reduction in total harmonic distortion (THD). The level-shifted multicarrier PWM strategy plays a critical role in shaping the output waveform and selectively suppressing undesirable harmonics.

As the number of voltage levels increases, the %THD is observed to decrease due to the finer resolution of the synthesized waveform. This also leads to a reduction in the voltage stress (dv/dtdv/dtdv/dt) experienced by each switching device, thereby enhancing overall reliability. Furthermore, the use of multiple levels enables a lower voltage drop across individual switches, which contributes to reduced switching losses and improved inverter efficiency.

Pulse width variation has a direct influence on harmonic elimination. By precisely controlling the

duration of each voltage level, selective harmonic cancellation can be achieved. The simulation results demonstrate that optimal pulse width modulation results in a waveform with minimized distortion and high-quality power delivery, making the inverter suitable for renewable and medium-power applications.

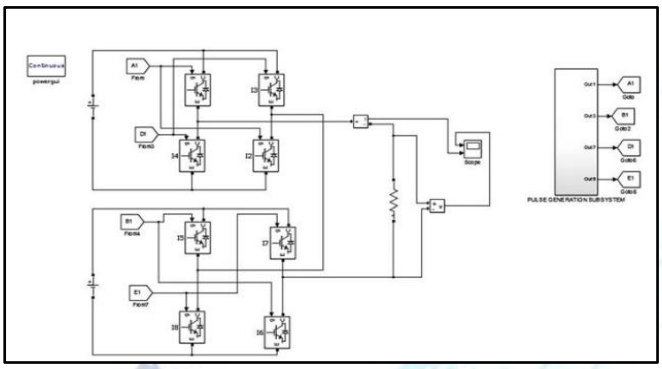

Fig. 4. Simulation diagram of cascaded H-bridge multilevel inverter using PD-PWM technique

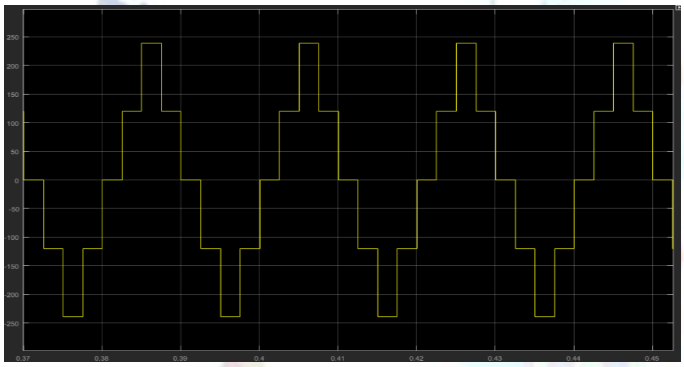

Fig. 5. Output voltage of five-level cascaded H-bridge multilevel inverter

V. CONCLUSION

The proposed multilevel inverter topology, comprising two cascaded H-bridges and eight switches, offers an efficient solution for generating high-quality AC output with reduced harmonic distortion. The use of a level-shifted PWM strategy allows for effective harmonic elimination by adjusting pulse widths, contributing to improved power quality and system efficiency.

The results indicate that increasing the number of voltage levels significantly reduces %THD and voltage stress across switches, which in turn enhances reliability and decreases power losses. The reduced voltage across individual switches also supports higher efficiency through minimized switching losses. These characteristics make the proposed design a promising candidate for renewable energy systems and medium-voltage industrial applications, where performance, efficiency, and simplicity are critical.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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