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Design of multiplier with low latency Approximate 5-2 compressor

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ABSTRACT

Multipliers one of the fundamental units in computer arithmetic blocks. Also, the delay in the system's architecture is an important factor. In this project, it is proposed to design and analyze two novel approximate 5-2 compressors with less delay than the present exact compressors systems, while maintaining precision equivalent to the current systems. These delay efficient approximate compressors can be used in the parallel multipliers to accelerate the compression process. Approximate computing can be applied in some digital signal processing application that can tolerate errors in permissible range, where the approximate compressors come in handy. Compared with exact4-2 compressors, the proposed approximate 5-2 compressors achieve a significant reduction in delay.

KEYWORDS: Xilinx 14.7 Software

1. INTRODUCTION

Exact computing units aren't necessarily essential in applications like data mining and multimedia signal processing. They may be substituted with a similar item. Research into error-tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers. In digital signal processing, approximate complete adders are suggested at the transistor level. Partial product accumulation in multipliers is handled by their suggested full-adder design.

The use of truncation in fixed-width multiplication designs is common to simplify the circuitry. In order to compensate again for quantization error induced by the reduced portion, a variable correction component is added. Accumulation of bits is critical in terms pf power usage when using approximation methods in multipliers. If the least relevant bits of the inputs can be trimmed, then partial products may be formed in order to decrease hardware complexity. In partial product accumulations, the suggested multiplier saves just a few adder circuits. A partial product reduction trees of four 8 x 8Dadda multiplier variations is given and applied with two types of roughly 4-2 compressors.

II. LITERATURE SURVEY

There has been a lot of study on approximate computing over the last decade, but much of it has focused on adders, which are hardware abstractions. Both traditional design measurements and approximation computing metrics are available for comparison. For computer arithmetic designs, inexact computing is

especially intriguing. In order to be used in a multiplier, the authors discuss the study and construction of two novel compressors with an approximate 4-2 compression ratio. A Dadda multiplier may be multiplied using four distinct techniques for using the suggested approximation compressors. There is substantial decrease in power consumption, delay and number of transistors compared to that of an exact design. There are three parts to this approximation multiplier: a Booth encoder, a 4-2 compressor, and an approximation tree structure. For 8x8, 16x16, & 32x32-bit signed multiplication schemes, the approximate design is built and tested. This project presents and discusses simulation findings for 45 nm technology. Image processing is used to test the suggested multiplier

III. EXISTING METHOD

A Redundant Binary (RB) format may be utilized to create high-performance multipliers because of its flexibility and carry-free addition. The traditional RB multiplier adds an extra RB Partial Product (RBPP) row, since an Error-Correcting Word (ECW) is produced both by the radix-4 Modified Booth Encoding (MBE) or the RB encoding. For the MBE multiplier, this means an extra RBPP accumulation step. To save one RBPP accumulation step, a novel RB Altered Bits Generator (RBMPPG) has been developed in this study. RBMPPG is less wasteful than RB MBE multiplier because it creates fewer incomplete product rows. When the length of each multiplier operand is at least 32 bits, simulation findings demonstrate that the proposed RBMPPG-based designs greatly lower area and power consumption; these reductions over earlier NB multiplier designs result in a minor latency gain (approximately 5 percent). The suggested RB multipliers may minimize the power-delay product by up to 59 percent when compared to current RB multipliers.

IV. PROPOSED METHOD

Digital filters play a critical role in DSP. DSP's popularity is mostly due to its ability to perform at such a high level. Separation and restoration are the two primary functions ofafilter.Whenthesignalistaintedbyinterference,noise,orot hersignals,signalseparationisrequired.Consider,forexam ple,anEKGgadgetformonitoringababy'scardiacactivityw hilestillinthewomb.Themother'sbreathingandpulsewillli kelydistorttherawsignal.Thesesignalsmustbefilteredouts othattheymaybeevaluatedseparately.Whenasignalhas been distorted in some manner, signal restoration is utilized. It's possible to improve an audio recording that was recorded with low standards by filtering it. Using a lens that is not properly focused or a camera that is shaken is another example. Analog or digital filters may be used to comb these issues.

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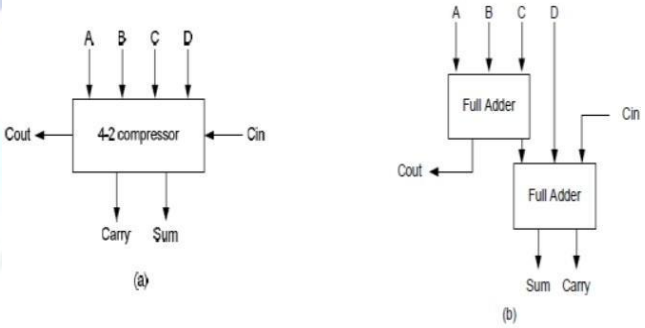


.1.1(a)adder compressor.
(b)4-2addercompressorimplementedwithfulladders.

Figures and Tables

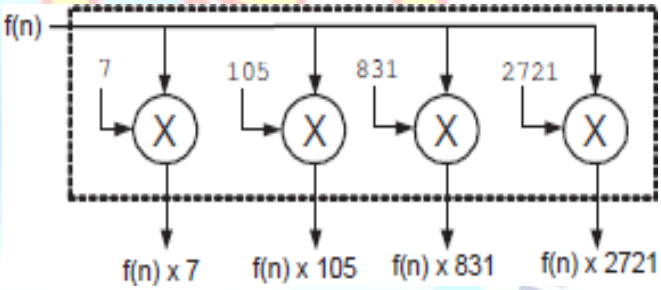


Fig:2.1Amultiplier-basedMCM example

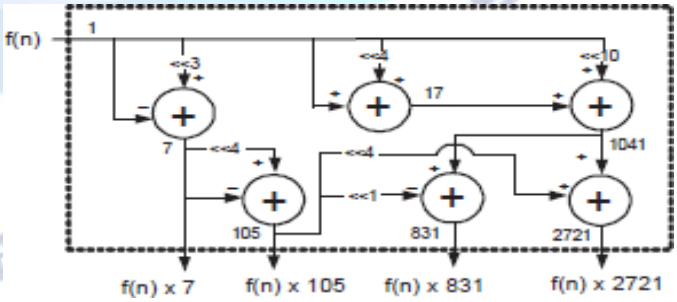


Fig:2.2 A multiplier less-based MCM exam**ple**

Equations

The straightforward method for decomposing the multiplication into adds and shifts translates 1's in

the binary representation of the constant t into shifts, and adds up the shifted inputs. For example ,fort= 71,

$$71x=1000111_2x=x\ll6+x\ll2+x\ll1+x$$

whichrequires3adds.Alternatively,the multiplication can be composed into subtracts and shifts by translating 0'sintoshifts,and subtracting from the closest constant consisting of 1's only (i.e., of theform2^n-1):

$$71x=1000111_2x=(x\ll7-x)-x\ll5-x\ll4-x\ll3 \quad (4.2)$$

Taking the best of the set wo methods yields in the worst and in the average case a solution with $\frac{b}{2}$+O(1) adds/subtracts, where b is the bit width of t.

A better digit-based method decomposes into both adds and subtracts by re-coding the number into the Canonical Signed Digit (CSD) representation [Aizen's 1961], which allows negative digits 1. Using CSD, the previous example can be improved to use only2add/subtract operations:

$$1000111_2x=1001001_{CSD}x=x\ll6+x\ll3-x$$

V. SOFTWARE IMPLEMENTATION USING XILINX

Xilinx Tools is a collection of digital circuit design software tools. Field-Programmable Gate Arrays(FPGA) as those from Xilinx or CPL devices are used(CPLD).For example, there are four stages in the design process: (a) the initial concept phase, (b) the actual design phase, and (c) functional simulation. A prototype entry tool, a Verilog Hardware Description (HDL) - VHDL or VHDL, or a mix of the two CAD tools may be used to input digital designs. Only the design flow using VHDL HDL will be used in this lab. As long as you start with VHDL HDL design requirements, you may use the CAD tools to create combinational and sequential circuits. The following are the stages in this design process:

a)Using a template-driven editor, create Verilog code design input files. Compile and design-simulation.

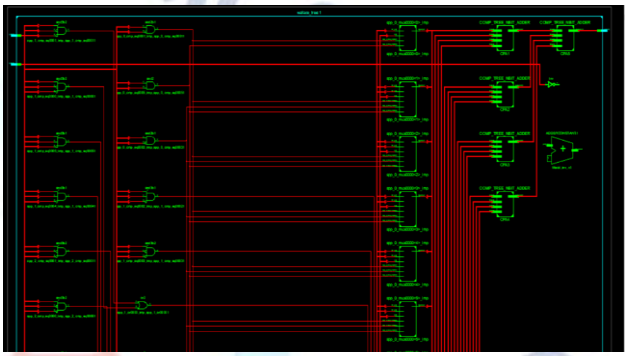
b)create the test vectors (functional simulation) instead of making use of a PLD (FPGA or CPLD).

c)Assign the design's input/output pins to a target device to implement it. Use an FPGA or CPLD to download the bit stream.

d) Interpretthe VHDL design file(s).

Testing on FPGA/CPLD device design.

VI.RESULTS



```
MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<59> (CPA2/Madd_fsum_cy<59>)
MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<60> (CPA2/Madd_fsum_cy<60>)
XORCY:CI->O           3   0.251   0.438  CPA2/Madd_fsum_xor<61> (n0538<61>)
LUT3:I0->O            2   0.043   0.347  CPA5/aa[61].b1/CCC1/Mmux_cout111 (CPA5/C<62>)
LUT5:I3->O            1   0.043   0.550  CPA5/aa[62].b1/CCC2/Mmux_sum111 (CPA5/sum<62>)
LUT6:I0->O            1   0.043   0.000  CPA5/Madd_fsum_lut<62> (CPA5/Madd_fsum_lut<62>)
MUXCY:S->O            0   0.230   0.000  CPA5/Madd_fsum_cy<62> (CPA5/Madd_fsum_cy<62>)
XORCY:CI->O           1   0.251   0.279  CPA5/Madd_fsum_xor<63> (p_63_OBUF)
OBUF:I->O                 0.000          p_63_OBUF (p<63>)
----------------------------------------
Total                     6.410ns (2.362ns logic, 4.048ns route)
                                  (36.8% logic, 63.2% route)

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oss Clock Domains Report:
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==========================================================================

tal REAL time to Xst completion: 11.00 secs
tal CPU time to Xst completion: 10.95 secs

tal memory usage is 4620648 kilobytes

mber of errors   :    0 (   0 filtered)
mber of warnings :   10 (   0 filtered)
mber of infos    :    4 (   0 filtered)
```

DELAY

VI CONCLUSION

Using signals generated and propagated ,this project proposes efficient approximation multipliers. A basic OR gate is used to create changed partial products for approximation .Half-adder, full-adder, and 4-2 compressors are all recommended to minimize the left over partial products in the final product. In Multiplier1, approximations are applied to all n bits, but in Multiplier2, they are applied just to the n 1 least significant bit. The space and power consumption of Multiplier1 and Multiplier2 are significantly reduced compared to exact designs. Both Multiplier1 and Multiplier2 save 87 and 58 percent, respectively, from accurate multipliers in APP compared to previous approximation solutions.

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Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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