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# DC-DC Boost Converter Based on Switched Capacitor Z-Network Plus 

R.Naveen Kumar, M.Viharika, K.Pragathi, J.Leela Gayathri, P.Divya<br>Department of EEE, Ramachandra College of Engineering, Andhra Pradesh, India

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## ABSTRACT

A DC-DC boost converter using a Z-network and switched capacitors (ZSCBC). The Z-network is integrated with such a switching capacitor to provide high voltage gain at duty ratios lower than the conventional quasi-Z-source dc-dc converter (QZSC), while still providing the same advantages of a common ground and decreased voltage stress on Z-network capacitors. The suggested converter, in contrary to the QZSC, places less strain on the switch the total diodes voltage even when the input voltage is raised dramatically. Z-network with decided to switch DC-DC boost converter simulation is performed in MATLAB Simulink (ZSCBC).

Keywords- Boost converter,quasi-Z-source dc-dc converter (QZSC), switched capacitor (SC), Z-source inverter (ZSI).

## 1. INTRODUCTION

The ongoing global fossil fuel energy crisis has shifted attention towards renewable energy sources. In the instance of rooftop solar (PV) power production, integration and power regulation through the DC grid are among the options [1]. Because to their very fluctuating and extremely low vout, PV panels need a series of intermediary cascade step-up energy conversion structures in order to function autonomously. In order to convert the low voltage from the Pv modules to the high voltage needed in the dc-link of the inverter, a basic dc dc - dc boost (BBC) is required. This multi-stage electronic power conversion may accomplish the aimed-for result, but the required number of intermediate converters is high, which increases the complexity of the process. More converters not only increase the number of components, but also decrease overall efficiency, which in turn
decreases dependability [2]. While theoretically BBC is optimal, the duty ratio is limited by semi of the gadgets, inductors, and efficiency concerns. significant voltage gain is possible. As a result, a front-end converter located inside the inverter's DC-Link voltage regulation should not use BBC. If you're in this predicament, the Z-source inverters (ZSI) [3] is your best bet. In addition to multistage power conversion, it supports single-stage conversion. Traditional voltage- and current-source inverters' limitations are greatly reduced. A group of semi (QZSI) inverter with voltage gains comparable to those of traditional ZSI are shown in [4]. Reducing overvoltage across Z -source capacitors is the goal of another QZSI with an interrupted input current. As compared to the ZSI, this QZSI is much larger. Several ZSI-based converters with single-stage conversion, brief protection of inverter legs, and alternative modulation
schemes for improved voltage gain, reduced inductance current ripple, and other performance indices are shown in [5]-[7]. Modulation methods, their influence on reliability Furthermore, [8] delves into the harmonics of a z-source inverter and their applications. Alterations in voltage/current stresses and power loss due to modulation methods are also discussed. In [9], inductors are swapped out with switched-inductor (SL) cells to increase the voltage gain of the ZSI. The gain is improved by the swap, but only at the price of a smaller switching frequency range and increased overvoltages on the components. With the introduction of SL-based QZSI (SLQZSI) in [10], one of the inductances of QZSI is swapped out for an SL cell, resulting in a voltage gain larger compared to QZSI [3]. To improve the voltage gains of dc-dc converters, Z-networks are combined with switching capacitors (SCs). Many workable answers to this conundrum may be found in the relevant literature. The voltage gain of ZSC has been much improved. Including a SC cells in the chain reaction. Nevertheless, it has poor voltage gain, no continuous input current, and no commonality among its output and input terminals. Improved voltage gain is achieved in the QZSC with wattage cell described in by reducing the allowable duty-ratio range and increasing the voltage stress from across devices. Even though none of the two new QZSC topologies with such a solitary SC branch share a common ground, overall voltage gain is negligible. Figure 1(b) shows a switching capacitor-based X y dc-dc converter (SCZSC), which, while being limited by discontinuous input current, provides a higher voltage gain while retaining all the properties of the converter in Fig. 1(a). Most of the converters discussed in the literature suffer from serious problems that must be fixed right away. The output and input terminals are not connected to a common ground, the voltage gain is poor, voltage stress is high across devices, the duty ratio range is narrow, and there is no common ground. These limitations prompted the proposed converter and Z-network plus SC-based solution, which creatively combines switching capacitor and the Z-network to overcome them. A new ZSCBC is presented in this article. As can be seen in Fig. 1(b), the voltage gain is increased when a quasi-Z-network is combined with a switched capacitor. ZSCBC maintains all the advantages of SOQZSC outlined in [18]. The device volt strain in ZSCBC is the same even if the circuit components are laid out differently. The steady-state
analysis and working principle of the ZSCBC are presented in. Design formulas for the converter's parameters and efficiency assessments are also supplied. below, in this paragraph. In the third section, we show our dynamic simulation and controller layout. A contrast to contemporary converters is provided in Section IV. A breakdown of the experimental results for ZSCBC as well as its regulator.


Fig.1. The Z-source switching capacitor dc-dc converter (a) (SCZSC). (b) The Dc-Dc Boost Converter with a Suggested Z-network Switched Capacitor (ZSCBC).

## 2. STEADY-STATE ANALYSIS OF ZSCB

The ZSCBC [see Fig. 1(b)] is a simple circuit that consists of a modified Z-network (L1, L2, C1, C2, D1, and D2), a SC configuration (C3, C4, C5, D2, D3, plus D4, capacitor c C6, switch S, and diode D5), and a diode D5. The converter is presumed to be operating in CCM mode. When in one of the converter's two modes, switch $S$ seems to be either engaged or disengaged.

Mode 1: This is the initial state, initiated by turning on the switch S , and illustrated by the analogous circuit in Fig. 2 (a). Since they have a negative power across them, diodes D1, D2, \& D4 are in their off states. L1 and L2 begin charging through


Fig. 2.Forms of a ZSCBC at rest
components C1 and C2 capacitors. Output capacitor C3 and C4 charge each other in a separate circuit (S-C3-D3-C4). both C1 and C2 capacitors. As the load discharges the capacitor C5, the capacitor C3 is charged by the capacitor C4 (S-C3-D3-C4). The voltage formulae for Fig. 2(a) are as follows: $\mathrm{vL} 1=(\mathrm{Vg}+\mathrm{vC} 2)$, $\mathrm{vL} 2=(\mathrm{Vg}+\mathrm{vC} 1), \mathrm{vC} 3=\mathrm{vC} 4, \mathrm{vC} 5=(\mathrm{Vg}+\mathrm{vC} 5)$, and so on.

Mode 2: Fig. 2 depicts the relevant circuitry for this operating mode (b). This setting takes effect after switch S is turned off. The duration of this mode is given by $\mathrm{D}=$ (1 D). Light emitting D3 through D5 are not conducting because they are in a reverse bias condition. Capacitors C 1 and C2 begin discharging the power from inductors L1 and L2, with only the output capacitor C6 providing power to the load. To calculate voltage, KVL came up with the following formulas: $\mathrm{vL} 1=\mathrm{vC} 1, \mathrm{vL} 2=\mathrm{vC} 2, \mathrm{vC} 5$ $=(\mathrm{vC} 3+\mathrm{vC} 4), \mathrm{vC} 4=(\mathrm{Vg}+\mathrm{vC} 1+\mathrm{vC} 2)$, and $\mathrm{vC} 5=(\mathrm{vC} 3+$ $\mathrm{vC} 4)$.

## 3. BOOST CONVERTER STEP-UP CONVERTER

The fundamental boost converter's wiring diagram. When an output voltage greater than the input voltage is necessary, this circuit is utilised.


Fig. 3.Boost Converter Circuit
In the ON state of the transistor, $\mathrm{Vx}=\mathrm{Vin}$, and in the OFF state of the transistor, $\mathrm{Vx}=\mathrm{Vo}$ due to the inductor current flowing through the diode. In this study, we assume that the inductor current is continuously flowing (continuous conduction). For the current to stay constant, the voltage that crosses the inductor must be zero.


Fig.4.Voltage and current waveform (Boost Converter)
The voltage output must be positive and constructive because the activity ratio " D " between 0 and 1 . The output voltage sense has been reversed, as shown by the negative sign.

## 4. QUASI Z-SOURCE INVERTER

By adopting a new architecture known as Quasi Z-source inverter, its drawbacks may be addressed. The ZSI has been extended to create the Quasi-Z-Source Inverter (QZSI). The link here between source and inverter in the Sort of pseudo inverter circuit is an LC impedance network, which sets it apart from the more common Z Source Inverter. The benefits of the more conventional Z-Source Inverter are fully inherited by the quasi-Z-source inverter. Continuous input current, lower component ratings, and improved dependability are just a few of the ways in which the Quasi $X$ and $y$ inverter outshines its Z-Source inverter counterpart. For these reasons, the Quasi X y inverter is an excellent choice for renewable energy power conditioning applications.


To address the drawbacks of the conventional VSI, a new architecture called the X and y inverter (ZSI) has been developed. Although these modern topologies do offer certain benefits over traditional ZSI, such as preserving the constant input current and lowering overvoltage just on Z- source capacitors, they do not provide any further voltage boost capability.

## 5. SWITCHING CAPACITORS

To achieve optimal performance, semiconductors used in Static Pulsed Power cycle between two different operating modes. The switching frequency of an SCR-based AC-DC Phase Shift Controller is about 50 Hz , whereas that of a MOSFET-based power supply is well over 1 MHz . For these and other reasons, including optimal drive, reduced power, EMI/RFI concerns, and switching-aid-networks, researchers have focused on the shifting or dynamic behaviour of Power Semiconductor devices, especially the faster ones. Both "forced commutation" and "natural (line) commutation" are often used to describe the switching behaviour of SCRs. Since the mechanics of turning on the SCR are often irrelevant, both terms pertain to its off mechanism. It is common practise to use a di/dt limiting snubber made of inductive components as a safety precaution. The 'commutation components' or'margin angle' for the SCRs are sized based on the turn-off data. The vast majority of all losses are due to conduction. In order to minimise the size and weight of the filter components, modern fast converters work at substantially higher switching frequencies. As a result, junction temperatures have been increasing due to switching losses. Devices are switched on and off in a completely silent manner by using special methods. This, in addition to effective management tactics and better evacuation of the produced heat, allows to utilize the devices with little deration. In this section, we take a look at the switching operation,
calculate the dissipation of the device, and outline the design steps again for cooling system.

Using a Switching Capacitor


Fig.6.Switched Capacitor in Charging Mode
While attached parallel to V1, the capacitor C stores energy, and when connected in series with the source, the capacitor $C$ discharges energy to the load. Whenever $\mathrm{V} 0=+\mathrm{Vc} 1$, the capacitor Bank is recharged via the S2 switch.


Fig.7.Discharged Capacitor Mode Turned On
In the proposed MLI architecture, the discharge of capacitor C begins at the front end, with switch S1 conducting. Diode D \& switch S2 are disabled when the battery is draining. The load capacity current is given by $\mathrm{V} 0=\mathrm{V} 1+\mathrm{VC} 1$, where V1 and VC1 are the energy sources powering the load.
6. SIMULATION AND RESULTS


Fig.8. Dc-dc Boost Converter using Suggested ZSCBC

Quasi-dynamic ZSI's simulation model is constructed using the topology's dynamic state-space equation; as shown, this equation is grounded in the topology's shoot-through and non-shoot-through states of operation. Diode voltage drop, capacitance, and inductance, and resistance are all taken into account. A representation in equivalent circuit form of the Quasi-ZSI circuit's behaviour in its shoot-through operational state. In MATLAB/Simulink, the blocks stand in for the individual subsystems of the dynamic model of the quasi-ZSI system. There are two loops in the quasi-Z-subsystem. network's Voltages are found by dividing integrated currents by Z-Network capacitance. Currents and voltages are not shown in any of these cycles, which just serve to obscure them. We need a state subsystem that operates independently of the switches. Throughout this time period, the voltage that flows through the capacitor will remain constant. On the other hand, the capacitor state across and the shoot-through state will be equivalent, and vice versa. By combining the currents in the right way, we can calculate the true voltage across the capacitors.The maximum Dc-link voltage is calculated using the current and voltage signals produced by the voltage switching block and the current switch block in the loop.


Fig.9. MOSFET Switching Device Voltage and Current Measurements


Fig.10. Current and voltage produced by a metal-oxide semiconductor field-effect transistor


Fig.11. The Current and Voltage of a Switched Capacitor Are Measured


Fig.12.The Current Waveform at the Output of a Switching Capacitor

When interfaced with practically any logic circuit or driver that can provide a positive output, the MOSFET can function as a switch thanks to its positive voltage level and very high (almost infinite) input resistance. Protecting the Load Voltage from Irregular Changes (Vg :20 V-95V, Ig:0A-45A ).the switching pulses and currents in the part of the device and output capacitor. Maximum value under damping of the input inductor current is achieved for the waveform of current travelling through the inductor, capacitance, diodes, and output current.

The output current has stabilised and shows just a little amount of ripple. voltage load against erratic changes (Ig:2A-3A)


Fig.13. The switching pulses and currents in the output capacitors
The switching pulses and currents in the output capacitors. The diode voltage stresses Vd1 and Vd3 are comparable, as are the diode current stresses Id1 and Id3. Inductor, capacitors, diode, and terminal voltage waveforms are all underdamped to maximise the input inductor current's value. withstand a surge in voltage ( Vg :10 V-95V).


Fig.14. DC-DC Boost Converter Output Voltage Using a Z-Network and a Switching Capacitor

The switching pulses and currents in the output capacitors. The diode voltage stresses Vd1 and Vd3 are comparable, as are the diode current stresses Id1 and Id3. Maximum value under damping of the input current is achieved for the waveform of current travelling through the inductance, capacitors, diodes, and output current. Protecting the Load Voltage from Irregular Changes ( Vg :40 V-85V).


Fig.15.Waveform of Voltage Produced by a Switched Capacitor at Its Output

## 7. CONCLUSION

In this research, we introduced a ZSCBC that improves upon QZSC in terms of voltage gain while keeping the main advantages of QZSC, such as common ground, a wider duty ratio range, and less undervoltage on the Z-network capacitors. A stable analysis of the ZSCBC compared with the other reported topologies 1-7 revealed that 1) the switch and the electrodes encounter the same voltage stress regardless of their actual location, 2) the strain on the toggle and electrodes is lower at even high voltage gain, and 3) the addition of an emitter network increases the voltage gain. The proposed converter offers an extra feature not seen in the first six topologies: voltage gain enhancement. Shuttered stability of ZSCBC was ensured by doing comprehensive analyses and developing a unified power controller. Using actual and measurable data, an a Controller's utility for regulating against transient fluctuations inside the load and source voltages was shown. The designed controller also efficiently nullified the influence of the source's low-frequency disturbances. There is load voltage variance of on the output of a $X$ and $y$ shunt capacitor dc-dc Buck converter ( $45 \mathrm{~V}-85 \mathrm{~V}$ ).

## Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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