International Journal for Modern Trends in Science and Technology, 9(03): 200-204, 2023

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST0903030
Available online at: http://www.ijmtst.com/vol9issue03.html

Modernization of 31 Level Distribution Network with Lower DC Voltage Sources

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To Cite this Article
Ch. Nikhil Kumar, Ganapavarapu Harish, Lakshminarayana Muvva and B.Kavya Santhoshi. Modernization of 31 Level Distribution Network with Lower DC Voltage Sources. International Journal for Modern Trends in Science and Technology 2022, 9(03), pp. 200-204. https://doi.org/10.46501/IJMTST0903030

Article Info
Received: 26 February 2023; Accepted: 15 March 2023; Published: 18 March 2023

ABSTRACT

In this study, we provide a new topology for a 31-level asymmetrical multilevelinverter that operates on a single phase and requires fewer parts than previous designs. Based on an H-bridge and a pair of asymmetric DC sources, the suggested topology may provide an output voltage with up to 31 discrete steps. Realization of the basic 13-level multilevel inverter (MLI) architecture; further development of the topology for 31-level; potential usage in renewable-energy applications. As a result, the system's size, cost, and number of individual components are all reduced. Despite MLIs' numerous benefits, dependability is a major issue because of the extra parts needed to cut down on THD. Researchers have a significant difficulty in attempting to improve dependability while reducing total harmonic distortion (THD). Total standing voltage (TSV), cost function (CF), and power loss are among the many metrics studied for both primitive 13-level and advanced 31-level MLIs. The inverter is put through its paces in the lab with a wide range of dynamic load conditions, including combinationalloads and unexpected load disturbances. The suggested MLI's costfunction is compared to other previously published topologies in terms of total standing voltage, and it is shown to be cost-effective. Numerous characteristics are compared in depth and graphically. For the suggested MLI, it is shown that less TSV and components are needed. Total harmonic distortion (THD) levels achieved are well below IEEE limits. The architecture is tested theoretically in MATLAB/Simulink and then empirically using a hardware prototype in a range of environments.

KEY WORDS: Total harmonic distortion, Total Sequence Voltage, Total Sequence Voltage Calculation, and Cost Function (CF) in Multilevel Inverters (THD).

1. INTRODUCTION

Multilevel inverters have a bigger market share because of their high power operating capacity and other benefits such as reduced electromagnetic interference, improved power quality, and lower switching losses [1, 2]. According to certain sources[not in citation given] These MLIs employ a variety of DC sources and power electronic circuits to create a discrete-step output voltage waveform. There is a large selection of power semiconductor switches that may be utilised in this circuit. [3] Boosting the volume may also enhance the quality of the waveform as a whole. [4] Increasing the number of circuit components to improve MLI reliability and efficiency raises circuit costs.

MLIs may be diode clamped, flying capacitor, or cascaded H-bridge (CHB). Depending on the

magnitudes of the DC voltages, CHB inverters may be classified as symmetric or asymmetric [6]. There are two major types of MLIs, and they are symmetric and asymmetric, respectively. All of the DC voltage sources in the symmetric multilayer inverter I'm employing are of the same strength. Every CHB type inverter module may either have a positive, negative, or 0 volt output. The module's state determines the output's current condition. The output voltage of a CHB type inverter may be determined by summing the voltages of each module [7], [8]. High-voltage voltage balancing is harder when using an FC or NPC type inverter as opposed to a CHB type inverter [9].

Cascaded multilevel inverters have seen a number of suggested topologies from a variety of control methods in recent years [4, [10]–[13]. Multiple symmetric cascaded multilevel inverter topologies are shown in [3], [14–20]. Benefiting greatly from low DC voltage sources, which is a key factor in deciding an inverter's cost, these topologies have several applications. However, the primary downside of various topologies is the increased need of bidirectional switches in places where a significant number of IGBTs is required. In [21], an asymmetric type inverter is shown as an architecture, where more IGBTs are needed due to the higher number of bidirectional power switches. A revolutionary architecture with a decreased number of switches provided with multiple algorithms in [18] yet numerous voltage sources exist, which is a downside of this topology. Minimizing these difficulties by efficient use of semiconductor devices is possible. Using sources with different magnitudes of dc voltage allows for a reduction in the total number of switches required [3]. Several devices [22], [23] are demonstrated that have an enhanced voltage level with lower power switching. The output of these devices is a DC step and is transformed to AC step using a full-bridge converter. Because the full-bridge converter filters out the higher voltages, its use is restricted to to those applications that need the high voltages. Many new topologies are provided to minimise the components count for both single-phase and three-phase system. In [24], we see the three-phase system represented as a collection of three independent phases.

Some multilayer output designs need fewer switches and DC sources [25]. [26]–[29] show topologies for bidirectional current with fewer switches. Antiparallel-coupled bidirectional switches are used. As switches become increasingly modular, cascading sub-units may reduce blocking voltage at each. As output level grows, such topologies need more switches. So, new MLI architectures with fewer components and blocking voltage are needed. Inverter price drops. A packed H-bridge MLI design [30, 31] has been suggested; it connects basic units on both sides of the full-bridge. Topologies are constructed without H-bridge to reduce voltage demand on circuit switches. Many of these topologies need certain items.

Single-phase inverters were originally connected in series to create the multilayer inverter design. A cascaded H-bridge (CHB) inverter [7] is a common name for this setup. By connecting diodes to the neutral point, as in Neutral Point Clamped (NPC) inverters, many levels of output voltage may be generated from a single DC source [8]. A Flying Capacitor (FC) inverter was built by combining multiple capacitors [9]. We often refer to the aforementioned architectures as "Classical Topologies." Figure 1 illustrates the requirement for innovative control procedures for the reduced device count inverters that have been the focus of much research in recent years. Packed U-Cell (PUC) is a three-output voltage source compatible modular construction. The number of active switches remains constant [10] in this setup..

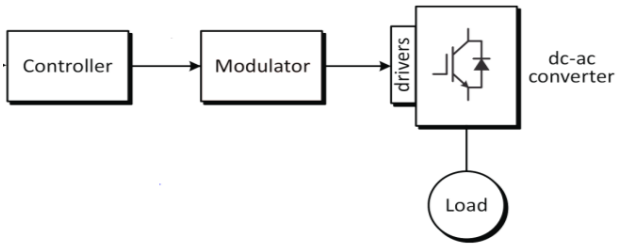

Fig. 1. Open-loop operation of DC/AC converter

2. MULTILEVEL INVERTER TOPOLOGY

In Fig. 2, we show the block diagram of the circuit that creates the 31-level inverter output, which comprises of the Level Generation Circuit, Polarity Generation Circuit, and Driving Circuit. Asymmetric designs may be able to provide more power than their symmetric counterparts when using the same number of semiconductor devices and voltage sources. The MLI

configuration is shown in Figure 3, and it comprises of the Level generating unit in the asymmetric basic circuit and the Polarity generation circuit in the H-bridge inverter. In the circuit that produces polarity, the switches will be subjected to more stress than those producing a constant level.

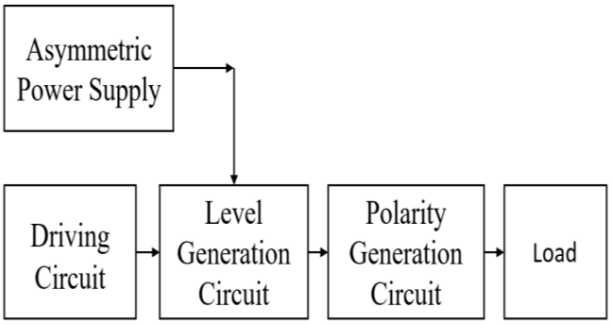

Fig. 2. Control block diagram

Because this design only makes use of unidirectional semiconductor switching components, the total number of MOSFETs and driver circuits remains same. In a multilayer inverter circuit, the current, blocking voltage, and switching frequency all have a connection with one another, which results in switching losses. The current status of each switch that makes up the level producing unit is broken out in Table 1. A total of 15 levels is produced when the outputs of the S1, S2, S3, and S4 level generators as well as those of the T1 and T2 polarity generators are combined. Turning off switches S1, S2, S3, and S4 simultaneously will result in the volume being reduced to zero. When the outputs of the polarity generator (T2 and T3) are combined with the outputs of the level generator (S1, S2, S3, and S4), a negative half cycle will be produced. This negative half cycle is the opposite of the positive half cycle.

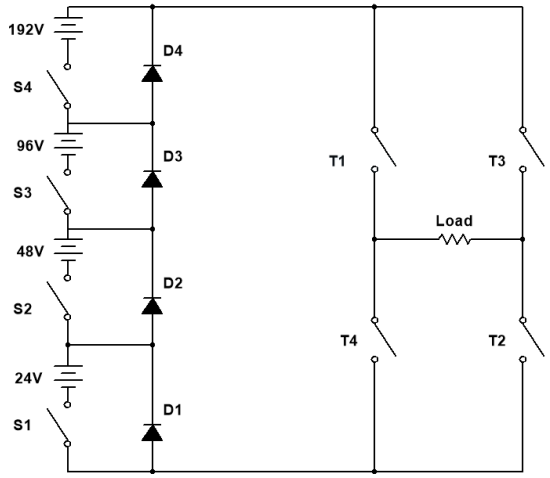

Fig. 3. Circuit Diagram

The third state, for instance, has diodes D3 and D4 forward biassed and switches S1 and S2 turned on. Vo = V1 + V2 is the result we acquire during the positive half cycle. To get the voltage values at the output, this procedure is repeated for each of the other states.

State	Switches States				Output Voltage
	S4	*S3*	*S2*	*S1*	
0	0	0	0	0	0
1	0	0	0	1	V_1
2	0	0	1	0	V_2
3	0	0	1	1	V_1+V_2
4	0	1	0	0	V_3
5	0	1	0	1	V_1+V_3
6	0	1	1	0	V_2+V_3
7	0	1	1	1	$V_1+V_2+V_3$
8	1	0	0	0	V_4
9	1	0	0	1	V_1+V_4
10	1	0	1	0	V_2+V_4
11	1	0	1	1	$V_1+V_2+V_4$
12	1	1	0	0	V_3+V_4
13	1	1	0	1	$V_1+V_3+V_4$
14	1	1	1	0	$V_2+V_3+V_4$
15	1	1	1	1	$V_1+V_2+V_3+V_4$

The subsequent chapters will cover the planning of this circuit. This circuit is simulated to test the THD and other characteristics.

3. WORKING:

From this structure, we can deduce that the semiconductor devices utilised in the polarity generator unit have a voltage blocking capacity of Vm. As a result, MOSFETs with higher ratings than the polarity generating unit will be employed in the level generation section [17]. Using a special arrangement, we may acquire new voltage levels by subtracting existing ones in a ternary setup.

Merits of this circuit are:

- Circuit is simple and modular
- Only unidirectional switches are used
- High rated switches can operate at fundamental frequency.

Open-loop control utilises a non-measurement dependent reference [18]. This benchmark has already been calculated (offline) for a specific operating condition. Because of this, the system's dynamic reaction suffers. The inability to use trinary combinations and the need for isolated DC sources are the main drawbacks of this architecture. The total harmonic distortion (THD) [11] is improved as a primary function of multilayer inverters.

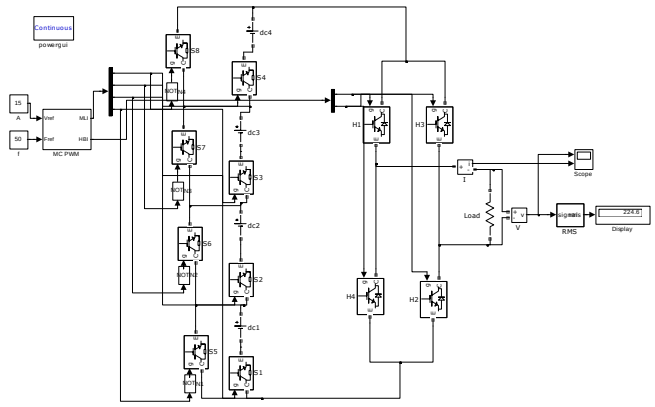

Fig. 4. The 31-level inverter's simulation diagram

Simulation Results

Following is an examination of the outcome of a 31-level inverter with the optimum number of switches. The following are examples of the input voltage sources: In this case, V1=24V, V2=48V, V3=96V, and V4=192V. Voltage output is assumed to be 50Hz. Table 1 displays the switching states and the corresponding magnitudes of the output voltage Vo. The semiconductor switching device, or MOSFET, receives the output from the pulse generator.

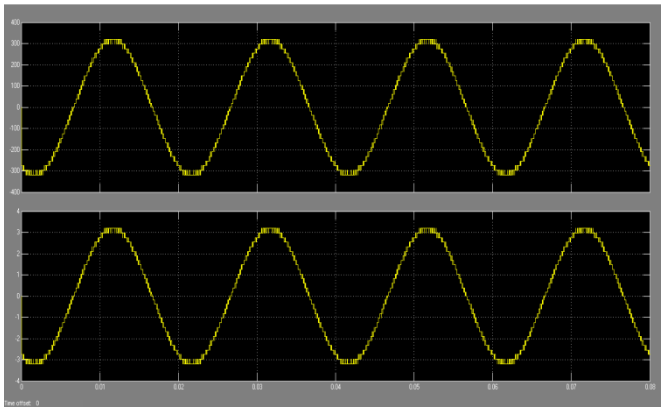

Fig. 5. Waveforms of voltage and current at the output have been modelled.

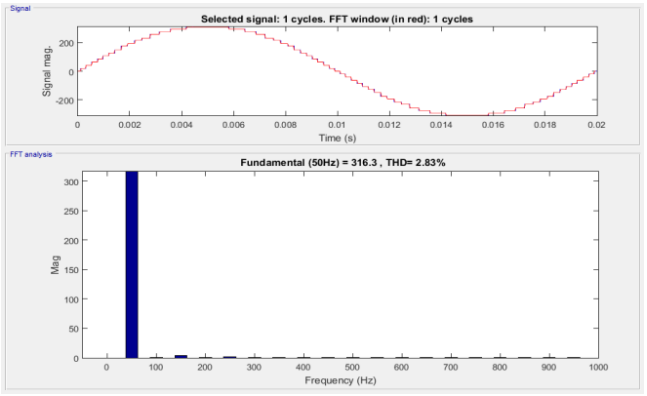

Fig. 6. Harmonic waveform and output voltage waveform simulated

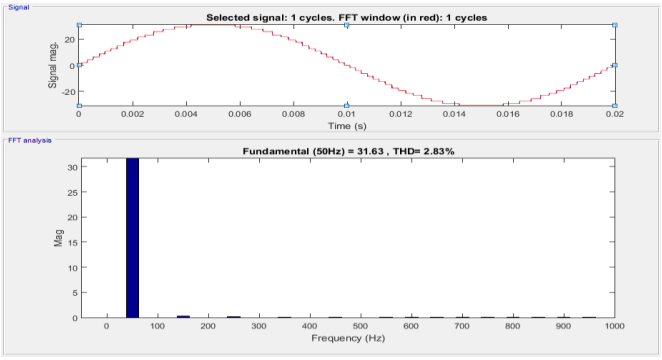

Fig. 7. The waveform and harmonic spectrum of the output current, as simulated.

There is a 1V amplitude to these pulses. The most stressed switch has the slowest operating frequency [19]. The inverter's output voltage and load current both fall within the 2.83% tolerance of the IEEE standard for harmonics (IEEE 519). Figures 6 and 7 illustrate this point.

4. CONCLUSION:

In this work, we suggest a multilayer inverter architecture that is optimal for medium voltage applications. The fundamental benefit of this layout is its straightforward construction, which makes it possible to minimise both the physical dimensions of the multilayer inverter and the complexity of the driving circuit. In order to simulate, we use the MATLAB/SIMULINK environment. A 31-level output with THD of 2.83% is achieved. In addition, characteristics of this topology at increased output levels may be deduced. The optimal asymmetric topology has been determined after evaluating its pros and cons against those of competing architectures. The MLDCL asymmetric structure inverter's semiconductor

switching devices have lower blocking voltage values compared to those of inverters with other asymmetric topologies. Here we give the simulated outcome for the recommended strategies. The number of MOSFETs required by the proposed inverter architecture has been shown to be reduced. By employing this topology we may equivalently decrease number of gate drivers, thereby lowering the size of the circuit. Energy savings are achieved by not having to use additional passive filters.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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