



Design and simulation of an asymmetrical 23-level inverter with modulation Techniques

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To Cite this Article

Pavan M and Dr. Madhusudhana J. Design and simulation of an asymmetrical 23-level inverter with modulation Techniques. International Journal for Modern Trends in Science and Technology 2022, 9(01), pp. 32-36. <https://doi.org/10.46501/IJMTST0901006>

Article Info

Received: 20 December 2022; Accepted: 15 January 2023; Published: 20 January 2023.

ABSTRACT

For medium voltage, high power regulation the Multilevel Inverters (MLI) are attracting industry and academic researchers. MLI generates the desired output in the form of stepped waveforms with reduced harmonics. The MLI is expected to be realised using a variety of traditional topologies. Traditional MLIs have the disadvantage of requiring additional components, which increases the complexity of gate pulse production. As a result, MLI's overall costs will rise. This research proposes a hybrid topology to alleviate these drawbacks. With the increase in the number of steps in output voltage, the number of dc sources, power switching devices, converter cost, and space required is significantly reduced compared to typical MLIs. The design and simulation of a hybrid converter using several types of PWM approaches are covered in this work. This hybrid converter combines a T-Type structure and a half bridge inverter that is back-to-back connected. The proposed construction is designed and simulated by MATLAB Simulink software. The proposed 23 level inverter circuit is designed and simulated by Equal phase angle modulation technique and half height modulation technique, THD is compared.

KEYWORDS: multi-level inverter, equal phase angle modulation technique, half height modulation technique, THD

1. INTRODUCTION

For many years, H-bridge traditional inverters were employed in numerous industrial applications due to their simple switch configuration and ease of control. Their output is of poor quality, with more harmonic components, and their use is unsatisfactory in several applications. PWM inverters with a high switching frequency have a low efficiency and a high dv/dt stress. Traditional H-bridge inverters and Pulse Width Modulated inverters have been replaced by new multilevel inverters.

Multi-level inverter techniques are used in industrial applications to reduce voltage stress on power equipment and create high-quality output voltages. Multi-level inverters increase ac power quality by converting power in short voltage steps, which results in decreased harmonic content. When compared to a two-level output voltage waveform, the harmonic content of this output voltage waveform is substantially reduced.

In response to the conventional limitations of inverters, this paper proposes a new asymmetrical 23-level inverter design, simulated with MATLAB

Simulink. Let us discuss the proposed inverter circuit design and switching table.

2. MULTILEVEL INVERTER

Because of the well-known drawbacks of traditional two-level inverters, a multilevel inverter is required. Multilevel inverter produces a desired AC voltage waveform from several levels of DC voltages. These DC voltages may be or may not be equal. AC voltage produced from these DC voltages is of stepped waveform. With this type of inverters, improvements in the harmonic quality of the output voltage can be achieved. Renewable energy sources such as photo-voltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for medium and high power applications. The benefits of a multilevel inverter, as well as the basic notion of a multilevel inverter, are also explained.

Need of Multilevel Inverter

The output voltage of two-level inverter contains more harmonics.

- PWM-VSIs operating at high switching frequencies are rarely preferred for high power applications due to considerable switching losses.
- PWM-VSIs generate Electromagnetic Interference (EMI).
- As the two-level inverters have to switch between the two extreme levels of the dc-link voltages, they are subjected to High dv/dt .
- The task of reducing harmonic content in the output voltage is addressed by the multilevel inverters.

Advantages of Multilevel Inverters

- They are suitable for high-voltage and high-current applications.
- They have reduced Total Harmonic Distortion (THD) in voltage with increased number of voltage levels.
- They can be operated with the lower switching frequency and hence the switching losses are reduced.
- They have higher efficiency.

- Power Factor is close to unity for MLIs used as rectifier.
- No Electromagnetic Interference (EMI) problem exists.
- It is possible to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output.

3. CIRCUIT DIAGRAM AND IT'S OPERATION

Figure 1 shows a single-phase multi-level inverter. This multi-level inverter is a 23-level CHB with a T-Type structure and a half bridge inverter that is back-to-back connected, as shown. Figure 1 shows the 23-Level Inverter design. five dc sources, and nine switches make up the architecture of the Hybrid Cascaded Multilevel Inverter. This configuration is made up of a T-Type structure and a half bridge inverter that is back-to-back connected,. This setup removes the need for additional dc sources while also reducing the amount of switches necessary.

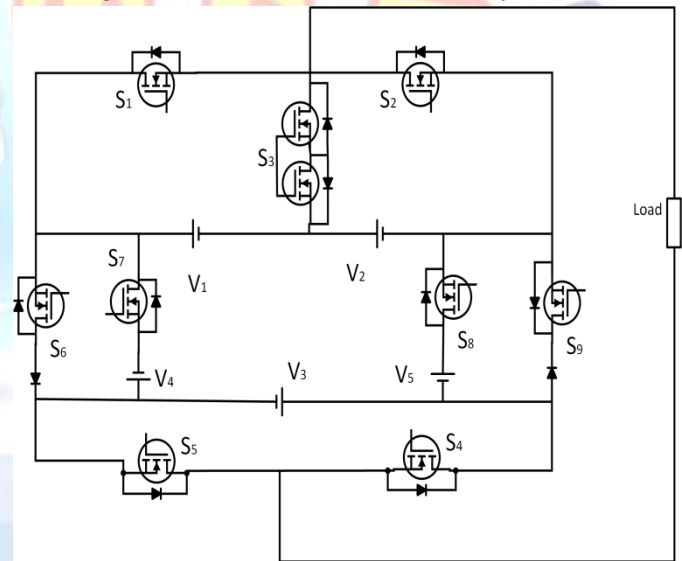


Figure 1 : 23- level asymmetrical inverter with reduced switches.

This paper seeks to introduced the general basic architecture of a 23 voltage-level optimal inverter which is depicted in Fig. 1. The module has five dc sources along with nine unidirectional switching devices S1, S2, S3, S4, S5, S6, S7, S8 and S9 in which we have eight unidirectional switches and one bidirectional switch S3. Dc sources values are ($V1=V2, V3, V4=V5$) which are all different. Therefore, the proposed structure offers an asymmetric structure.

To avert short-circuits in the dc sources, the unidirectional switches S1, S2, S4, S5, S6, S7, S8, S9 operate in an opposite mode. In this basic module, switches S8, S9 are used to generate positive levels and switches S6, S7 are used for negative levels. Considering this information, Table I details the feasible switching combinations of the suggested module. The optimal module creates nine levels by choosing the values of dc sources equally. If these magnitudes are different, the suggested inverter will generate more voltage levels. In this paper, they are considered as follows:

$$V1 = V2 = 1Vdc$$

$$V3 = 3Vdc$$

$$V4 = V5 = 6Vdc$$

Voltage level	S1	S2	S3	S4	S5	S6	S7	S8	S9
-11	0	1	0	1	0	0	1	0	0
-10	0	0	1	1	0	0	1	0	0
-9	1	0	0	1	0	0	1	0	0
-8	0	1	0	0	1	0	1	0	0
-7	0	0	1	0	1	0	1	0	0
-6	1	0	0	0	1	0	1	0	0
-5	0	1	0	1	0	1	0	0	0
-4	0	0	1	1	0	1	0	0	0
-3	1	0	0	1	0	1	0	0	0
-2	0	1	0	0	1	1	0	0	0
-1	0	0	1	0	1	1	0	0	0
0	0	1	0	1	0	0	0	0	1
1	0	0	1	1	0	0	0	0	1
2	1	0	0	1	0	0	0	0	1
3	0	1	0	0	1	0	0	0	1
4	0	0	1	0	1	0	0	0	1
5	1	0	0	0	1	0	0	0	1
6	0	1	0	1	0	0	0	1	0
7	0	0	1	1	0	0	0	1	0
8	1	0	0	1	0	0	0	1	0
9	0	1	0	0	1	0	0	1	0
10	0	0	1	0	1	0	0	1	0
11	1	0	0	0	1	0	0	1	0

Table I : Switching Table for 23-level asymmetrical inverter

4. MODULATION TECHNIQUES

Modulation is the process that used to switch the power electronic device from one state to other. The purpose of the modulation techniques is to generate the multilevel output waveform. Each modulation technique generates different switching pulses to achieve the desired output waveform.

Equal Phase (EP) Switching Modulation Technique

In this technique the switching angles are distributed averagely over the full complete cycle ranging from 0 – 360 degrees. The equation to calculate the switching angles by Equal Phase (EP) method is given by

$$U_g = g * (180 / M) \text{ where } g = 1, 2, 3, 4, \dots, 2M$$

M = Number of output voltage levels

Half height switching modulation technique method

The half height method is employed to reduce the harmonic content at the output voltage side. For M is odd, 2(M - 1) switching angles is determined for the period of 0°–90° Since the sine wave is symmetrical waveform, the positive half cycle is mirror symmetrical to its negative half cycle. We define the switching angles in the first quadrant period (i.e., 0°–90°) as main switching angles. Switching angles in second quadrant (90°–180°), third quadrant (180°–270°), fourth quadrant (270°–360°) are to be calculated.

$$\alpha_i = \sin^{-1} \left[\left(i - \frac{1}{2} \right) \frac{2}{N-1} \right]$$

where $i = 1, 2, \dots, (N-1)/2$
 $N =$ level of switching angles

5. MATLAB SIMULINK MODEL

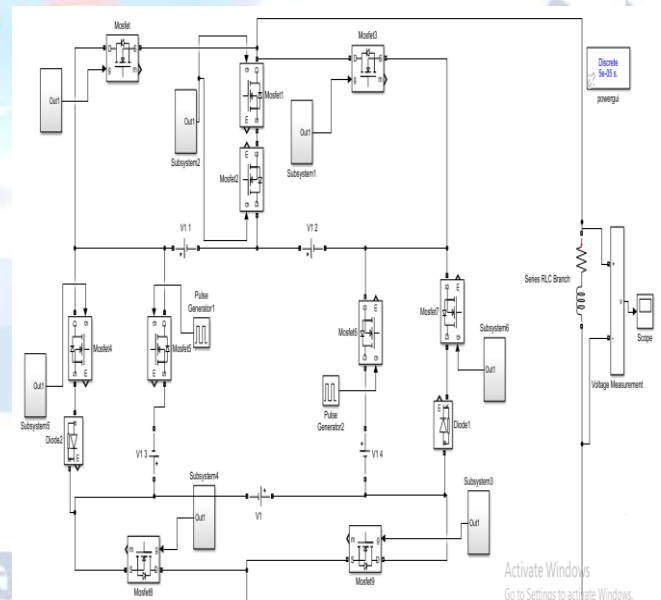


Figure 2 : Simulation diagram of 23- level asymmetrical inverter

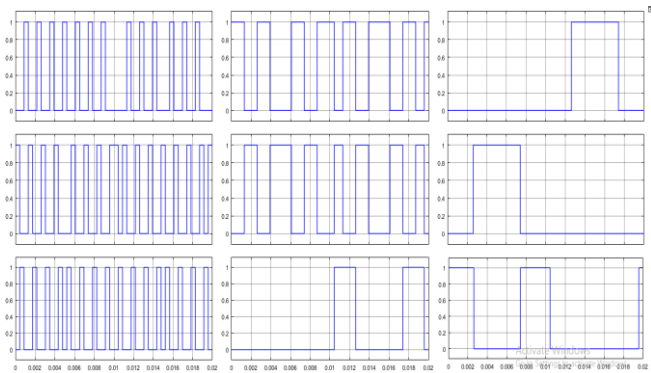


Fig 3 : Timing diagram of switches for EPA modulation technique

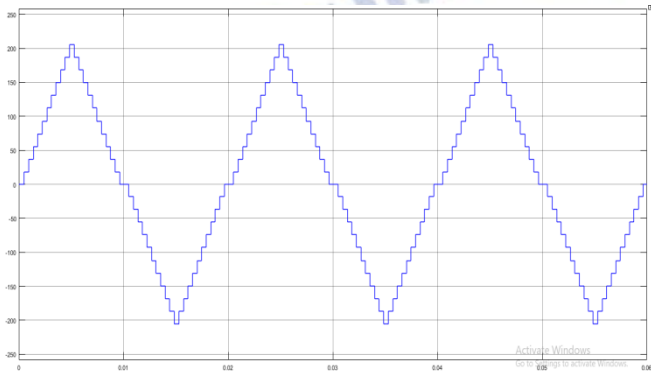


Fig 4: Output voltage waveform of asymmetric 23- level inverter circuit using EPA method

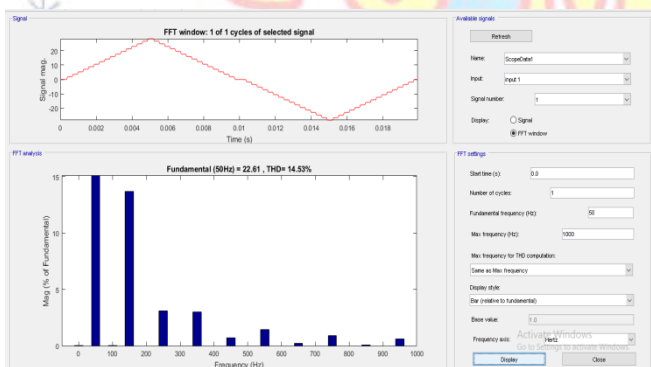


Fig 5 : FFT analysis for THD of 23-level proposed topology using equal phase angle modulation technique.

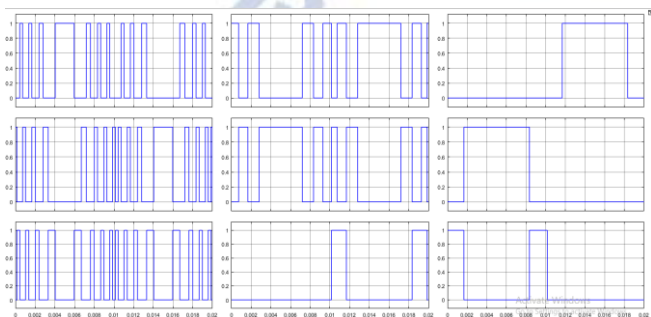


Fig 6 : Timing diagram of switches for half height modulation technique

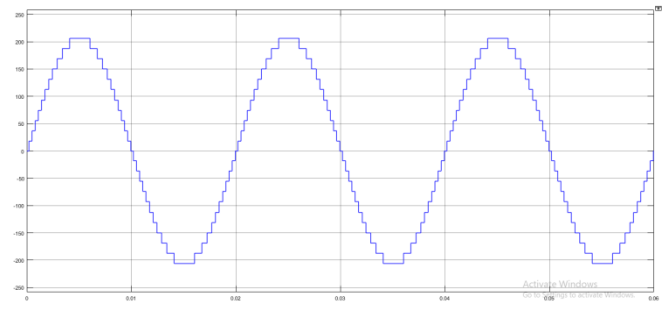


Fig 7: Output voltage waveform of asymmetric 23 level inverter circuit using half height method

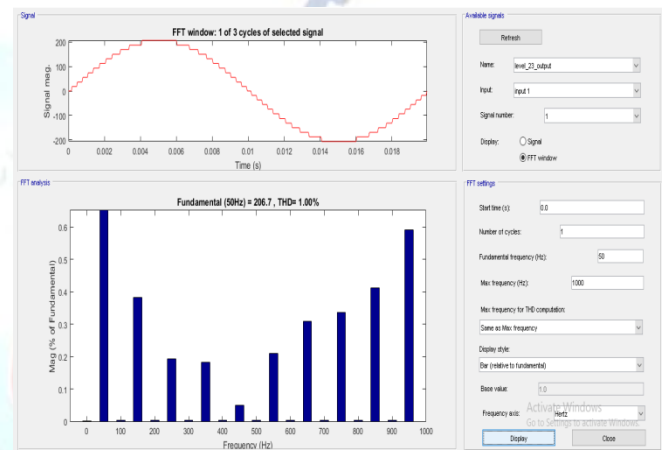


Fig 8 : FFT analysis for THD of 23-level proposed topology using half height modulation technique

Modulation technique	Type of load	THD % voltage
Equal phase (EP) modulation technique	<i>R-L Load</i> $R=45.3833ohms$ $L=1.083mH$	14.53%
Half height modulation technique	<i>R-L Load</i> $R=45.3833ohms$ $L=1.083mH$	1.00%

Table 3: Comparison table of results with Equal phase modulation technique and half height modulation technique.

6. CONCLUSION

In MATLAB-Simulink, a new family of multilevel inverters has been introduced and created. When compared to typical similar inverters, it has a lower number of switches. The new topology's operation modes and switching technique are discussed. An equal phase modulation strategy is used with the aid of a pulse generator to research the THD of this model, and

then a SHE modulation technique is used with the use of a pulse generator to examine the harmonic elimination of the new topology based on the theory of resultant. Traditional MLIs have the disadvantage of requiring additional components, which increases the complexity of gate pulse production. As a result, MLI's overall costs will rise. To address these flaws, this study proposes a hybrid architecture, which includes the design and simulation of a hybrid converter using several PWM approaches. This hybrid converter is made up of a single phase T-Type inverter and an H-Bridge module with sub switches. Switching functions are easily improved in this hybrid topology. The right figures and tables demonstrate the operational principle. In simulation findings, a high-quality output voltage wave is obtained. It reduces the dv/dt stresses that switches are subjected to, as well as the output voltage harmonic component. The simulation results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the in the output voltage THD i.e. 1.00%.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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