International Journal for Modern Trends in Science and Technology, 8(S09): 32-35. 2022

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST08S0908
Available online at: https://www.ijmtst.com/vol8si09.html

Optimisation in Modern VLSI Placement

Radeep Krishna R[1] | Abraham C.G[2] | KarthikKumar S[3] | Sruthi Prasad[4]

[1,2] Department of ECE, Mangalam College of Engineering, Ettumanoor, Kerala, India
[3,4]Department of EEE, Mangalam College of Engineering, Ettumanoor, Kerala, India

To Cite this Article
Radeep Krishna R, Abraham C.G, KarthikKumar S and Sruthi Prasad[4]. Optimisation in Modern VLSI Placement. International Journal for Modern Trends in Science and Technology 2022, 8(S09), pp. 32-35. https://doi.org/10.46501/IJMTST08S0908

Article Info
Received: 26 May 2022; Accepted: 24 June 2022; Published: 30 June 2022.

ABSTRACT

Placement is crucial to the creation of IC placements for the new technology. Compared to 2D IC installation, it provides more advantages. It has the ability to significantly reduce latency, shorten interconnects, use less energy, and increase speed and bandwidth. This study seeks to use Parallel Genetic Algorithm (PGA) in contemporary VLSI placement to decrease the area and wirelength of ISPD98 placement benchmark. The higher numbers of blocks are put one over the other in modern VLSI

KEYWORDS: Parallel Genetic Algorithm (PGA), area, wire length, VLSI placement, ISPD 98

1. INTRODUCTION

Everyday life has included electronic systems. These electronic systems are based on integrated circuit (IC) chips and are widely utilised in the fields of communication systems, software, and hardware systems. Due to the rapid advancement of integration technologies and the numerous advantages of large-scale system design, the electronics industry has experienced explosive expansion over the past few decades [1]. The manufacturing capacity and complexity of massive electronics systems, along with their economic advantages, are driving a revolution in their design and posing difficulties for integrated circuit designers. One of the crucial areas of VLSI backend design is VLSI placement. The circuit placement makes an effort to position fixed shape blocks on a layout surface in a way that minimizes the area and wirelength. To enable interconnection between
blocks, some space has been purposefully left empty between the blocks. Placement has been demonstrated to be an NP-hard problem. The major goals of VLSI placement are to reduce the circuit area and interconnect delay, introduce interconnect area, and position all logic cells within flexible blocks. The results of the placement tool will have a significant impact on how well the circuit performs. Placement in places with low total wirelength but high traffic density frequently results in routing detours around the area, which increases routed wirelength. the region and by decreasing the dead space or dead cells in the ISPD98 Placement benchmark, wirelength can be simultaneously decreased.In order to increase system performance, manufacturers are now creating integrated circuit.chips with numerous functions. Both the number of transistors and the level of integrated circuit chip density are rising. There will be various difficulties to overcome, such as a rise in temperature level, when the density of integrated circuit chips increases. The designer must overcome these obstacles. High-rise, multi-layer chips are currently the focus of study. Circuitry is not only arranged horizontally but also vertically by designers. Technically speaking, the 3-D approach known as VLSI stacking

refers to the vertical layouts of circuits for integrated circuit chips. More designers have looked into the placement of VLSI integrated circuit chips. This demonstrates the expansion of VLSI chip placement over the past few decades. Both the use of contemporary physical synthesis tools and the quality of IC chips have risen. The issue is also remains exceedingly difficult for a variety of reasons. According to Moore's Law, the circuit density on an integrated circuit chip is increasing first. Here, the entire design is placed in order to derive a physical hierarchy. The second issue is the system on chip (SoC), which has time and routing restrictions. These limitations are thought to be the most complicated. The power reduction in the current VLSI integrated circuit chip layout would be the other significant difficulty as well as the circuitry's increased density. In the semiconductor industry, it is thought to be a significant and important effort to reduce the area and wire length in the current VLSI integrated circuit chip.

2. METHODOLOGIES AND IMPLEMENTATION

1.Algorithm:

For VLSI placements, numerous algorithms have been proposed. For this, algorithms like
stimulated annealing are employed. In this case, the Parallel Genetic Algorithm is used.

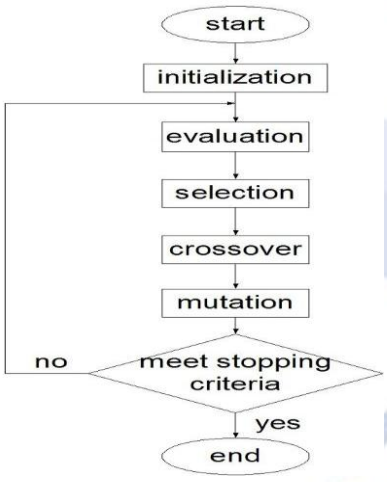

Fig1.1: Parallel Genetic Algorithm Flow

Problems that arise throughout the optimization process are resolved using a parallel genetic method, as shown in fig. 1.1. It is the greatest algorithm because it is the simplest and quickest way to optimise the area and wirelength in the placement of contemporary VLSI chips. The initialization, evaluation, selection, crossover, and mutation phases of the parallel genetic algorithm are followed during optimization. Every member of the population has their fitness assessed every generation. In an optimization problem, the fitness is often the value of the objective function. From the present population, the Fitness individual is chosen at random, and each person's chromosomes and DNA are changed to create the fittest offspring.The new generation of candidate solution is then used in the next iteration of the algorithm. Commonly, the algorithm terminates when either a maximum number of generation has been produced, or as satisfactory fitness level has been reached for the population. Parallel genetic algorithms are adaptive heuristic search algorithm based on the evolutionary computing a rapidly growing area of intelligence. Parallel genetic algorithm is inspired by Darwin's theory on –"survival of the fittest". The Parallel genetic algorithm (PGA) represents an intelligent exploitation of a random search used to solve optimization problems [2].

In order to optimise area and wirelength when placing current VLSI chips, the ISPD98 benchmark is employed. The fundamental benefit of the ISPD98 benchmark over alternative placement benchmark files is that without it, it is debatably impossible that the academic community could have produced consistent physical design throughout the past fifty years. This benchmark will serve as our choose the parents at random. Crossover between the chosen parents will occur when the selection process is finished, producing offspring. The fitness value algorithm is applied accordingly.

2.Optimization:

An improved solution to the issue is found through optimization. Three things dominate the optimization issues: (I) A desired minimization or maximisation of an objective function (II) A group of factors or unknowns that have an impact on the objective function. (III) A collection of restrictions that permit some values for the unknowns while excluding others [3].

The main challenge in placing VLSI (Very Large Scale Integration) chips is optimising the area and wirelength. The Parallel Genetic Algorithm can be used to minimise these parameters.

3.Area And Wirelength Calculation:

Before determining the wire length, several assumptions must be made. It states that the Through Silicon Via (TSV) should be regarded as a cell before computing the wire length in the Half Perimeter model layer by layer. In contemporary VLSI design, TSVs are used to connect two layers.

$$Lt=\sum l\,(Em) \quad (1)$$

The wire length in the m layers is represented by l (Em), where Lt denotes the total wire length in the 3-D IC device.

All of the net's p pins and as many additional p-2 Steiner (branching) points are connected by the rectilinear Steiner minimal tree (RSMT) model. It is NP-hard to determine the best set of Steiner points for each given point set. Computing an RMST requires a constant amount of time for nets with a finite number of pins. The RMST model is depicted in picture 1.1.

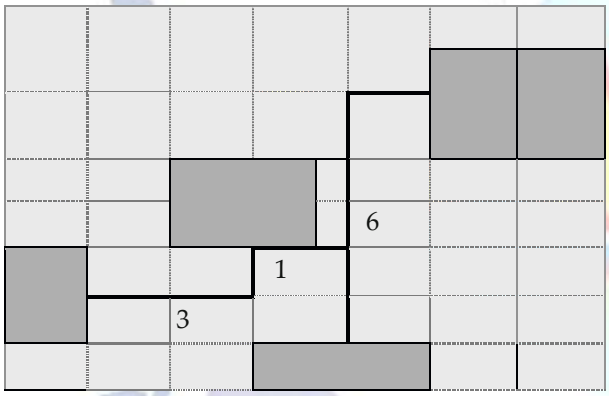

Figure1.2: Total wire length with net weights (weighted wire length)

Certain nets are prioritized above others based on their net weight.

$$L\,(P) = w\,(net)\,L\,(net) \quad (2)$$

is an estimation of the total weighted wire length for location P.

Where L(net) is the projected length of the net's wire and w(net) is its weight.

Utilizing mathematical methods like numerical analysis or linear programming, analytical placement minimises a specified target, such as wire length or circuit delay. These techniques frequently involve making specific assumptions, like that the objective function is differentiable or that placeable objects are treated as dimensionless points. For instance, it is typical to optimise quadratic wire length rather than linear wire length to make the calculation of partial derivatives easier. The cell placements must be moved further apart by specialised post-processing procedures in order to remove overlap when such algorithms place cells too near to one another.

Because it can be determined quickly and with reasonable accuracy, the half-perimeter wire length (HPWL) model is frequently employed. The smallest rectangle that a net with p pins can have as its bounding box the pin locations are included. Half of the enclosing box's perimeter is thought to be the length of the wire. This is identical to the rectilinear Steiner minimal tree for two- and three-pin nets (70–80% of all nets in most contemporary designs).

3. RESULTS AND FUTURE SCOPES:

The C language-based application is coded to encompass population chromosomes as well as selection, crossover, and mutation, with crossover probability and mutation probability both being equal to 0.5. The GCC compiler is then used to run it. The obtained Fitness Value is shown in Table 1 below.

Area total = 139169.000000

Table-1: Fitness value for various combinations

Combinations	Fitness Value
C1	12.22
C2	12.22
C3	24.31
C4	53.14
C5	59.41
C6	16.76
C7	16.76
C8	24.31

Table-1(a): Selection of parents with their Fitness value

Content	first parent	second parent
Fitness value	11.78	15.22

Table-1(b): Fitness value for off springs

Content	first offspring	second offspring
Fitness value	8.6	33.22

The fitness value for different parent pairings is given in Table 1. According to the Parallel Genetic Algorithm, this is the initialization phase (PGA). Following that, a parent pair is chosen based on how fit they are. Table 1 lists the chosen parent pair along with their fitness value (a). These will enable the Crossover process to occur, producing offspring. Depending on their fitness value, the best offspring are selected.

Table-2: Optimized Value

Benchmark	HPWL(mm)	Optimized HPWL(mm)	Area for 10 blocks	Optimized area
ISPD98	8	7	10438	10409

The Table-2 lists the optimal area and wirelength values for current VLSI placement utilising a parallel evolutionary method. The optimum value (HPWL) of 9.8mm is displayed in findings from [5]. This method provides the optimised value in contrast to that.

With TSVs (Through Silicon Via) present in contemporary integrated circuit chip layout, this optimization of space and wirelength will be carried out in the future.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

[1] J. W. Joyner, R. Venkatesan, P. Zarkesh-Ha, J. A. Davis, and J. D.Meindl, "Impact of three-dimensional architectures on interconnects in gigascale integration," IEEE Trans. on VLSI Systems, vol. 9, no. 6, pp. 922–928, Dec. 2001.

[2] A. Rahman and R. Reif, "System-level performance evaluation of three dimensional integrated circuits," IEEE Trans. on VLSI Systems, vol. 8,no. 6, pp. 671–678, Dec. 2000.

[3] R. Zhang, K. Roy, C.-K. Koh, and D. B. Janes, "Stochastic wire-length and delay distributions of 3-dimensional circuits," in Proc. of IEEE/ACM ICCAD, 2000, pp. 208–213.

[4] J. Cong, G. Luo, J. Wei, and Y. Zhang, "Thermal-aware 3D IC placement via transformation," in Proc. of ACM/IEEE ASPDAC, 2007, pp. 780–785.

[5] Wai-Kei Mak, "Rethinking the Wirelength Benefit of 3D Integration" Member, IEEE, and Chris Chu, Senior Member, IEEE

[6] Bazargan K, Kastner R, Sarrafzadeh M "Simulated annealing and greedy placement methods for Reconfigurable computing systems". IEEE Workshop on Rapid System Prototyping. Paris France, 2000: 38-43.

[7] M.-K. Hsu, Y.-W. Chang, and V. Balabanov, "TSV-aware analytical placement for 3-D IC designs," in Proc. ACM/IEEE Design Autom. Conf., 2011, pp. 664–669.

[8] Y.-L. Chuang, P.-W. Lee, and Y.-W. Chang, "Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs," Proceedings of the 2009 International Conference on Computer-Aided Design, pp.666-673, 2009.

[9] J. Cong and G. Luo, "Thermal-aware 3D placement," Springer Publishers, 2009.

[10] J. Cong and G. Luo, "Advances and challenges in 3D physical design,"IPSJ Transactions on System LSI Design Methodology, vol. 3, no. pp. 218, 2010.

[11] J. Cong and M. Xie, "A robust mixed-size legalization and detailed placement algorithm," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 8, pp. 1349-1362, Aug. 2008