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Stack IC Placement

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ABSTRACT

The layers of a 3D integrated circuit are stacked vertically utilizing Through Silicon Vias (TSVs), which ensures to extend integration density above Moore's law. In 3D IC, optimization plays a crucial role. In this paper, the analysis and optimization of wire-length and TSVs utilizing 3D IC placer and 3D IC optimizer are discussed. The outcomes are compared to the benchmark circuits used to optimize the system.

KEYWORDS: *Moore's law, 3D IC placer, IBM benchmark, optimizer.*

1. INTRODUCTION

In the semiconductor industries, three-dimensional integration of IC is becoming a critical concern. TSV optimization plays a crucial role. Numerous tools exist for the numbering and placement of TSVs, as well as for their optimization. Primarily offered are 3D IC Placer, optimizer, and hotspot tools. In general, 3D integration technologies can be divided into three categories: I 3D packaging, (ii) 3D TSV based integration (top-down, parallel integration), and (iii) 3D Monolithic integration (bottom-up, sequential integration).

A cross-sectional illustration of 3D IC is provided in the figure.

Integration in 3D IC is based on TSVs, which are used to create individual wafers in parallel and stack dies using TSVs.This technology has garnered significant industry and academic study and development in recent years. TSVs have multiple variations based on the fabrication process: (i) via-first method, (ii) via-middle approach, and (iii) via-last approach. In the via-first method, Through Silicon Vias (TSVs) are fabricated on a wafer before transistors and metal layers. The via-middle technique produces TSVs after constructing transistors but prior to constructing metal layers. The via-last approach creates TSVs after transistors and metal layers have been fabricated.

2. TSV NUMBERING AND LOCATION

Understanding the issues posed by 3D IC TSV when their location is defined and their total number is determined based on the number of connecting blocks in adjacent layers is referred to as this. TSVs must be kept in an area where interference is minimal[1]. Regarding placement, the positioning and numbering of Through Silicon vias are specified. The default identification of TSV locations is based on the distribution of white space. TSVs such as power TSV, ground TSV, and signal TSV have distinct site schemes. For each site plan, pre-planned TSV must be used to design nets.

Objective = min (alpha * cost_TSV * number_TSV + wirelength). (1)

Equation 1 indicates that the TSV cost function is determined for the purpose of TSV location. Adding TSV will reduce wire length, but will increase production costs. The aim is to accurately model the TSV cost and appropriately position the TSV in order to minimize the wire length. For the identification of site schemes, algorithms linked to lowering spanning trees, low cost, and nearby object search can be applied. Lastly, algorithms must be capable of reducing the wire length between linking blocks of different levels via TSV.

3. Analytical Placement

Optimization is the process of discovering the best or most effective solution to a problem. The 3D IC Placer and 3D IC optimizer are utilized to optimize TSVs in this instance. Micro Magic, Inc. has introduced 3D IC placer. After the layer assignment, the Through Silicon Vias may be placed. Once the layer is assigned, Hotspot and Keep/Knock Out Zone (KOZ) can be identified during 3D floor planning or vertically stacked IC deployment [2]. TSV insertions and net splitting can also be implemented using the minimal spanning tree (MST), the Steiner tree method, or a 3D router that is optimized for the task.

Minimize

$\sum (1+Ye)\ (WL(e)+\alpha TSV.tsv(e)$ (2)

Subject to

$\sum$ Overlap (binm, n,k,vi)<=Wbin.hbin

After Through Silicon Via (TSV) insertion and net splitting, a vertically stacked IC placement with a fixed layer assignment is conducted to optimize the arrangement of blocks and TSVs, thereby decreasing the wire length and temperature. When the temperature is optimized, thermally aware issues can be managed. The equation (2) states that minimizing the total number of TSVs and wire length maximizes the 3D IC's area indirectly. The standard-cell IC arrangement has the same aspect ratio for each block in the circuit, whereas the macro cell IC placement has variable aspect ratios for each block. Our 3D analytical placer functions for both standard and large cell IC placement. A multiple-step size scheme is devised to efficiently and effectively manage mixed-size net-lists. To prevent illegal solutions, we would like to start the analytical 3D placer with fixed huge macros.

The following diagram illustrates the 3D Placer outcomes for the IBM placement benchmark.

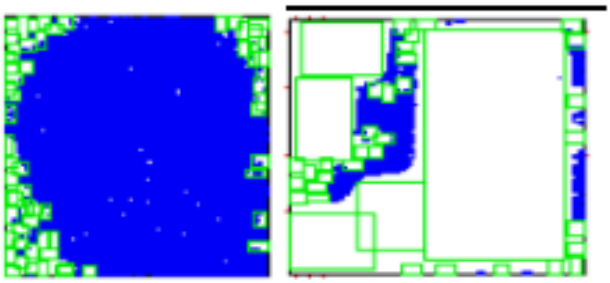

Fig : IBM 07,08 benchmarks done with analytical placement.

These outputs provide a clear perspective of the 3D placer's global placements for the various IBM Placement benchmark files. The benchmark includes the following files: area (are) file, net file, netD file, and placement (pl) file.TSV numbering and total number of wire length are calculated using the geometric mean of TSV numbering and total number of wire length, which is tabulated and shown in table 1.

Table 1: Results

Circuits	2-Leve1		
	WL $X10^7$	W L $X10^7$	#TSV $X10^3$
ibm07	1 .47	1.71	18.67
ibm08	2.69	2.99	36.96
Geometric mean	1.21	1.34	0.45

4. CONCLUSION

This 3D IC Placer output was implemented with a Linux operating system background. Thus, the total number of wire-length and TSVs for various IBM placement benchmarks was determined. Future optimization of this work can consider the restrictions of Stress and temperature.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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