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Area Efficient Wallace Tree Encoder for Flash ADC

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ABSTRACT

The area-efficient Wallace Tree encoder is described in the proposed work. Flash analogue to digital converter uses this encoder to translate thermometer code to binary code (ADC). The quickest analogue to digital converter is the parallel ADC, also referred to as flash ADC. The best option for high-speed applications is flash ADC. It is made up of an encoder circuit, a comparator, and a resistor ladder. A thermometer code is the comparator's output. It needs to be converted using an appropriate encoder to the appropriate binary code. When designing low power flash ADC, lowering encoder power dissipation is a top priority. In terms of bubble error correction, Wallace tree encoder performs best, but it uses more energy. In this paper, a suitable full adder design and an efficient Wallace tree encoder are proposed. Using gate diffusion input technique and pass transistor logic (PTL), a full adder is designed. Therefore, low power flash ADC design is better suited to it. There are 110 transistors in the suggested design. Utilizing the EDA tool CADENCE 5.1.0, the circuit is designed.

KEYWORDS: Wallace Tree encoder; bubble error; hybrid full adder; pass transistor logic ; gate diffusion input technique; area efficient.

1. INTRODUCTION

The development of wireless technology ushers in a wire-free era. Digital signal processing is used by the majority of wireless communication systems to transmit and receive information. Signals in the physical world are analogue. The analogue signal is transformed to digital form for easier processing due to the analogue signal's processing complexity. Since integrated circuit technology has advanced over the past ten years, the field of digital signal processors has developed quickly[1,2,3,4]. Additionally, digital processing has the benefit of being more noise-resistant. Thus, the analog-to-digital converter serves as an interface between the digital signal processing system and analogue signals. High speed low resolution analog-to-digital converters are in high demand due to the wireless communication networks' ongoing efforts to increase their speed[5]. Because of its well-known parallel design, flash ADC is employed for high-speed ADC applications. According to Abualsaud[6], Fig. 1 depicts the fundamental block diagram of a flash ADC, which consists of a reference ladder, comparators, and an encoder.

The comparators are coupled to each reference voltage in this arrangement. The output of the comparators, which are 0s and 1s bit streams that constitute thermometer code, is supplied into the encoder for ADC processing. The reference ladder creates the reference voltage that is compared with the input. Using a Wallace tree encoder, the bit stream is transformed into binary output patterns throughbubble error correction logic[7]. The outputs of the comparators must all be synchronized in order to achieve a high conversion rate. The number of components increases exponentially as the resolution of

the ADC is increased, which further expands the area and power consumption. For *N*-bit flash ADC 2^N resistors are required to generate a reference voltage for the 2^N- 1 comparators. The output of the comparator is a bit-string called thermometer code. A simple 2^N- 1: *N* encoder will convert thermometer code to binary code.

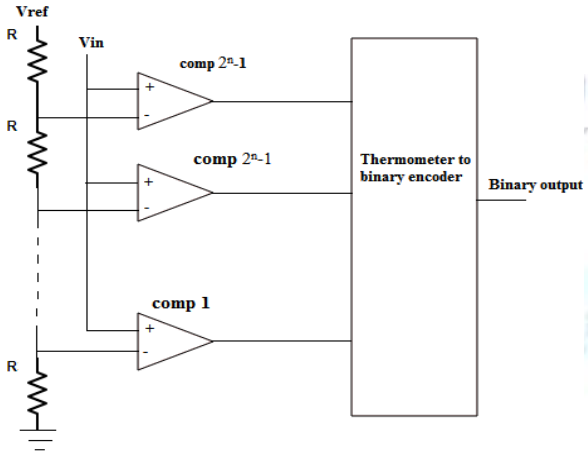

Fig.1 Basic block diagram of flash ADC[1]

The speed of the converter plays a crucial role in the design of flash ADC. Wallace tree counts the number of 1's available in the output of the comparators[8]. This technique offers global bubble error correction/suppression unlike the fat tree encoder and ROM encoder where bubble errors are usually handled locally using three or higher input NAND gates[9,10]. But it consumes more power. The basic building block of the Wallace tree encoder is full adder cell. The total number of full adders utilized in an encoder of N bit is $2^N - N - 1$.

The Wallace Tree encoder's primary component, the full adder, has a significant impact on the system's overall performance. Therefore, one of the main research areas is to improve the performance of 1-bit full adders. Therefore, the Wallace tree encoder performs better thanks to the whole adder cell's optimal design. In order to accomplish area, a modified full adder is used in this study in place of the traditional full adder.Section II introduce the architecture of existing work. Section III presents proposed Wallace Tree encoder architecture and section IV bring into contact with simulation design using CADANCE tool and finally in section V results are compared followed by conclusion in section VI.

2. EXISTING WALLACE TREE ENCODER

One of the quickest ways to transform analogue information into digital information is via a flash ADC. Encoder is the primary part of an ADC. It comprises of a full adder in the case of Wallace Tree encoder. Fig. 2 displays a block diagram of the 15:4 Wallace tree encoder. It has 11 complete adders with 15 inputs (thermometer code) and the outputs b3, b2,b1 and b0 in binary.

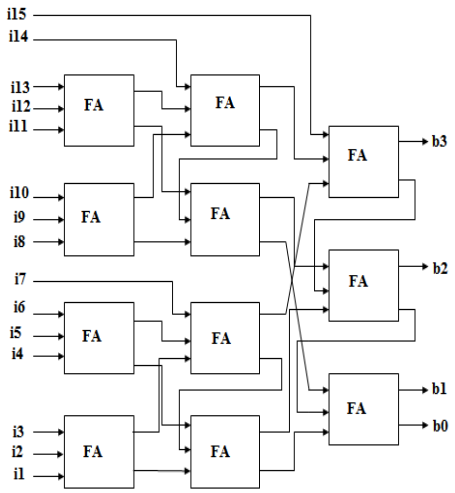

Fig.2 Block diagram representation of 15:4 Wallace tree encoder[1]

The Wallace tree encoder's ability to pass each input through an equal number of complete adders is one of its key features. Therefore, all of the inputs' propagation delays are effectively the same. The speed of the encoder's functioning can be enhanced by installing pipelining. However, the current Wallace Tree encoder, which uses a conventional full adder with 28 transistors, has high power dissipation. Consequently, the Wallace Tree encoder has a total of 308 transistors.

3. PROPOSED WALLACE TREE ENCODER

The conversion of the thermometer code to binary code is one of the difficulties in a high-speed flash ADC design[13]. Wallace Tree Encoder offers good results at any resolution and is adaptable. A modification to the full adder's design reduces the area of the Wallace tree encoder. The proposed full adder has only 10 transistors, which reduces the number of transistors and lowers power dissipation. Modified full adder is shown in Fig. 3. In order to enhance the performance of a 1-bit hybrid full adder circuit, hybrid logic style takes advantage of the features of currently used standard logic designs. Multiple logic styles are used in hybrid logic design styles.

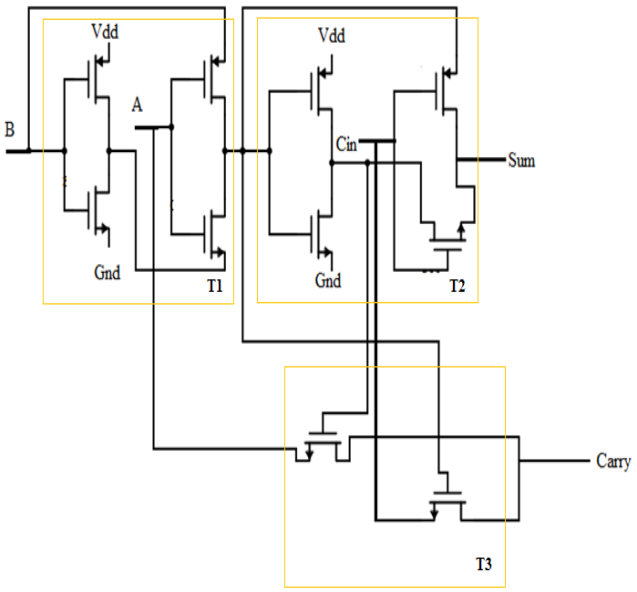

Fig. 3 Modified full adder used in Wallace Tree encoder

The module T1, T2 and T3 consists of GDI XOR, PTL XOR, PTL MUX. Module T1 is the GDI XOR. Module T2 and T3 is the PTL XOR and PTL MUX respectively. Module T1 and T2 are responsible for the generation of sum of full adder. Carry output is generated by the help of module T3. In order to reduce the area proposed full adder replaces conventional full adder in Wallace Tree encoder. Fig. 4 shows the proposed Wallace Tree encoder with modified hybrid full adder.

4. SIMULATION RESULTS

The proposed circuit is designed using CADENCE 5.0.1 EDA tool and simulated using spectre virtuoso. Design of full adder is changed to block, then by these full adder block designed the proposed Wallace Tree encoder. In proposed Wallace Tree encoder design there is no degradation of output voltage. This encoder is suitable for flash ADC in the field of digital communication.

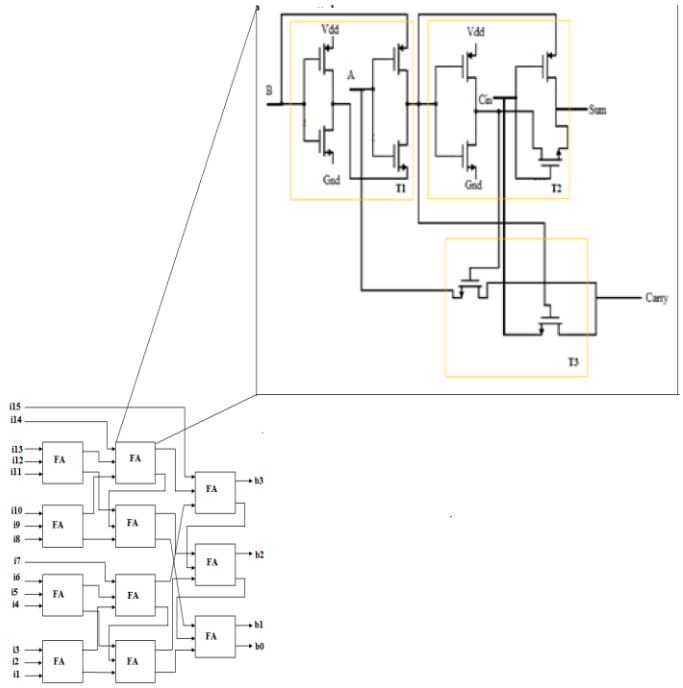

Fig. 4 Proposed Wallace Tree encoder with modified hybrid full adder

Fig. 5 shows the schematic diagram of proposed design in cadence.

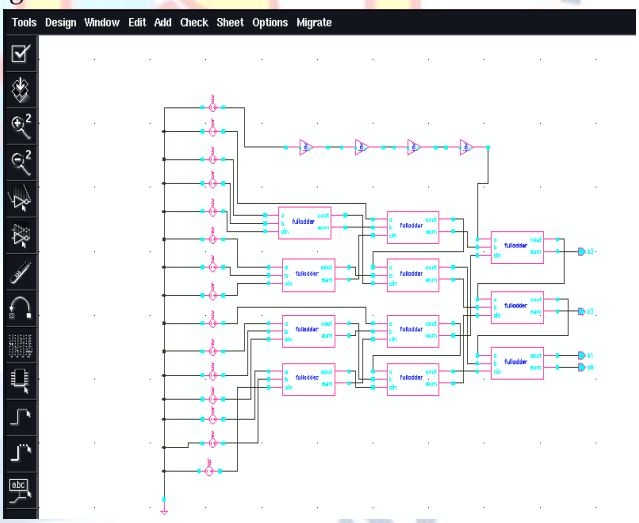

Fig.5 Schematic diagram of proposed Wallace Tree encoder

Fig. 6 shows the transient response of proposed Wallace Tree encoder. It shows 15 inputs (thermometer code) and its corresponding binary outputs b3,b2,b1,b0.

Fig.6 Transient Response of proposed Wallace Tree encoder

PERFORMANCE SUMMARY

TABLE I. COMPARISON OF DIFFERENT ENCODERS

Encoders	Wallace Tree encoder[1] (2019)	Heterogenous encoder[2] (2017)	MUX based encoder[2] (2018)	ROM based encoder[3] (2018)	Fat Tree encoder[3] (2018)	Proposed Wallace Tree encoder
Transistor count	308	196	132	126	156	110

Table I shows the comparison of different encoders. Transistor counts reduced to 110 with existing Wallace Tree encoder.

5. CONCLUSION

The proposed work describes an efficient Wallace Tree encoder using a complete adder that is designed properly. For use with flash ADC, this encoder transforms thermometer code into binary code. The quickest analogue to digital converter is the parallel ADC, sometimes referred to as flash ADC. The Wallace tree encoder performs the best in terms of correcting bubble errors, but it uses more space and energy. Circuit complexity is reduced by the proposed Wallace Tree encoder with modified hybrid full adders. Spectre virtuoso is used to simulate the proposed circuit once it has been constructed using the EDA programme CADENCE 5.0.1.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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