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Efficient and Low Density Based Binary Counters and Compressors

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ABSTRACT

To perform the summation of multiple operands at the same time is the critical path in various DSP units. To speed up the summation exact/approximate compressors are necessary. In this paper, we present a novel method of efficient and low density based binary counters and compressors and also show the comparison of Exact (4:2) compressor and Approximate (4:2) compressor with one error using the sorting network which comprises basic logic gate along with multiple input and output. The major objective is to reduce the power consumption. This was implemented by using Xilinx Vivado 18.1.

Vivado Design Suite is software suite produced by Xilinx for synthesis and analysis of hardware description language (HDL) designs. Vivado includes the in-built logic simulator. Specifically the Xilinx Vivado compiler provides a programming for optimization of C and C++ programs. Vivado simulator is a mixed language simulator and can handle simulation models in both VHDL and Verilog.

Keywords: Exact and approximate compressor, sorting network, Lookup table, Power Dissipation.

1.INTRODUCTION

The summation of multiple operands is widely used in many digital signal processing units and is one of the critical paths. One of the methods is by using the compressor combined by full adder.

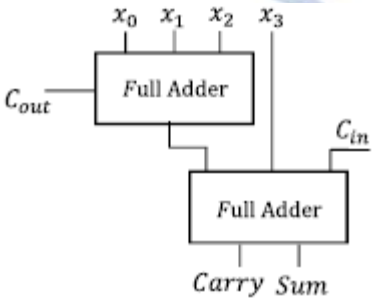

Fig 1:(4:2) compressor by full adders.

The basic multiplier circuit adds all the small products with the Wallace tree structure where this method use full adders as counters to accelerate the summation. For example, a basic (7, 3) counter structure combined with full adders is shown in fig2. Also the compressors compress n rows into 2 rows by considering the carry bits between adjacent columns which are still in the frame work of full adders. The counters compress n rows into _log2n_ rows.

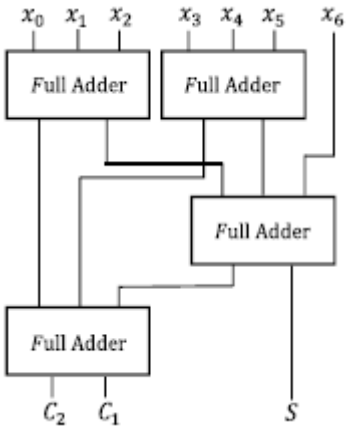

Fig 2 : (7,3) counter combined by full adders.

These were implemented using sorting network which is an efficient parallel hardware network utilized for data sorting. The famous zero-one principle says that if a sorting network works correctly when each input is drawn from the set {0,1}, then it works correctly on arbitrary input numbers.

The first step in our construction of an efficient sorting network is to construct a comparison network that can sort any bitonic sequence a sequence that either monotonically increases and then monotonically decreases, or else monotonically decreases and then monotonically increases. Here is the comparison network and its characteristics. A comparison network is comprised solely of wires and comparators. A basic comparator is a device with 2 inputs x and y and 2 outputs x' and y' as shown in below figure

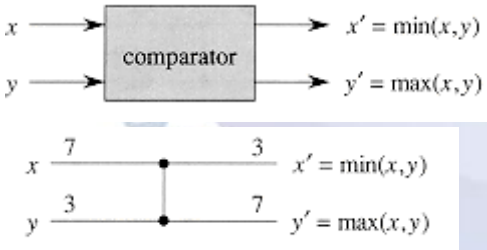

Fig3: Basic comparison network with single vertical line.

2. LITERATURE SURVEY

The compressor performance is determined by many factors like power consumed, chip area including its speed. Numbers of methods are used to increase the performance of the compressor like binary multiplier, bit multiplier, sorting network, half adder, full adder, Wallace tree. In this paper we choose to work using sorting network.

EXACT (4:2) COMPRESSORS

The (4:2) compressor has the logical function similar to the compressor combined by the adders. In this project to construct a high speed (4:2) compressor, we used 4 way sorting network which functions as shown in fig below,

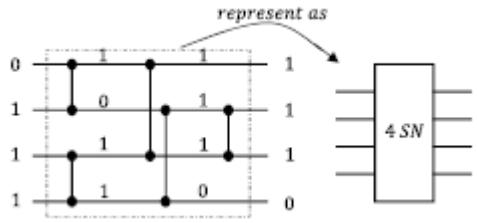

Fig4: four-way sorting networks.

In 4 way sorting network we need 3 stages to sort 4 inputs where the last stage of the 4 way sorting network sorts the two data in the middle which means the data at the top and the data at bottom are maximum and minimum of the four data respectively

The first two stages of the sorting network are shown and explained in fig: as "half-sort" and the results are denoted as A, B, C, D. since A is maximum data and D is minimum data the sequence [A, B, D] is completely sorted.

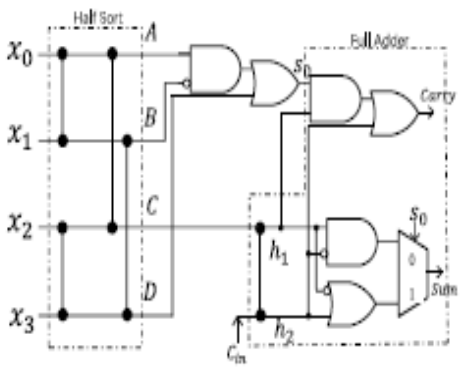

Fig5: Proposed exact (4:2) compressor.

The summation of A, B, and D can be calculated with the following equation:

$s_0 = (A \,\&\, \bar{B}) \mid D$

$C_{out} = B.$

The summation of s_0, C_{in} and C is calculated with full adder.

$h_1 = C \mid C_{in}$

$h_2 = C \,\&\, C_{in}$

$Carry = (s_0 \,\&\, h_1) \mid h_2$

$Sum = s_0 ? (\bar{h}_1 \mid h_2) : (h_1 \,\&\, \bar{h}_2)$

APPROXIMATE (4:2) COMPRESSORS:

We constructed it using the sorting network where D is one of the outputs of 4SN and it is the minimum one. By discarding D gets the below equations.

$Carry = A \& h_1$

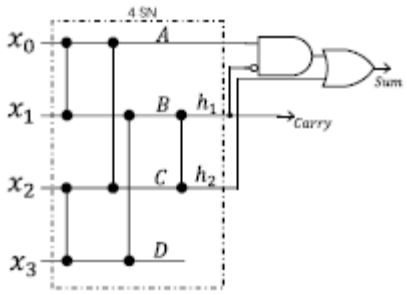

Fig6: Approximate (4:2) compressor with one error.

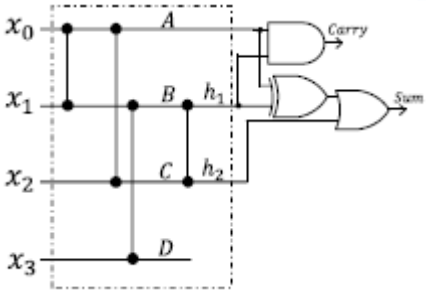

Fig7: Approximate (4:2) compressor with two errors.

To construct a faster approximate (4:2) compressor a sorter is discarded in 4SN. Although it is not confirm that the sequence [A, h1, h2] is sorted completely, we consider it is sorted to correct the deviation introduced by incomplete sorting.

A Lookup table is an array of data which maps input values to output values and then approximating a mathematical function. Given a set of input values, a lookup operation retrieves the respective output values from the table.

3. RESULTS

The fig8 and fig9 shows the simalation results of the exact (4:2) compressor and approximate (4:2) compressor with one error respectively.

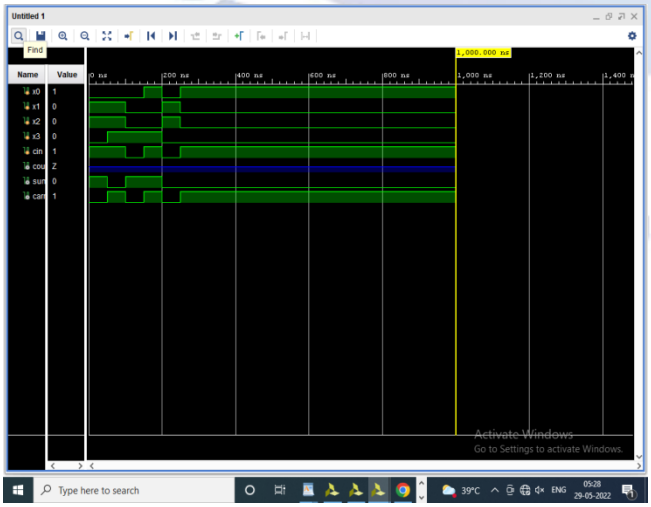

Fig8: Exact (4:2) Compressor waveform

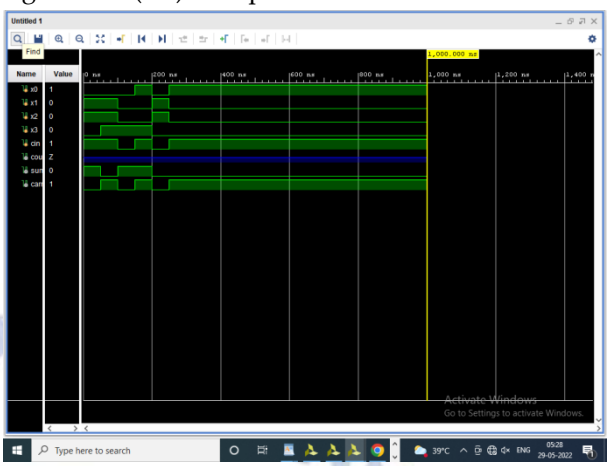

Fig9: Approximate (4:2) Compressor with one error waveform.

TYPE	Power Dissipation (μW)	LUT
Exact(4:2) Compressor	1.497	1
Approximate compressor	1.107	2

4. CONCLUSION

Both the efficient exact (4:2) compressor using full adder and approximate (4:2) compressor with one error using sorting network are compared. Exact compressor requires a bit more power when compared to approximate compressor with two lookup table whereas exact compressor has only one lookup table. Overall Exact (4:2) compressor have simple design when compared to approximate compressor.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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