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VLSI Implementation for High Performance Encoder of Flash ADC

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ABSTRACT

The fastest analog to digital converter, commonly known as parallel ADC, is the flash ADC. It is perfect for applications that require a lot of bandwidth. A resistor ladder, comparator, and encoder circuit make up the circuit. The comparator's output is a thermometer code. It must be translated to binary code using the appropriate encoder. When building a low-power Flash ADC, reducing encoder power consumption is a primary concern. The Wallace tree encoder and MUX based encoder, are compared in this research. The Wallace tree encoder can overcome the problem of bubble error but it consumes more power. The multiplexer based encoder is more power efficient and simple in design.So, it is more suitable for low power flash ADC. These encoders are implemented by using Xilinx Vivado 18.1

Keywords – Flash type ADC,Parallel ADC, thermometer code, encoder, power dissipation, Low power, High speed.

1.INTRODUCTION

A flash type ADC, often known as a parallel A/D converter, is the simplest to comprehend. It is made up of several comparators, each of which compares the input signal to a different reference voltage. The comparator outputs are connected to the priority encoder circuit's inputs, resulting in a binary output. The Fig1 illustration shows a 3-bit flash ADC circuit:

Vref is a stable reference voltage provided by a precision voltage regulator, which is not depicted in the schematic, as part of the converter circuit. The comparator outputs will sequentially saturate to a high state as the analogue input voltage surpasses the reference value at each comparator. The priority encoder creates a binary number from the highest-order active input while ignoring all other active inputs.

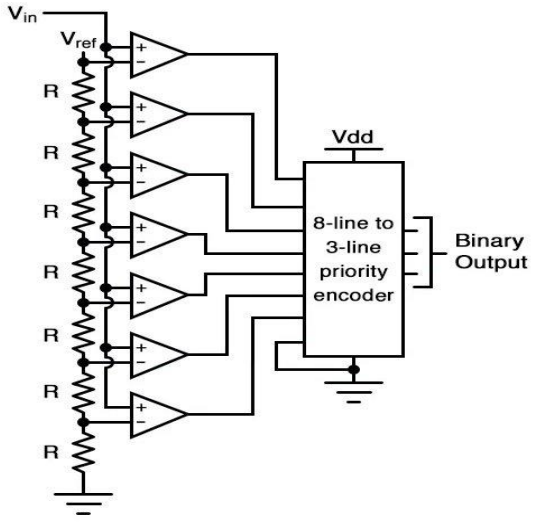


Fig 1: 3-bit flash ADC circuit

Because of the nature of sequential comparator output states (each comparator saturating "high" in order from lowest to highest), the same "highest-order-input

selection" effect may be achieved using a group of Exclusive-OR gates, allowing the use of a simpler, non-priority encoder.

Seven comparators are required for this three-bit flash ADC. A four-bit version would necessitate the use of 15 comparators. The number of required comparators doubles for each additional output bit.

When realise that eight bits is typically considered the minimum for any workable ADC (255 comparators are required!), the flash approach rapidly reveals its flaw. Another feature of the flash converter that is often ignored is its capacity to produce non-linear output.

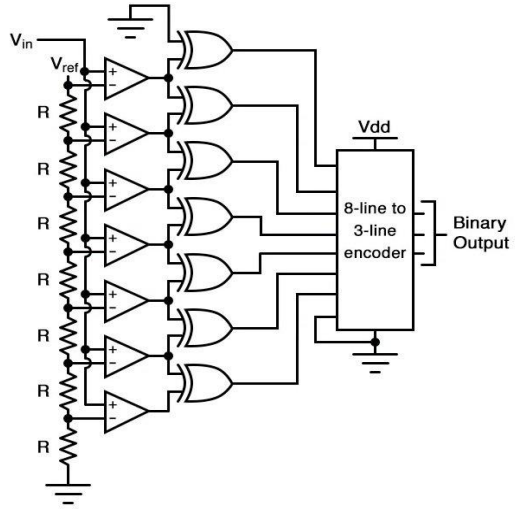


Fig 2: 3-bit flash ADC circuit using XOR

Each successive binary count in the reference voltage divider network indicates the same amount of analogue signal increase, resulting in a proportionate response. The resistor values in the divider network can, however, be set non-equal for particular applications. This gives the ADC a nonlinear response to the analogue input signal that is unique to it. With only a few component value changes, no other ADC design can provide this signal-conditioning behaviour.

2. LITERATURE SURVEY

The ADC's performance is determined by a number of factors, including its speed, power consumption, chip area, and aperture jitter. Various strategies are used to improve the efficiency of the Flash ADC.A typical the over-range is reduced using a termination circuit. As a result, electricity usage is lowered [1].

A supplementary average value technique was presented in which the input signal is pre-processed before being compared to a predetermined voltage reference level in order to simplify the comparator architecture [2].

MUX-based circuit for thermometer to binary conversion that can correct bubble errors. These bubble error correction circuit correct only first order bubble error[3].

The standard CMOS full adder is resistant to voltage scaling and transistor sizing.

High input capacitance and the need for buffers are disadvantages [4].

ENCODER

An encoder is a machine that turns one type of code into another. The process of encoding is the inverse of decoding. An encoder has a total of "m" input lines and "n" output lines. It generates a "n bit binary code" for the digital input number.

WALLACE TREE ENCODER

A wallace tree encoder is constructed by using blocks of full adder as shown in Fig 3. The number of adders required for the construction of encoder is done by using the following formula

$XN = i{-}1\ .2\hat{}(N{-}i)Ni{=}1$

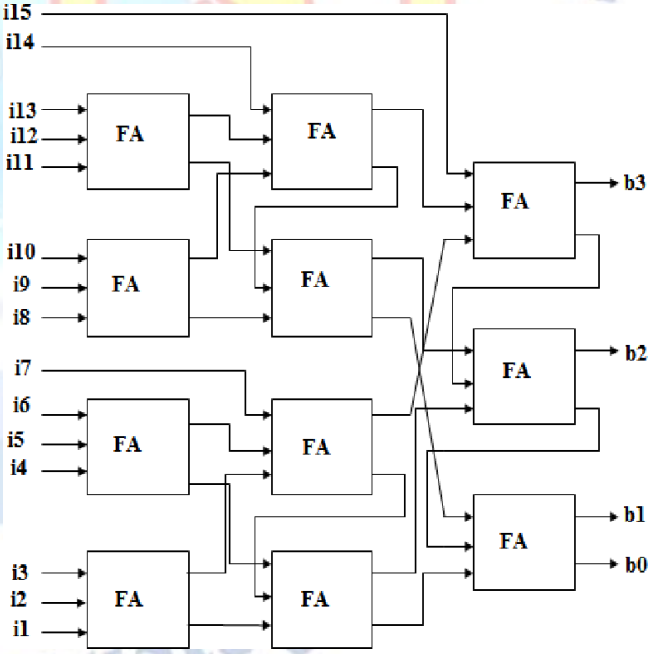


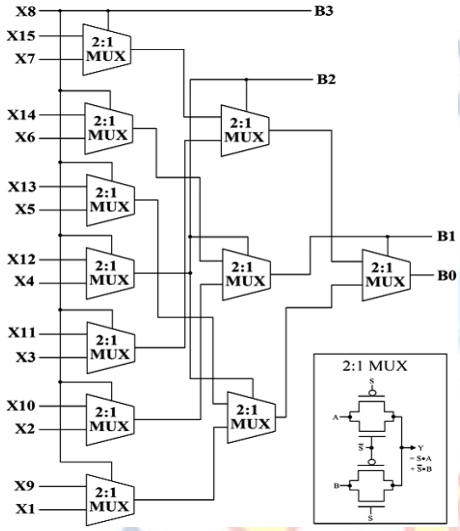
Fig3: Wallace tree encoder

Each input's and output's propagation delays are effectively controlled and identical. As a result, the existing design's speed of operation is adequate. This design employs a traditional full adder, with each full adder containing 28 transistors. The entire adder Wallace design tree encoder requires a total of 308 transistors, therefore the current circuit consumes more energy.

As it reduces the problem of occurrence of bubble error but it increases the problem of area when number of inputs are increased. Hence the consumption of power and delay must be increased.

MULTIPLEXER BASED ENCODER

A Multiplexer based encoder is easy to construct because of direct form of encoding by 2:1 using multiplexers. fig.4 shows the 15:4multiplexer based encoder.



The output of a N bit flash ADC thermometer at level 2N-1 is the MSB bit. The middle digit of the thermometer code is the most significant bit (MSB) with this sort of encoder. If the 2N-1 (middle digit) is one, we choose the upper half; otherwise, we choose the lower half. The MSB-1 bit is determined in the same way as MSB was determined from the specified scale. This technique was repeated until all bits of output were discovered.For high resolution, the multiplexer-based encoder structure was enlarged.

It converts the thermometer code into gray code and then converts it into binary code. The complexity of designing the circuit is less compared with other type of encoder. Speed of operation also good.

3 RESULTS

The figure5 shows the simulation output of wallace tree encoder

The figure6 shows the simulation output of Multiplexer based encoder

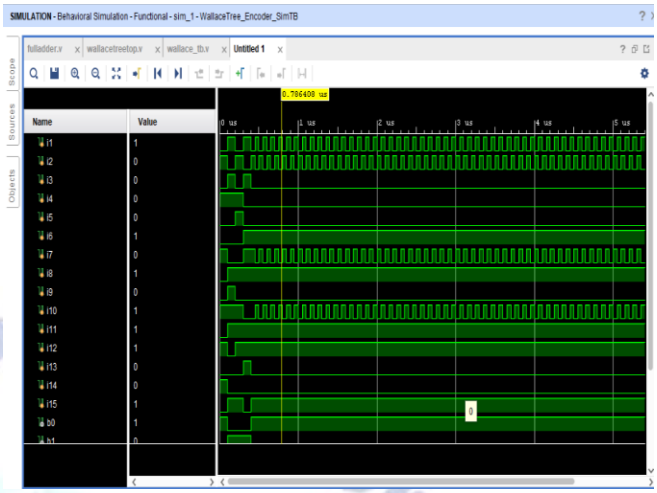


Fig5: Wallace tree encoder waveforms

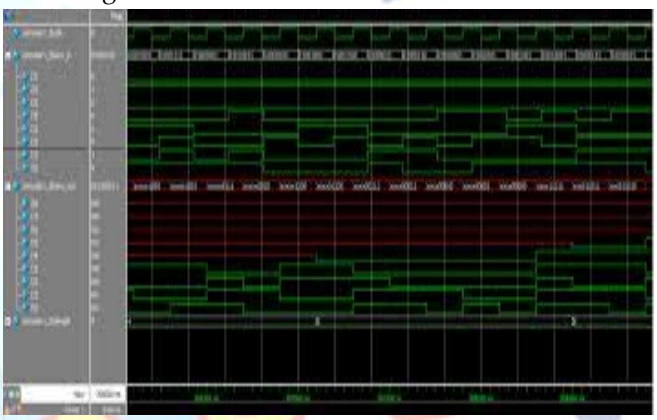


Fig6: MUX based encoder waveforms

Type e of Encoder	Power Dissipation (μW)	Delay (ns)	PDP(fJ)
Wallace Tree Encoder	6.077	0.1346	58.1
Multiplexer based encoder	2.41	0.1325	0.0058

4 CONCLUSION

Both the encoders i.e Wallace tree encoder and Mux based encoder are compared. Wallace tree encoder is able to controller the bubble errors but it requires more power where as the Mux based encoder is more power efficient and simple to design. Hence a Mux based encoder is more suitable for the practical applications of the low power flash type ADC

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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