IJMTST is UGC Approved Journal with Journal Id: 43137

International Journal for Modern Trends in Science and Technology, 8(S05):35-45, 2022

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST08S0508
Available online at: https://www.ijmtst.com/vol8si05.html

Increasing the Power Efficiency of Radix-4 Booth Multiplier with Pre-Encoded Mechanism

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To Cite this Article
G.Anantha Lakshmi, G.S.P.Prem Kumar, T.Charan Sai, A.Jayasree and G.Srihari. Increasing the Power Efficiency of Radix-4 Booth Multiplier with Pre-Encoded Mechanism. International Journal for Modern Trends in Science and Technology 2022, 8(S05), pp. 35-45. https://doi.org/10.46501/IJMTST08S0508

Article Info
Received: 26 April 2022; Accepted: 24 May 2022; Published: 30 May 2022.

ABSTRACT

The radix-4 Booth algorithm is widely used to improve the performance of multiplier as it can reduce the number of partial products by half. As we know, numerous additional encoders and decoders would cause the power consumption of the Booth multiplier to be considerable. In this paper, Booth pre-encoded mechanism is proposed to reduce the power consumption of the Booth multiplier. The proposed design can effectively reduce the power of the Booth multiplier dissipated in the redundant activities by disabling the Booth encoders and decoders from unnecessary working. Particularly, since the control signals are generate dearlyat the pipeline input register before the multiplier, the performance of our design is better than the traditional Booth multiplier. Based on the TSMC 40nm technology, the simulation results show that the proposed pre-encoded mechanism can reduce the dynamic and static power by 45%and65%, respectively, compared to the traditional 16-bit radix-4 Booth multiplier.As we compare to the previous designs,the proposed design has lower power consumption. Even compared to the approximate design, the proposed design has better power efficiency and can provide the exact products.

Keywords: Booth algorithm, low power multiplier, power efficiency, partial product, radix-4Booth multiplier

1.INTRODUCTION

Many digital signal processing (DSP) and machine learning applications are heavily dominated by multiplication e.g., more than 90% convolutional neural networks (CNN) computations are occupied by multiply-accumulate (MAC) operations .Multiplier is an important component in various hardware platforms. The conventional multiplication includes three major phases.Two inputs (multiplier and multiplicand) are multiplied to generate the partial products (PPs). Reducing the PPs' matrix into two rows by partial product reduction schemes The final carry propagated addition of the remaining two rows of PPs.The second phase plays a significant role in power consumption, cost, and overall performance. Then, the radix-4 Booth algorithm can improve its performance of multiplication as the radix-4 Booth multiplier can reduce the number of PP rows by half.

The authors provided a simple and intuitive encoding/decoding method to implement the radix-4 Booth algorithm; reference provided a modified sign extension structure to reduce the cost and to improve performance. In, the author found that the traditional radix4 Booth implementations may result in unnecessary glitches of PPs. Thus, the proposed the glitch-free Booth encoder and partial product generator to eliminate the unnecessary glitches of the radix-4 Booth multiplier.These traditional designs still suffer from high

power consumption and high cost of Booth encoders and decoders. Thus, the proposed a high performance and low cost radix-4 Booth decoder. The also keeps the advantage of race-free and its cost is less. To reduce the glitches in the second phase of multiplication. In order to reduce the cost of the Booth encoder and decoder, the authors proposed automatic Speaker recognition ASR as a hybrid biometric recognition approach and it has two components of the physical one related to the formation of the vocal apparatus, and the behavioral component of pertinent to the mood of the speaker just in the recording. There are several approaches to ASR based on features, vector quantization, score normalization, pattern matching, etc., and we propose text independent ASR system using Machine Learning based on Mel-Frequency Cestrum Coefficients (MFCC) and Gaussian Mixture Models (GMM). This model parameters are estimated with the maximum similarity ovulation use of the Expectation and Maximization (EM) algorithm novel modified Booth encoder (NMBE) scheme that is based on the pass transistor logic (PTL). Some of the error-tolerant applications, the approximate circuits can be employed to achieve low power, low circuit complexity, and high performance. The traditional radix-8 Booth algorithm can generate fewer PPs than the radix-4 Booth algorithm, but it needs additional adders to process the operation of odd multiples of the multiplicand. Therefore, the approximate 2-bit adder was proposed to generate the triple multiplicand with no carry propagation to improve the performance.The approximate radix4 Booth multipliers were proposed by using their approximate Booth encoders and approximate Wallace tree structure.Three approximation techniques for the radix-4 Booth multiplier were proposed and these designs can reduce the logic complexity of the PP generator. One specific feature of the radix-4 Booth algorithm is that when the continuous three bits of multiplier Y (y2i+1, y2i , y2i−1) have the same values, the corresponding PPs will be 0. This feature inspired us to find the ''0X'' case earlier to reduce the unnecessary switching activities of the radix-4 Booth encoders and decoders. Thus, we propose the pre-encoded scheme to detect the ''0X'' case before every multiplication. When the ''0X'' case occurs, the proposed pre-encoder will turn off the Booth encoders and decoders to save power, and set the corresponding PPs to 0 directly before the starting of multiplication. The simulation results show that the proposed design outperforms these designs in terms of transistor count, delay, and power consumption. Section II reviews the traditional radix-4 Booth multiplier and the related works. Section III describes the low power radix4 Booth multiplier with pre-encoded mechanism in detail. Section IV shows the simulation results of the proposed design.

2. TRADITIONAL RADIX-4 BOOTH MULTIPLIER AND RELATED WORKS :

Multiplication is a basic arithmetic operation; many DSP and machine learning applications are highly multiply-intensive. Therefore, the power consumption and performance issues of the multiplier are important. However, the traditional array multiplier generates a lot of PPs (n × n multiplication has n PP rows) and accumulates all PPs to get the final product; it consumes huge power and is not power efficiency. Then, the Booth algorithm (radix-2 Booth algorithm) has been proposed to improve the performance of the multiplication; the radix-4 Booth algorithm (also called modified Booth algorithm) [24] can reduce the number of PP rows by half to facilitate the multiplication. Here,we introduce the traditional radix-4 Booth algorithm and the related works.

Radix-4 Booth Algorithm:

y(2i+1)	y(2i)	y(2i-1)	M(i)	Operation on X
0	0	0	0	0X
0	0	1	+1	+1X
0	1	0	+1	+1X
0	1	1	+2	+2X
1	0	0	-2	-2X
1	0	1	-1	-1X
1	1	0	-1	-1X
1	1	1	0	0X

A. **TRADITIONAL RADIX-4 BOOTH ALGORITHM :**The radix-4 Booth algorithm method is used to improve the performance of multiplication and applies to two's complement operands. The radix-4 Booth algorithm partitions the multiplier Y (yn−1yn−2 . . . y0) into overlapping groups of contiguous three bits. Each group is encoded and then decoded with multiplicand X (xn−1xn−2. . . x0) to generate the corresponding PPs. The n-bit multiplication of radix-4 Booth algorithm can be expressed as follows:

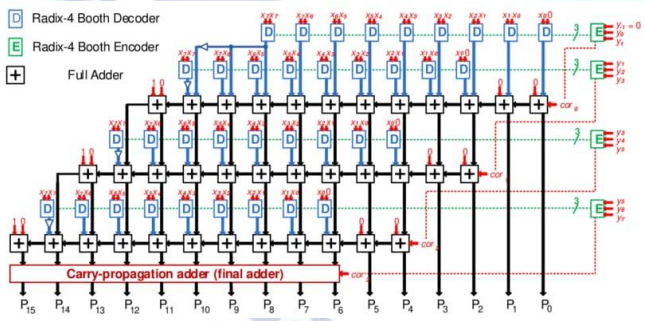
$$X\times Y = X\times(-y_{n-1}2^{n-1} + \sum_{i=0}^{n-2} y_i 2^i)$$
$$= X\times\sum_{i=0}^{(n/2)-1}(-2y_{2i} + 1 + y_{2i} + y_{2i} - 1)2^{2i}$$
$$= X\times\sum_{i=0}^{(n/2)-1} Mi\,2^{2i}$$

$= \sum_{i=0}^{(n/2)-1} Mi2^{2i}X(1)$

multiplicand X and multiplier Y are n bit two's complement numbers. According to the continuous three bits of multiplier Y (y2i+1, y2i , y2i−1), the radix-4 Booth algorithm can generate the corresponding coefficient Mi . The coefficient Mi has five possible values (±1, ±2, or 0) as shown.,the radix-4 Booth algorithm can reduce the number of PPs rows by half, and one specific feature is that the corresponding PPs will be 0s when the continuous three bits of multiplier Y (y2i+1, y2i , y2i−1) (Mi = 0) have the same values. As shown in Table 1, the continuous three bits of multiplier Y (y2i+1, y2i , y2i−1) have the same values that indicate the ''0X'' case. Notice that y−1 is always 0 when i equals to 0. Although the radix-4 Booth algorithm can reduce the number of PPs, the cost of the radix-4 Booth multiplier is

still high.A modified sign extension structure which can reduce the number of PPs and the cost further. Fig. 1 shows the traditional radix-4 Booth multiplier with the modified sign extension structure. Each PP row has one Booth encoder and n + 1 Booth decoders. Booth encoders and decoders generate the PPs; full adders and carry-propagation adder add all PPs to get the final product. However, the unnecessary glitches and switching activities occur in the traditional radix-4 Booth multiplier because of

The traditional 8*8 radix-4 Booth multiplier:



unbalanced signal paths of radix-4 Booth encoders and decoders,which leads to high power consumption,where overall power consumption of CMOS can be defined as,

P = aCV2 dd f +Vdd Ileakage

The first and second terms are dynamic and static power consumption, respectively. Here a is the switching activity parameter, C is the total capacitance load, Vdd is the supply voltage, f is the operating frequency, and I is the leakage currents and the power consumption can be reduced by minimizing the switching activities.

B. RELATED WORKS The radix-4 Booth encoder and decoder is the most common implementation of the radix-4 Booth algorithm, and the authors provided more compact implementations. However, the author found these designs have unnecessary glitches caused on PPs. Therefore, the glitch-free Booth encoder and partial product generator (decoder) have proposed to reduce the unnecessary glitches. The propagation delay from inputs X and Y to PP is only two units (one XOR/XNOR and the complex gate for output), and all paths almost have the same propagation delay.The authors proposed a high performance and low cost radix-4 Booth decoder that also keeps the advantage of race-free. Especially, the cost is less.The authors proposed a neg/two/one-nf (nf means neg-first) generator as shown in Fig. 2, and the neg-first radix-4 Booth algorithm is shown in Table 2. The neg first radix-4 Booth algorithm is the three-signal scheme; signals one-i , two-i , and neg-i can indicate that (y2i+1, y2i , y2i−1) belongs to which case. The signal neg i is for negation

y_{2i+1}	y_{2i}	y_{2i-1}	Operation on X	neg_i	two_i	one_i	cor_i
0	0	0	+0X	0	0	0	0
0	0	1	+1X	0	0	1	0
0	1	0	+1X	0	0	1	0
0	1	1	+2X	0	1	0	0
1	0	0	-2X	1	1	0	1
1	0	1	-1X	1	0	1	1
1	1	0	-1X	1	0	1	1
1	1	1	-0X	1	0	0	0

operation and cor-i is the correction bit for negative operation. The neg-first means that the negation operation is done before the selection between ''1X'' and ''2X''. For generating PP, the neg/two/one-nf decoder adopts the OR-AND-INV (OAI) gate, and all input signals of this OAI gate almost arrive at the same time (about 1 XNOR gate delay) as shown in Fig. 2. Therefore, the signal paths are way more balanced than other schemes and the glitches can be reduced. However, in the case of ''−0X'', neg-i = y2i−1 may lead to more switching activities in the XNOR gate since signals one-i and two-i can set PP to 0 regardless of neg-i . Note that the neg-first design needs one more compact decoder to generate the first nx signal and this decoder no needs to generate the PP as shown in Fig. 3. Therefore, each PP row of the neg-first design has one encoder and n + 2 decoders. The NMBE scheme which is based on the PTL has less cost than traditional design. But, this scheme suffers from the problems of weak 1/strong 0 and the signal paths are not balanced. Research provided three approximation

techniques for radix-4 Booth multipliers and one of them is called approximate Booth multipliers models 1 (ABM-M1). ABM-M1 is composed of the exact partial product generators (radix-4 Booth encoder and encoder) and the approximate

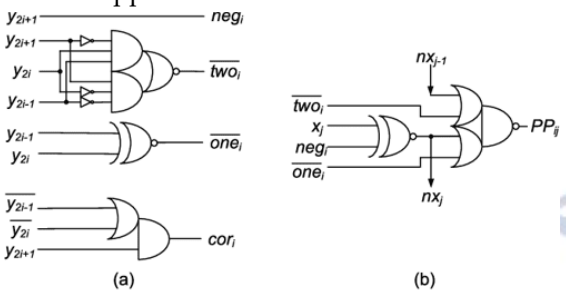


FIGURE 2. Neg/two/one-nf generator. (a) encoder; (b) decoder. 2-signal partial product generators (called PPG-2S).

Take 8-bit ABM-M1 with m = 4 for example, the PPs with a significance less than 4 are generated by PPG-2Ss and the remaining PPs are generated by the exact partial product generators. ABM-M1 can provide useful results with the low area-power product.

3. THE PROPOSED RADIX-4 BOOTH MULTIPLIER WITH PRE-ENCODED MECHANISM:

In this paper, we propose a pre-encoded mechanism to reduce the power consumption of the radix-4 Booth multiplier. As mentioned above, the unnecessary switching activities make multiplier consume more power, and the PPs must be 0s in the ''0X'' case. For that reason, we propose a pre-encoded mechanism to find the ''0X'' case earlier to reduce the unnecessary switching activities of the radix-4 Booth encoders and decoders. When detects the ''0X'' case, the proposed pre-encoded mechanism can turn off Booth encoders and decoders immediately to save power. The architecture and the timing chart of the proposed pre-encoded mechanism are shown in Fig. 4 and Fig. 5, respectively. As shown in Fig. 4, the proposed pre-encoded mechanism is composed of multiplicand and multiplier registers, additional proposed pre-encoders, and radix-4 Booth multiplier (includes adders, the proposed low cost Booth encoders and decoders). The signals xn−1_db. . . x0_db (db means data bus) and yn−1_db. . . y0_db denote the multiplicand X and multiplier Y on the data bus, respectively; xn−1. . . x0 and yn−1. . . y0 denote the outputs of the multiplicand and multiplier registers. As shown in Fig. 5, the multiplicand X and multiplier Y would be set on the data bus during the data setup time before the multiplication (multiplication phase). The proposed mechanism can detect the ''0X'' case during this setup time (denotes as pre-encode phase). In order to detect the ''0X'' case before the multiplication, the proposed design needs additional pre-encoders. If the ''0X'' case occurs, the proposed pre-encoders will immediately turn off the corresponding Booth encoders and decoders, and the corresponding PPs will be set as 0s to reduce the switching activities. In contrast, the Booth encoders and decoders will work as usual. Because the pre-encoders process the ''0X'' case already, the proposed Booth encoders and decoders only

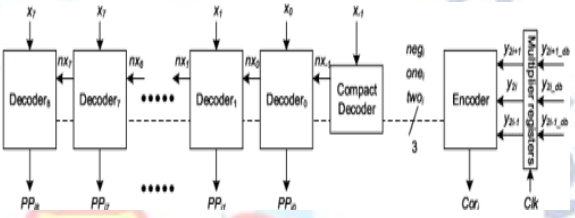


FIGURE 3. One 8-bit PP row of the neg-first scheme.

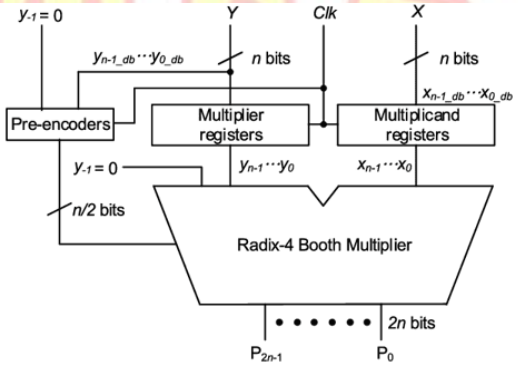


FIGURE 4. The architecture of the proposed radix-4 booth multiplier with the pre-encoded mechanism.

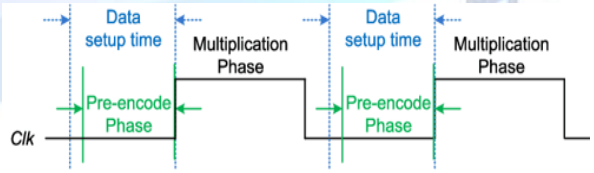


FIGURE 5. The timing chart of the proposed pre-encoded mechanism.

TABLE 3. The proposed pre-encode radix-4 booth algorithm.

y_{2i+1}	y_{2i}	y_{2i-1}	Operation on X	$zero_i$	neg_i	ot_i	cor_i
0	0	0	0X	1	0	d	0
0	0	1	+1X	0	0	1	0
0	1	0	+1X	0	0	1	0
0	1	1	+2X	0	0	0	0
1	0	0	-2X	0	1	0	1
1	0	1	-1X	0	1	1	1
1	1	0	-1X	0	1	1	1
1	1	1	0X	1	1	d	0

need to process the ''±1X'' and ''±2X'' cases, then, the cost of our design can be reduced. Accordingly, the proposed pre-encoded mechanism has less cost than the other designs. A. THE PROPOSED PRE-ENCODER The proposed pre-encoded mechanism needs pre-encoder to detect the ''0X'' case in the pre-encode phase. Table 3 shows the proposed pre-encoded radix-4 Booth algorithm. The proposed pre-encoded mechanism has three encoded signals. Signal zeroi which is generated by the proposed pre-encoder can determine the continuous three bits of multiplier Y on the data bus are the same or not. Signals negi and oti are generated.

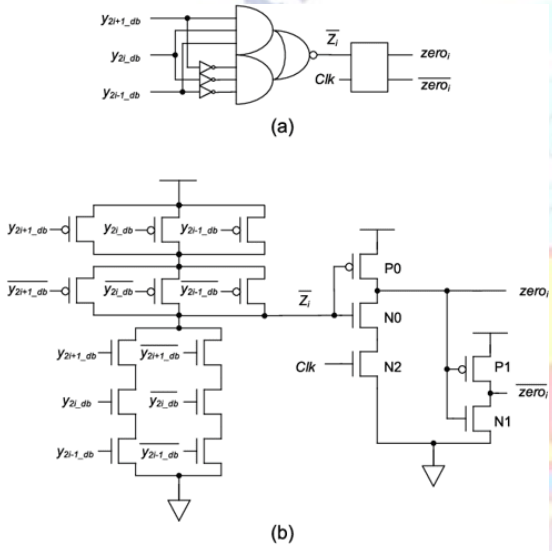


FIGURE 6. The proposed pre-encoder. (a) gate level; (b) transistor level. by the proposed encoder. Signal neg-i is for the negation operation; signals neg-i and oti are for the remaining cases (''±1X'' and ''±2X''). Note that signal zero-i has the highest priority, cor-i is the correction bit for negative operation, and d means ''don't care''. According to Table 3, when y2i+1, y2i , and y2i−1 on the data bus have the same value, the ''0X'' case occurs, thus, the signal zeroi will be 1. The equation of zeroi can be written as zero-i = (y2i+1 · y2i · y2i−1)db + (y2i+1 · y2i · y2i−1)db (3) where db means that the y2i+1, y2i , and y2i−1 arrive at the data bus in the pre-encode phase. According to (3), the proposed pre-encoder can be implemented with the AND-OR-INV (AOI) gate and a latch-like circuit as shown in Fig. 6(a). Fig. 6(b) shows the proposed pre-encoder at the transistor level. In the pre-encode phase, when the multiplier Y arrives on the data bus, the pre-encoder starts to detect the ''0X'' case. The signal zero-i is generated to control the proposed low cost encoder and decoders (introduce in section III-B) of the ith PP row; the encoder and decoders work as usual or not in the multiplication phase according to the signal zero-i . 1) ''Non-0X'' cases: In the pre-encode phase, if the y2i+1_db, y2i_db, and y2i−1_db are not the same, the signal zero-i will be set to 0 by the proposed pre-encoder. Therefore, the proposed encoder and decoders of the ith PP row will work as normal to generate the corresponding PPs in the multiplication phase. 2) ''0X'' case: In the pre-encode phase, if the y2i+1_db, y2i_db, and y2i−1_db are the same, the signal zero-i will be set to 1 by the proposed pre-encoder. Thus, the proposed encoder and decoders of the ith PP row will be powered off to reduce power consumption, and the corresponding PPs will be set to 0s directly in the

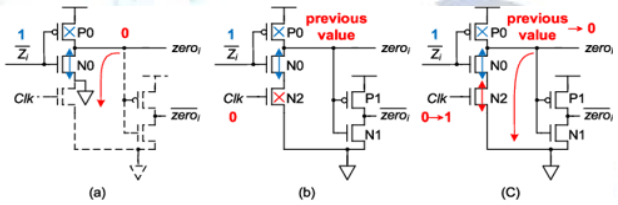


FIGURE 7. The difference between the proposed pre-encoder without and with the latch-like circuit. (a) without the latch-like circuit; (b) with the latch-like circuit in the pre-encode phase; (c) with the latch-like circuit in the multiplication phase.

pre-encode phase. In the multiplication phase, these gated encoder and decoders are no need to work since they are already turned off and the corresponding PPs are already set to 0s. Note that the latch-like circuit shown in Fig. 6 is added to prevent the probably happened unnecessary switching activities when ''0X'' case changes to ''non-0X'' case. Fig. 7 shows the latch-like circuit operations in this special situation. As shown in Fig. 7(a), when ''0X'' case changes to ''non0X'' case (signal Zi changes from 0 to 1) in the pre-encode phase, the pre-encoder without the latch-like circuit generates zero-i as 0 immediately that makes encoder and decoders turn on to do the redundant multiplication of the previous time (''0X'' case). To avoid this redundant multiplication, the latch-like circuit is required. As shown in Fig. 7(b), when ''0X'' case changes to ''non-0X'' case in the pre-encode phase, Clk is 0, and N2 is turned off. The pre-encoder with the latch-like circuit makes zero-i keep the previous value at a high voltage level to turn off the encoder and decoders, then, the redundant

multiplication can be avoided. However, until Clock changes from 0 to 1, N2 is turned on and the pre-encoder with latch-like circuit makes zero-i as 0 through N0 and N2 to power on the encoder and decoders; the ''non-0X'' multiplication starts normally in the multiplication phase. B. THE PROPOSED LOW COST RADIX-4 BOOTH ENCODER AND DECODER Because the ''0X'' case has been processed by the proposed pre-encoder, the encoder and decoder only need to process the remaining cases (''±1X'' and ''±2X''). For that reason, the costs of radix-4 Booth encoder and decoder can be reduced. In this paper, we propose the low cost radix-4 Booth encoder and decoder as shown in Fig. 8 and Fig. 9 to reduce the power consumption further. The gating techniques (power gating and ground gating) and the low cost of our design can reduce the dynamic and also static power consumption effectively. In particular, the issues of reducing static power consumption become more and more important when technology progresses. Table 4 shows a summary of the proposed pre-encoded radix-4 Booth algorithm. Signal zero-i can be used as the control signal of the gating transistors that are added in the proposed encoder and decoder. When zeroi is 1, the proposed encoder and decoder will be gated to reduce

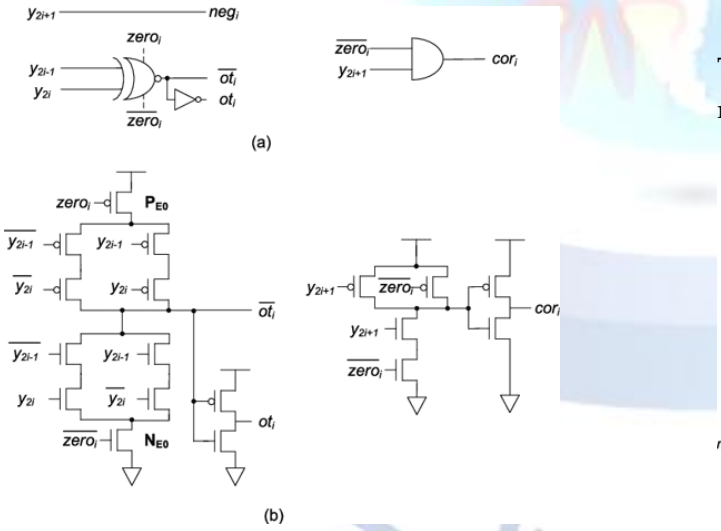


FIGURE 8. The proposed low cost encoder. (a) gate level; (b) transistor level.

power consumption. The proposed encoder and decoder will work as usual. Fig. 8(a) and Fig. 8(b) show the details of the proposed encoder. Like the traditional design, the inputs y2i+1, y2i , and y2i−1 of the proposed encoder are the outputs of the corresponding multiplier registers. Note that the inputs of the proposed pre-encoder are the multiplier Y on the data bus since the pre-encoder needs to detect the ''0X'' case earlier in the pre-encode phase. Because of this pre-encoder, the proposed encoder only needs to generate signals neg-i and oti . According to Table 3, the expressions of negi and oti are neg-i = y2i+1 (4) oti = y2i−1 ⊕y2i (5) Signal neg-i is equal to y2i+1 and signal oti can be generated by an XOR gate. The XOR gate can be implemented with the CMOS logic.To reduce the power consumption in the ''0X'' case, the XOR gate of the proposed encoder adopts the gating techniques. As shown in Fig. 8(b), the gating transistor PE0 is added between the power supply and the XNOR logic, and is controlled by zero-i . The gating transistor NE0 is added between GND and the XNOR logic, and is controlled by zero-i . Signals zero-i and zero-i are generated by the proposed pre-encoder as introduced above. 1) ''Non-0X'' cases: In the pre-encode phase, if the y2i+1, y2i , and y2i−1 are not the same, the signal zero-i is 0. Thus, the gating transistors PE0 and NE0 of the proposed encoder will be turned on. The proposed encoder works as normal to generate the corresponding encoded signals in the multiplication phase. 2) ''0X'' case: In the pre-encode phase, if the y2i+1, y2i , and y2i−1 are the same, the signal zero-i is 1. Thus, the

TABLE 4. The summary of the proposed pre-encoded radix-4 booth algorithm simplified from Table 3.

Case	$zero_i$	ot_i	cor_i	PP_{ij}
$0X$	1	d	0	0
$\pm 1X$	0	1	neg_i	$neg_i \oplus x_j$
$\pm 2X$	0	0	neg_i	$neg_i \oplus x_{j-1}$

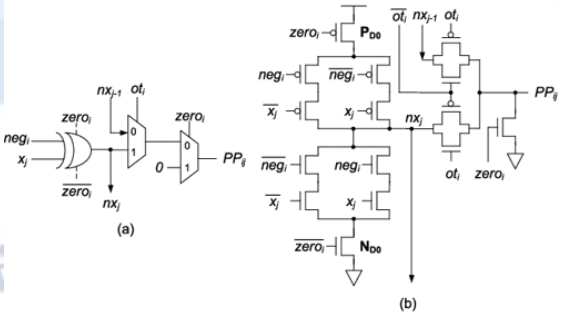


FIGURE 9. The proposed low cost decoder. (a) gate level; (b) transistor level.

gating transistors PE0 and NE0 of the proposed encoder will be turned off to reduce the dynamic power consumption and leakage currents. In the multiplication

phase, the proposed encoder still stays in the standby mode to save power.

According to Table 3, the expression of correction bit cor-i can be written as cor-i = y2i+1 · zero-i (6) the correction bit can be generated by an AND gate that is simpler than the circuitry. The correction bit cor-i is 0 in the ''0X'' case; otherwise, the value of cor-i depends on y2i+1 (neg-i) as summarized in Table 4. Fig. 9(a) and Fig. 9(b) show the details of the proposed decoder. Like the traditional design, the input xj of the proposed decoder is connected with the output of the corresponding multiplicand register. According to the encoded signals of the proposed pre-encoder and encoder, the proposed decoder can generate the corresponding PP. As introduced before, the PP should be 0 when the ''0X'' case occurs. The PP of ''+1X'' is xj and the PP of ''−1X'' is xj . The PP of ''+2X'' is xj−1 and the PP of ''−2X'' is xj−1. Table 4 summarizes the PP value of each case; the PP values of ''±1X'' and ''±2X'' can be defined as (7) and (8), respectively. PP±1X = neg-i ⊕xj = nxj (7) PP±2X = neg-i ⊕ xj−1 = nxj−1 (8) Based on Table 4, the expression of PP value can be written as PPij = zero-i · 0 + zero-i · oti · nxj + oti · nxj−1 (9) According to (9), the proposed decoder can be composed of an XOR gate and two multiplexers (MUXs). The XOR gate

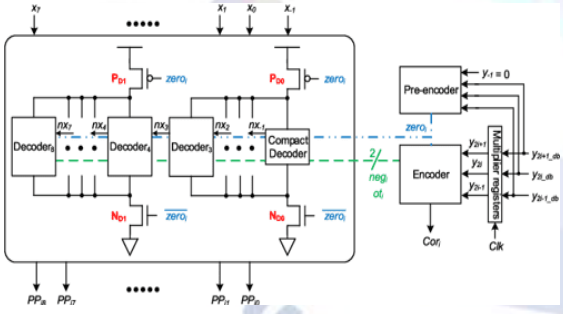


FIGURE 10. One 8-bit PP row of the proposed pre-encoded mechanism.

is implemented with the CMOS logic and its output is shared with the neighbor decoder. The first MUX which is controlled by oti is implemented by the transmission gates (TGs); the second MUX which is controlled by zero-i can be implemented easily by an NMOS. Like the proposed encoder, the proposed decoder adopts the gating techniques. As shown in Fig. 9(b), the gating transistor PD0 which is controlled by zero-i is added between the power supply and the XOR logic; the gating transistor ND0 which is controlled by zero-i is added between GND and the XOR logic. 1) ''Non-0X'' cases: In the pre-encode phase, the signal zero-i is 0 when the y2i+1, y2i , and y2i−1 are not the same. In the multiplication phase, the gating transistors PD0 and ND0 of the proposed decoder are turned on to generate the signal nxj as normal. Therefore, the proposed decoder can generate the corresponding PP according to the encoded signals oti and zero-i . 2) ''0X'' case: In the pre-encode phase, the signal zero-i is 1 when the y2i+1, y2i , and y2i−1 are the same. Since zero-i is 1, the PP will be set to 0 directly in the pre-encode phase. In addition, the gating transistors PD0 and ND0 of the proposed encoder are turned off to reduce the dynamic power consumption and leakage currents. In the multiplication phase, the PP is 0, and the proposed decoder still stays in standby mode to save power. As shown in Fig. 10, each PP row of the proposed preencoded mechanism has one pre-encoder, one encoder, and n + 2 decoders (10 decoders for n = 8). Clearly, the decoders account for the majority of the circuitry cost of each PP row. To minimize the cost of the proposed decoders, the additional gating transistors can be shared. As shown in Fig. 10, every five decoder shares a set of gating transistors. Take 8-bit multiplication (n = 8) for example, there are 10 decoders including the compact decoder in each PP row, and these decoders can be divided into two groups. In the first group, decoder0 to decoder3 and the compact decoder share the gating transistors PD0 and ND0. Notice that the compact decoder is implemented only by the XOR gate with the gating transistors because the compact decoder no needs to generate the PP. In the second group,decoder4 to decoder8 share the gating transistors PD1 and ND1. When zeroi is 0, these two groups work as usual to generate the corresponding PPs. When zero-i is 1, these two groups will be turned off to reduce power consumption and set PPs of this row to 0s immediately. Table 5 summarizes the comparisons for the proposed pre-encoded design and the related designs. The traditional design is the four-signal scheme and have balanced signal propagation paths. But, the cost of traditional design is higher than the others. The NMBE design is the three-signal scheme and based on the PTL. The cost of the NMBE design is low, but the signal paths are not balanced. Moreover, the NMBE design suffers from the problems of weak 1/strong 0 that makes the

static power increase. In order to reduce the circuit complexity, the ABM-M1 design adopted the approximate decoders (PPG-2S) in some least-significant bits. The encoder has 50 transistors which is larger than the others since this encoder needs to encode for the exact and approximate decoders. The ABM-M1 design can only be used in the error-tolerant applications. Same as the neg-first design proposed design has three encoded signals and balanced signal propagation paths. However, the neg-first design has the ''−0X'' case that may lead to more switching activities in XNOR gates of decoders. For n-bit multiplication of design and the proposed design, one PP row needs one encoder and n+ 2 decoders (one additional pre-encoder for the proposed design). Obviously, the proposed design has less cost than the others even though the proposed design needs the additional pre-encoder. Because of the pre-encoder, the proposed design can turn off the encoder and decoders to save power in the ''0X'' case. Therefore, we expect that the proposed design has the better power efficiency than the other designs.

4. SIMULATION RESULTS:

In this paper, the related works and the proposed pre-encoded mechanism are simulated by using TSMC 40 nm CMOS technology. The supply voltage is 1.0V, the clock frequency is 100 MHz, and the simulation is done by HSPICE tool. We simulate generating one PP row of n-bit multiplication (n = 8 or n = 16); we provide the power consumption, the performance, and transistor count (TC) to show the effectiveness of the proposed pre-encoded mechanism. We also provide the overall comparisons of multipliers to prove the superiority of the proposed design over the related works.

A. FUNCTIONALITY: To verify the feasibility and correctness of the proposed preencoded mechanism, the TSMC 40 nm technology is used to simulate two specific scenes with HSPICE. One specific scene is changing from ''0X'' case to ''non-0X'' case and the other is changing from ''non-0X'' case to ''0X'' case. Fig. 11 and Fig. 12 show the waveforms of these two specific scenes. The black solid line is the clock signal Clock, the blue solid

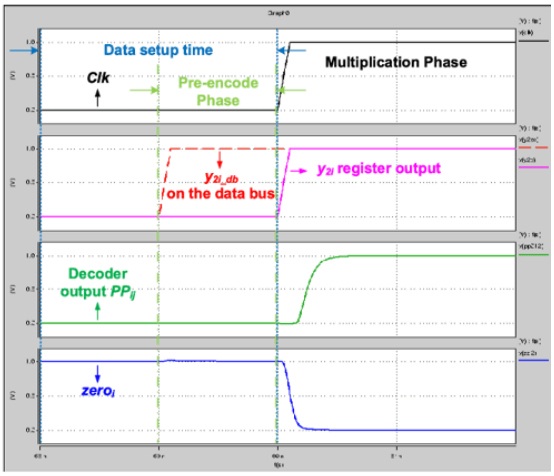


FIGURE 11. The waveforms of ''0X'' case changing to ''non-0X'' case

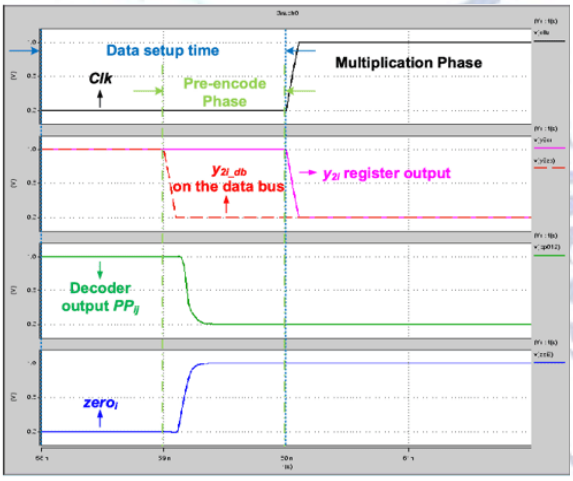


FIGURE 12. The waveforms of ''non-0X'' case changing to ''0X'' case.

B.POWER CONSUMPTION ANALYSIS:

The proposed pre-encoded design is compared with the related works [16], [18], [19], [22]; we simulate generating one PP row with 8-bit multiplication and 16-bit multiplication for each design. The continuous three bits of multiplier Y (y2i+1, y2i , y2i−1) change from one pattern to each pattern. We simulate these pattern switches with the 100 MHz clock frequency and provide the average power consumption for each pattern. The power consumption of the proposed design is composed of the power consumption of pre-encoder, encoder, and decoders. The power consumption of each related work is composed of the power consumption of encoder and decoders. Note that we simulate one row of the ABM-M1 design [22] with the approximation factor m = 4 (m = 8) for the 8-bit multiplication (16-bit multiplication). When m = 4(m = 8), one row of the ABM-M1 design [22] is

composed of one encoder, five (nine) exact decoders, and four (eight) PPG-2Ss. Fig. 13 shows the average dynamic power consumption for each pattern switch. For instance, ''000'' in Fig. 13 represents the average power consumption for changing from each pattern to pattern ''000''. Obviously, the dynamic power consumption of the proposed design is less than the power consumption of the other designs for each pattern switch because the proposed design has the advantages of less cost and race-free. The dynamic power consumption of the NMBE design is larger than the traditional design in some cases (especially ''000'') because of the strong 0/weak 1 problems. Table 6 summarizes the average dynamic power consumption of pattern switches for generating one PP row. The NMBE design has the largest dynamic power consumption due to the drawbacks of the poor voltage level. The results of the ABM-M1 design in Table 6 are simulated with approximation factor m = 4 (8-bit) and m = 8 (16-bit). For 8-bit (16-bit) case, compared to the traditional design [16] and the neg-first design [18], the proposed design can reduce the dynamic power consumption by 70.4% (75.4%) and 24.9% (32.1%), respectively; compared to the approximate design [22], the proposed design can reduce the dynamic power consumption by 43.3% (48.6%) and provide precise products. Fig. 14 shows the static power consumption for each pattern. Take ''000'' for example, the multiplier Y (y2i+1, y2i , y2i−1) is fixed at 000 to get the static power consumption of ''000'' pattern. As shown in Fig. 14, in patterns ''000'' and ''111'', the proposed design can save more static power consumption since the proposed pre-encoder can turn off the encoder and decoders in these patterns (the ''0X'' case). The static power consumption of the NMBE design [19] is larger than the traditional design [16] in some cases (especially ''000'') because of the drawbacks of the poor voltage level. Table 6 summarizes the average static power consumption of the eight patterns for one PP row. The NMBE design still has the largest static power consumption. For 8-bit (16-bit) case, compared to the traditional design [16] and the neg-first design, the proposed design can reduce the static power consumption by 71.5% (75.8%) and 23.3% (27.4%), respectively; compared to the approximate design the proposed design can reduce the static power consumption by 40.6% (44.6%). C. PERFORMANCE AND COST ANALYSES The performance and cost analyses for one PP row are summarized in Table 6. The worst case delay is the metric to evaluate the performance. For example, the worst case delay of the neg-first design will occur when signal twoi changes from 0 to 1 or 1 to 0. The worst case delay of the proposed design will occur when the encoded signals change from ''0X'' to ''non-0X'' case. As shown in Table 6, the NMBE design has the longest delay due to the weak drivability of signals. For 8-bit (16-bit) case, compared to the traditional design [16] and the neg-first design, the delay reductions of the proposed design are 20.9% (34.4%) and 20.5% (20.7%), respectively. As shown in Table 6, the worst case delay of the ABM-M1 design is contributed by the exact decoder. Compared to the ABM-M1 design delay reduction of the proposed design is 18.7% (23.6%).

C. **COMPARISON OF RADIX-4 BOOTH MULTIPLIERS:** In order to show the effectiveness of our design, we also provide the comparisons of the radix-4 Booth multipliers as shown in Table 7. For a fair comparison, each design adopts the same adder array for PP accumulation as shown in Fig. 1. Only the multiplier of the ABM-M1 design is the approximate multiplier, and the approximation factor m = 4 for 8-bit multiplication (m = 8 for 16-bit multiplication). Take 16-bit multiplication with m = 8 for example, the PPs with a significance less than 8 are generated by PPG-2Ss and the remaining PPs are generated by the exact decoders. Compared to the traditional design the other designs can reduce the dynamic power consumption and TC. However, the NMBE design is the worst in terms of static power consumption and delay because of the drawbacks of the poor voltage level that increases the leakage currents and delay. Because the proposed pre-encoded design has the advantages of race-free, conditional power gating, and low cost, the proposed design is the best design in terms of dynamic power, static power, delay, power-delay product (PDP), and TC as shown in Table 7. For 8-bit (16-bit) case, compared to the traditional design [16], the proposed design can reduce the dynamic power and static power by 43.9% (44.9%) and 61.6% (65.2%), respectively, with 4.0% (5.0%) performance improvement. Compared to the neg-first design [18], the proposed design can reduce the dynamic power and static power by 5.9% (6.9%) and 26.1% (29.4%), respectively. Compared to the approximate design [22], the proposed design can provide the exact results, and can reduce the dynamic power and static power by 26.5%

(28.0%) and 38.6% (41.1%), respectively. Obviously, the proposed design has the lowest PDP results. Fig. 13, Fig.14, Table 6, and Table 7 prove the superiority of the proposed design compared to the other designs.

5. CONCLUSION:

In this paper, a low power radix-4 Booth pre-encoded mechanism has been proposed to reduce the unnecessary switching activities of encoders and decoders in the ''0X'' case. The proposed pre-encoded mechanism can detect the ''0X'' case earlier and adopts the gating techniques. When the ''0X'' case occurs, the encoder and decoders will be turned off immediately by the proposed pre-encoder to reduce the power consumption and leakage currents. The simulations are done by HSPICE with the TSMC 40 nm technology and the results show that the proposed design can provide significant reductions in power consumption, delay, and transistor count compared with the state-of-the-art encoded designs. For 16-bit multiplication, compared to the traditional radix4 Booth multiplier, the proposed pre-encoded mechanism has 35% reduction in transistor count, 5% improvement in performance, and can reduce dynamic and static power consumption by 65% and 85%, respectively. Compared to the neg-first design and the NMBE design, the proposed design has better performance, less transistor count, and lower power consumption. Even compared to the approximate design, the proposed design can provide precise products, and can achieve 28% dynamic power reduction and 41% static power reduction

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

[1] G.-N. Sung, Y.-J. Ciou, and C.-C. Wang, ''A power-aware 2-dimensional bypassing multiplier using cell-based design flow,'' in Proc. IEEE Int. Symp. Circuits Syst., May 2008, pp. 3338–3341.

[2] G.-L. Jiang, T.-C. Wu, and Y.-J. Chang, ''Low power multiplier with alternative bypassing implementation,'' in Proc. Int. Conf. Embedded Syst. Appl. (ESA), Jul. 2012, pp. 77–82. 114852 VOLUME 8, 2020 Y.-J. Chang et al.: Low Power Radix-4 Booth Multiplier With Pre-Encoded Mechanism

[3] X. Cui, W. Liu, X. Chen, E. E. Swartzlander, and F. Lombardi, ''A modified partial product generator for redundant binary multipliers,'' IEEE Trans. Comput., vol. 65, no. 4, pp. 1165–1171, Apr. 2016.

[4] J. M. D. Moss, D. Boland, and H. W. P. Leong, ''A two-speed, radix-4, serial–parallel multiplier,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 27, no. 4, pp. 769–777, Dec. 2018.

[5] B. Moons and M. Verhelst, ''An energy-efficient precision-scalable ConvNet processor in 40-nm CMOS,'' IEEE J. Solid-State Circuits, vol. 52, no. 4, pp. 903–914, Apr. 2017.

[6] J. Jo, S. Kim, and I.-C. Park, ''Energy-efficient convolution architecture based on rescheduled dataflow,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 12, pp. 4196–4207, Dec. 2018.

[7] C.-H. Chang, J. Gu, and M. Zhang, ''Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits,'' IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 10, pp. 1985–1997, Oct. 2004.

[8] P. Aliparast, Z. D. Koozehkanani, and F. Nazari, ''An ultra high speed digital 4–2 compressor in 65-nm CMOS,'' Int. J. Comput. Theory Eng., vol. 5, no. 4, pp. 593–597, Aug. 2013.

[9] Y.-J. Chang, Y.-C. Cheng, Y.-F. Lin, S.-C. Liao, C.-H. Lai, and T.-C. Wu, ''Imprecise 4–2 compressor design used in image processing applications,'' IET Circuits, Devices Syst., vol. 13, no. 6, pp. 848–856, Sep. 2019.

[10] J. Park, S. Kim, and Y.-S. Lee, ''A low-power booth multiplier using novel data partition method,'' in Proc. IEEE Asia–Pacific Conf. Adv. Syst. Integr. Circuits, Aug. 2004, pp. 54–57.

[11] I. S. Abu-Khater, A. Bellaouar, and M. I. Elmasry, ''Circuit techniques for CMOS low-power high-performance multipliers,'' IEEE J. Solid-State Circuits, vol. 31, no. 10, pp. 1535–1546, Oct. 1996.

[12] M. D. Ercegovac and T. Lang, Digital Arithmetic, 1st ed. Los Altos, CA, USA: Morgan Kaufmann, 2003.

[13] P. J. Song and G. De Micheli, ''Circuit and architecture trade-offs for high-speed multiplication,'' IEEE J. Solid-State Circuits, vol. 26, no. 9, pp. 1184–1198, Sep. 1991.

[14] G. Goto, T. Sato, M. Nakajima, and T. Sukemura, ''A 54 × 54-b regularly structured tree multiplier,'' IEEE J. Solid-State Circuits, vol. 27, no. 9, pp. 1229–1235, Sep. 1992.

[15] N. Ohkubo, M. Suzuki, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasalu, and Y. Nakagome, ''A 4.4 ns CMOS 54 × 54-b multiplier using pass transistor multiplexer,'' IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 251–257, Mar. 1995.

[16] R. Fried, ''Minimizing energy dissipation in high-speed multipliers,'' in Proc. Int. Symp. Low Power Electron. Design, Aug. 1997, pp. 214–219.

[17] W.-C. Yeh and C.-W. Jen, ''High-speed booth encoded parallel multiplier design,'' IEEE Trans. Comput., vol. 49, no. 7, pp. 692–701, Jul. 2000.

[18] Z. Huang and M. D. Ercegovac, ''High-performance low-power left-to-right array multiplier design,'' IEEE Trans. Comput., vol. 54, no. 3, pp. 272–283, Mar. 2005.

[19] P. R. Rajput and M. N. S. Swamy, ''High speed, efficient area, low power novel modified booth encoder multiplier for signed-unsigned number,'' Adv. Intell. Syst. Comput., vol. 464, pp. 321–333, Apr. 2016.

[20] H. Jiang, J. Han, F. Qiao, and F. Lombardi, ''Approximate radix-8 booth multipliers for low-power and high-performance operation,'' IEEE Trans. Comput., vol. 65, no. 8, pp. 2638–2644, Aug. 2016.

[21] W. Liu, L. Qian, C. Wang, H. Jiang, J. Han, and F. Lombardi, ''Design of approximate radix-4 booth multipliers for

error-tolerant computing,'' IEEE Trans. Comput., vol. 66, no. 8, pp. 1435–1441, Aug. 2017.

[22] S. Venkatachalam, E. Adams, H. J. Lee, and S.-B. Ko, ''Design and analysis of area and power efficient approximate booth multipliers,'' IEEE Trans. Comput., vol. 68, no. 11, pp. 1697–1703, Nov. 2019.

[23] A. D. Booth, ''A signed binary multiplication technique,'' Quart. J. Mech. Appl. Math., vol. 4, no. 2, pp. 236–240, 1951.

[24] O. Macsorley, ''High-speed arithmetic in binary computers,'' Proc. IRE, vol. 49, no. 1, pp. 67–91, Jan. 1961.

[25] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.

[26] N. S. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and V. Narayanan, ''Leakage current: Moore's law meets static power,'' Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[27] (2015). Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: http://www.itrs2.net/

[28] S. Nishizawa, T. Ishihara, and H. Onodera, ''Analysis and comparison of XOR cell structures for low voltage circuit design,'' in Proc. Int. Symp. Qual. Electron. Design (ISQED), Mar. 2013, pp. 703–708.