International Journal for Modern Trends in Science and Technology, 8(07): 286-291, 2022

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST0807043
Available online at: http://www.ijmtst.com/vol8issue07.html

An Advanced Power Flow Control Strategy for A Series APF with Critical Load Bus Voltage Feedback in Distribution System

N.Sunil Kumar Reddy[1] | B.N.Prasad[2]

[1]PG Student, Dept of EEE, AITS, Kadapa, AP, India.
[2]Assistant Professor, Dept of EEE, AITS, Kadapa, AP, India.

To Cite this Article
N.Sunil Kumar Reddy and B.N.Prasad. An Advanced Power Flow Control Strategy for A Series APF with Critical Load Bus Voltage Feedback in Distribution System. International Journal for Modern Trends in Science and Technology 2022, 8(07), pp. 286-291. https://doi.org/10.46501/IJMTST0807043

Article Info
Received: 19 June 2022; Accepted: 21 July 2022; Published: 26 July 2022.

ABSTRACT

Power quality is an important measure of the performance of an electrical power System. Moreover, problems related to the utility grid, such as voltage sags or swells, voltage unbalances and voltage harmonics have helped to decrease the power quality needed for critical loads. Series active power filters (APF) are an important solution to deal with power quality issues in weak grids under the presence of non-linear loads. The use of voltage feedback from the critical-load-bus in the series active power filter (APF) allows for a control strategy that has performance and processing power advantages, when compared to other strategies in literature, but can cause saturation of injection transformers. This paper presents a control strategy that uses critical load-bus voltage feedback with an additional control loop of the dc current in the output of the series APF voltage source converter (VSC), to avoid injection transformer saturation. The controlled dc current is additionally used for balancing the split dc-bus capacitors voltage in the VSC. The series APF and the proposed control strategy are modeled using small signal analysis for allowing controller design. MATLAB/SIMULINK Simulation results are presented with Critical load-bus voltage while achieving the objectives of improved critical load voltage waveform, controlled transformer dc current and balanced dc-bus capacitors voltage.

1. INTRODUCTION

The injection transformer's performance is critical to the system's correct operation. This transformer's design is critical since it must contend with saturation, overrating, overheating, cost, and performance. The injected voltage may include fundamental, desired harmonics, switching harmonics, and direct current voltage components. If the transformer is not appropriately designed, the injected voltage may saturate the transformer, resulting in poor system operation. This problem is overcome in the literature by over-rating the transformer; however this raises the overall cost and size of the system. The authors offer a systematic technique for designing and determining the voltage rating of a transformer while accounting for all frequency components in this study. Because designing with each frequency component is time-consuming, an equivalent fundamental frequency component is determined to account for all of the components. Transformer current is significantly distorted due to magnetising current, non-linear load current, and filter current. This could result in greater power loss than

pure sinusoidal current. The traditional series APF configuration connects a voltage source converter (VSC) in series from the PCC-bus to the cload-bus via an injection transformer. The traditional abc frame control approach for the voltage controlled series APF indirectly supplies pure sinusoidal voltage to the loads by extracting the fundamental and harmonic components of the PCC-bus voltage to provide counter harmonics as references for the VSC output voltage. However, additional low- or high-pass filters are required to isolate the fundamental voltage component, which increases computing efforts and adds a temporal delay that may impair compensation performance.

Other control systems employ transformation to distinguish between negative and positive sequences, as well as the dq0 reference frame to convert sinusoidal to dc variables. However, extra filters are required, and the reference frame translation increases computing work. If the feedback voltage is placed on the converter side (henceforth referred to as primary transformer side) when using these control techniques, it does not eliminate disturbances caused by the transformer, such as voltage drops in the leakage inductance, and there is no guarantee that the load voltage is well compensated. Due to the dc blocking nature of transformers, an undesired dc voltage at the VSC output would not be observed if the voltage is measured at the secondary of the transformer, and could destabilise the voltage controller. The control strategy presented in this paper acts directly on the cload bus voltage to ensure that it is regulated by placing the feedback voltage sensor on the load side, but an additional primary side dc current control loop is integrated to provide system stability with respect to injection transformer saturation. The dynamics of the injection transformer are taken into account in the formulation of the tiny signal models to design the controller for the proposed strategy. In split capacitor VSC, regulated dc current is also employed to create balanced dc bus capacitors voltage. The series APF requires a three-phase inverter with a neutral connection to correct each voltage independently. The simplest converter to correct voltages individually in each phase is the three-phase two-level VSC topology with split dc-bus capacitor.

This topology can be thought of as three separate half-bridge converters sharing a dc-bus. The neutral conductor serves as a return path, carrying current across the midway of the two capacitors, allowing each phase to generate totally independent compensation voltages. The shared dc-bus facilitates power transfer between phases, allowing for the adjustment of phase voltage imbalances. Unbalanced phase voltages create ripple in the dc-bus voltage unbalance (voltage differential between the split capacitors) in the split capacitor VSC because the neutral conductor instantaneous current is not zero. With an appropriately sized dc-bus capacitance, this is not an issue. In steady-state, however, the neutral conductor current cannot have a dc component since it would entirely discharge one of the capacitors. A split capacitor 3P4W converter and an output filter are used in the proposed series APF. Three single-phase transformers are utilised to connect the utility grid's series APF to the cload-bus. The suggested control approach may send PWM signals to the converter to achieve adequate voltage quality at the cload-bus by measuring the cload voltages (vcl), dc-bus voltages (vdc), and inductor filter currents (if). To synchronise the cload-bus voltage reference, the PCC-bus voltage (vPCC) is also measured.

2. SYSTEM TOPOLOGY

In Brazil, the conventional low-voltage power distribution consists of a three-phase transformer with a grounded neutral conductor. Adjustable speed drives, electric furnaces, lighting ballasts, office equipment, and other facilities with power electronics are typical loads linked to this three-phase, four wire (3P4W) power system. These loads can have high harmonic content input current, which causes voltage distortion at the PCC, and they can be single-phase or three-phase, resulting in voltage unbalance (different fundamental amplitude) across the three phases. This distribution line arrangement is a non-symmetrical system with three independent variables, i.e., the sum of the instantaneous value of phase voltages might be more than zero. The series APF requires a three-phase inverter with a neutral connection to correct each voltage independently. The simplest converter to correct voltages individually in each phase is the three-phase two-level VSC topology with split dc-bus capacitor shown in Fig. 1. This topology can be thought of as three separate half-bridge converters sharing a dc-bus. The neutral conductor serves as a return path, carrying current across the midway of the two capacitors,

allowing each phase to generate totally independent compensation voltages. The shared dc-bus facilitates power transfer between phases, allowing for the adjustment of phase voltage imbalances. Unbalanced phase voltages create ripple in the dc-bus voltage unbalance (voltage differential between the split capacitors) in the split capacitor VSC because the neutral conductor instantaneous current is not zero. With an appropriately sized dc-bus capacitance, this is not an issue. In steady-state, however, the neutral conductor current cannot have a dc component since it would entirely discharge one of the capacitors. To maximise the output voltage that may be achieved without over-modulation, equal voltages across two capacitors are preferred. Balanced dc capacitors also increase the dc bus's energy storage capacity for a given maximum capacitor voltage. Even if a certain amount of voltage unbalance is acceptable, this behavior can be unstable (i.e. the unbalance voltage diverges), and is hard to predicted in the design phase of the converter and maintain during its lifetime. The voltage unbalance can be compensated by controlling the neutral current of the converter, however, the neutral current and the dc output current in each phase can have different polarities. Therefore, high dc current, with opposite polarities, can be seen in two phases, while the neutral dc current is zero, causing transformer saturation. Therefore, a better solution is to independently control each phase dc output current, indirectly controlling the neutral current, achieving dc-bus voltage balance and preventing injection transformer saturation.

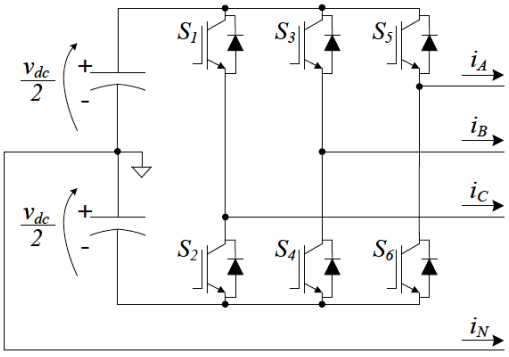

Fig. 1. Three-phase, four wire, split capacitor VSC.

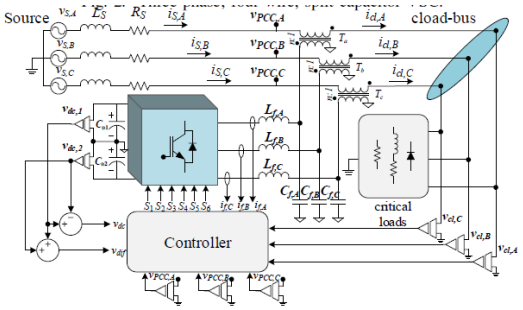

Fig. 2. General diagram of the series APF.

Another alternative power circuit topology is the fourleg VSC topology, where the neutral conductor is directly controlled. By adding this extra leg there is no need to split the capacitors and unbalance control is unnecessary, however, the overall cost and complexity of the fourth leg approach is a drawback, as it requires a controller for the fourth leg, and additional switching elements. Furthermore, the four-leg VSC topology does not eliminate the problem of dc output current saturating the transformers, and still requires the control of phase dc output current proposed in this paper. Therefore, in this paper the proposed series APF is composed of a split capacitor 3P4W converter and an output filter. Three single-phase transformers are used to connect the series APF from the utility grid to cload-bus as shown in Fig. 2. No PCC-bus loads are shown for simplicity. By measuring the cload voltages (vcl), dc-bus voltages (vdc) and inductor filter currents (if), the proposed control strategy can provide PWM signals to the converter to achieve satisfactory voltage quality at the cload-bus. PCC-bus voltage (vPCC) is also measured to synchronize the cload-bus voltage reference. The block diagram of the proposed control strategy for a 3P4W series APF with split dc-bus capacitors is presented in Fig. 3. It is composed of 2 external control loops, which controls dc-bus total voltage and dc-bus voltage unbalance, and two internal control loops (repeated for each phase), which controls the dc output current and cload-bus voltage. The controllers are Cv;cl(s), one for each cload-bus voltage, Ci;f , one for each dc output current, Cdif for the dc-bus voltage unbalance, and Cdc for the total dc-bus voltage. Sensors are represented by blocks hv;cl, hi;f , hdif and hdc, for the cloadbus voltage, dc output current, dc-bus voltage unbalance, and dc-bus total voltage, respectively. The inverter PWM gain is represented by block GPWM, and small signal models representing the

dc-bus voltage unbalance as a function of dc-output current (Vdif (s)=if (s)), dc-bus total voltage as a function of load-bus voltage (vdc(s)=vcl(s)), output current of the inverter (before the coupling transformer) as a function of the duty ratio , (if (s)=d(s)), and load-bus voltage (after the coupling transformer) as a function of the output current (vcl(s)=if (s)), are also used. The cload-bus voltage vcl is directly controlled by the innermost control loop, formed by Cv;cl, GPWM, hv;cl, if =d and vcl=if. The cload-voltage controller's reference is generated by a PLL and is completely sinusoidal, with the amplitude specified by the dc-bus voltage control loop. This technique eliminates the need for power computation and harmonic extraction, which are required in conventional control strategies. Load voltage harmonics generate an inaccuracy in the input of controller Cv;cl, which works on the duty ratio to track the sinusoidal reference. The branch in the control loop at if is not taken into account in the load-bus voltage design, and the dc-current control loop should be built so that it does not affect the load-bus voltage loop. Therefore, the cload-bus control loop can be simplified to the same, where the converter duty ratio is set by Cv;cl as to control the load-bus voltage at line frequency and its harmonics. Each phase also has a dc output current control loop. The dc output current of the inverter, measured before the transformer, is compared with its reference i_f, compensated by the controller Ci;f and given as a dc-voltage reference to the load-bus control loop. Because of the coupling transformer's dc-blocking nature, this technique was devised. Figure 4 depicts a simplified block diagram of the series APF control with cload-bus side feedback as an example. The voltage sensor hv;cl's dc offset error, voff, could produce a dc error in the controller Cv;cl's input. The controller acts to eliminate this dc level, but the series APF cannot impose a dc voltage on the transformer's secondary side. Cv;cl often has a high dc gain integrator in this control strategy, and the dc level continues to be integrated, applying a dc voltage to the primary side and causing the transformer to saturation. A traditional cascade controller, with inner current loop and outer voltage loop cannot solve this problem, as the same problem would arise as the voltage controller increases the current loop dc reference when trying to compensate the voltage offset. The proposed control strategy in Fig 3 solves this problem by adding a compensating dc voltage to the cload-bus voltage reference. This dc voltage reference is generated by the dc current control loop to ensure the dc current on the primary side of the transformer is within the reference i_f. To allow the design of these control loops, the small signal model of the VSC is split in two parts, the output current (before the transformer) as a function of the duty ratio, and the cload-bus voltage as a function of the converter output current (after the transformer). Both models are further developed. Considering that the dc output current control loop is designed to controlling the primary side dc current, it needs high dc gain to achieve low steady state error, but should have high attenuation at line frequency and its harmonics to avoid injecting harmonic content in the cload-bus voltage reference. The dc output current control loop includes the Cv;cl controller, which should be designed for high gain at line frequency to create the cload voltages with low harmonic content. Therefore the dc-current control loop naturally includes a source of high gain at line frequency. Therefore, proper design of Ci;f and hi;f should have high attenuation at line frequency to compensate the gain from Cv;cl. This allows the product of Ci;f and hi;f to be considered negligible when analyzing the cload-bus voltage control loop in Fig. 3, as previously considered.

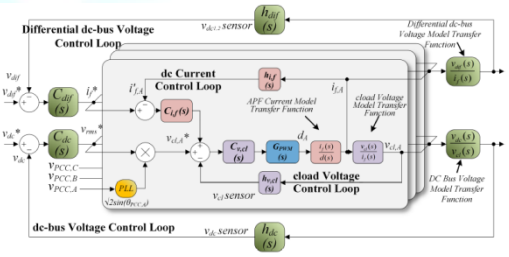

Fig. 3. Block diagram of the series APF control strategy including the representation of small signal models.

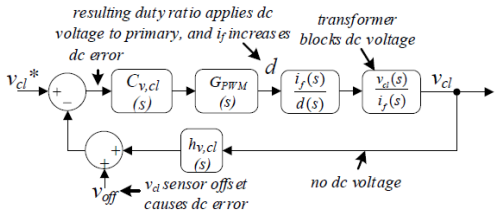

Fig. 4. Example of how cload sensor dc offset can cause dc current in the transformer.

The rms amplitude of the load voltage vrms is set by the total dc-bus voltage control loop, formed by controller Cdc, sensor hdc, model Vdc=Vcl(s), and the

load-bus voltage control loop. A decrease in the cload voltage increases the voltage drop in the series APF, which also increases the absorbed active power. An increase in the cload voltage has the opposite effect, decreasing the absorbed active power. By changing the active power flow into the converter, the charge rate of the dc-bus is controlled. The three load-bus voltage controllers receive sinusoidal voltage references with the same amplitude, v_rms. The four wire split-capacitor inverter can generate each phase voltage independently, allowing the controllers to balance the phase voltages to the same reference, with the required power transfer across phases occurring through the dc-bus capacitor. If the source voltages are unbalanced, and since the cload bus voltage is balanced due to action of the cload-bus controllers, each phase of the series APF can be either absorbing or providing active power.

3. SIMULATION RESULTS

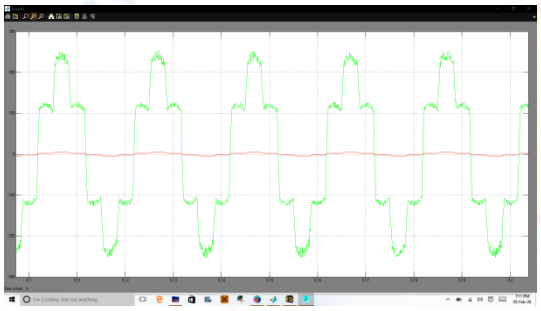

Fig:5. simulation waveforms without the VSC

The system is initially run without the series APF VSC, but with the injection transformer connected and its primary side short circuited. Simulation waveforms of phase A are shown in Fig. 5. The objective of running the system with the injection transformer is to verify its series voltage drop, since the dc-bus control strategy will increase this voltage drop for compensating the losses in the series APF VSC.

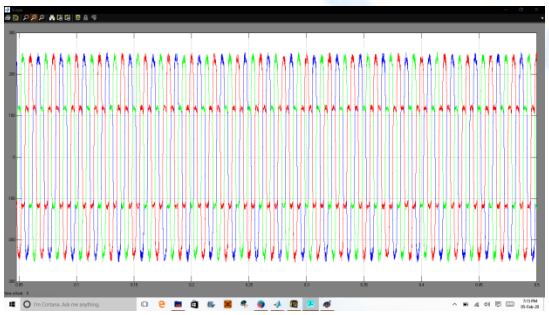

Fig:6. PCC-bus voltage waveforms of the series APF

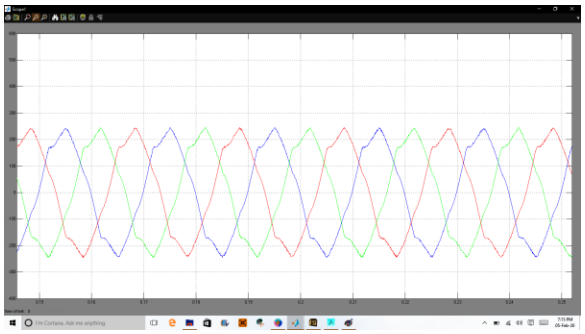

Fig:7. cload-bus voltage waveforms of the series APF

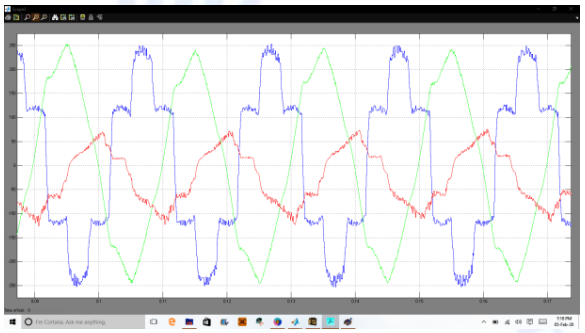

Fig:8. simulation waveforms of phase A cload voltage, PCC voltage, and series APF injected voltage

The phase voltage waveforms of the system running in its nominal operation point are shown in Fig. 6 and 7, for the PCC-bus and cload-bus respectively. Waveforms of the cload, PCC and transformer injected voltage of phase A is shown in Fig 8. The voltage injected by the series APF has significantly lower amplitude than the PCC-bus and cload-bus voltage.

4. CONCLUSION

This paper presented a complete control strategy for a 3P4W series APF which uses injection transformers to improve the PCC-bus voltage in a secondary, critical load bus. This control strategy uses cload-bus voltage feedback that provides increased harmonic elimination with simpler control as it can compensate the voltage drops in the injection transformer. A new strategy for controlling the dc output current of the converter, to avoid transformer saturation, was developed, and is also used for controlling the dc-bus capacitor voltage unbalance. Small signal models required for designing the proposed dc output current controller were also presented. The dc current control strategy can also be applied to other converters, including DVR and UPQC, when the series connected inverter uses load-bus voltage feedback. The experimental results showed the viability of the control strategy. The connection of an

unbalanced load in the dcbus does not cause steady state unbalance in its voltage, or transformer saturation. Operation without the dc-bus voltage unbalance controller and the primary side dc current controller was not possible, as the voltage from one of the dc-bus capacitors drops to zero, showing that the complete control strategy presented in this paper is necessary and an important contribution if use of load-bus voltage feedback is desired. The operation with lower dc bus voltage shows that the voltage drop in the series APF, necessary for compensating its losses in the proposed control strategy, can be small enough to achieve satisfactory load voltages, but is still a point that requires improvement as the phase of the voltage drop in the series APF is synchronized with the PCC-bus phase, resulting in a reactive voltage drop if the load displacement factor is not unity. Future work can verify the possibility of improving load-bus voltage amplitude by varying the series APF voltage drop phase angle.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

REFERENCES

[1] P. Fang Zheng, "Application issues of active power filters," IEEE Industry Applications Magazine, vol. 4, no. 5, pp. 21–30, 1998.

[2] A. M. Rauf and V. Khadkikar, "An enhanced voltage sag compensation scheme for dynamic voltage restorer," IEEE Transactions on Industrial Electronics, vol. 62, no. 5, pp. 2683–2692, 2015.

[3] R. J. M. d. Santos, J. C. d. Cunha, and M. Mezaroba, "A simplified control technique for a dual unified power quality conditioner," IEEE Transactions on Industrial Electronics, vol. 61, no. 11, pp. 5851–5860, 2014.

[4] E. R. Ribeiro and I. Barbi, "Harmonic voltage reduction using a series active filter under different load conditions," IEEE Transactions on Power Electronics, vol. 21, no. 5, pp. 1394–1402, 2006.

[5] J. G. Pinto, H. Carneiro, B. Exposto, C. Couto, and J. L. Afonso, "Transformerless series active power filter to compensate voltage disturbances," in Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Aug 2011, pp. 1–6.

[6] G. A. de Almeida Carlos and C. B. Jacobina, "Series compensator based on cascaded transformers coupled with three-phase bridge converters," IEEE Transactions on Industry Applications, vol. 53, no. 2, pp. 1271–1279, March 2017.

[7] Y. Chang, L. Jinjun, W. Xiaoyu, and W. Zhaoan, "A novel control of series active power filter without harmonics detection," in 2007 IEEE Power Electronics Specialists Conference, Conference Proceedings, pp.1112–1115.

[8] F. Mekri, M. Machmoum, N. Ait-Ahmed, and B. Mazari, "Saturation influence on the performances of series active power filter," in 2009 35th Annual Conference of IEEE Industrial Electronics, Nov 2009, pp. 3258–3263.

[9] B. Wang and M. Illindala, "Operation and control of a dynamic voltage restorer using transformer coupled h-bridge converters," IEEE Transactions on Power Electronics, vol. 21, no. 4, pp. 1053–1061, July 2006.

[10] S. A. O. D. Silva, P. F. Donoso-Garcia, and P. C. Cortizo, "A three-phase series-parallel compensated line-interactive ups system with sinusoidal input current and sinusoidal output voltage," in Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370), vol. 2, 1999, pp. 826–832 vol.2.