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Soft Switched Interleaved Boost Converter

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ABSTRACT

Power losses and their effects withinside the addition of garage cells have the bad impact of reducing the energy density and the performance in Electric Vehicles. For this reason, a performance optimization technique is needed to assist lessen that problem. Specifically, within the energy converters that interface the garage unit with the electrical vehicles and their inverters, a performance optimization is critical to lessen the energy losses and thereby downsize the cooling additives and the garage unit. In this work, the topology beneath neath assessment is the two-section interleaved raise converter the usage of specific magnetic additives including coupled and non-coupled inductors, which can be topologies referred to as powerful for excessive energy density applications. This paper affords a technique that optimizes the performance of the selected topologies through a whole energy loss modeling of every component. Next era additives including Super Junction Mosfets, GaN and SiC diodes and Mosfets are in comparison to achieve the maximum green and appropriate fabric to be carried out to the topologies, in particular to the converter with coupled-inductor. Moreover, a layout system is proposed to combine the loss version and the traits of the chosen additives because the base to achieve the goal function, that later solved the usage of analytical calculations. Finally, the optimization technique is confirmed with the aid of using experimental tests.Generally the converter performance is wanted in all of the designs. Probably we're having numerous converters, Among the numerous DC – Dc Converters, the evaluation remains to show which converter yields a great performance, Power issue and Current ripple In this Project, we going to evaluate the performance, Power Factor, Current Ripple, Voltage Ripple and to determine which Converter is ideal and green. The following DC-DC converter goes to be in comparison

1. ***Boost Converter.***
2. ***Bridge Boost Converter.***
3. ***Interleaved Boost Converter.***
4. ***Soft Switched Interleaved Boost converter.***

In comparison the results Soft Switched Interleaved Boost Converter has a good efficiency and less current ripple value.

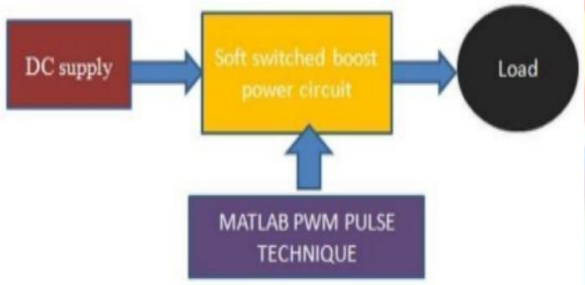
KEYWORDS: Optimization technology,ZCS,ZVS,Currentripple,Voltage ripple.

1. INTRODUCTION

Power electronics will play an important role in energy saving. Energy efficiency can make a significant contribution to meeting the world energy demand. A lift converter could be a particular kind of power converter with an output DC voltage greater than the input. This kind of circuit is employed to 'step up' a source voltage to the next, regulated voltage, allowing

one power supply to supply different driving voltages. In recent years, interleaved boost converters are like-minded for top-performance applications. The benefits of IBC include increased efficiency, reduced size, reduced electromagnetic emission, faster transient response, and improved reliability. The switching losses pre-dominate causing the junction temperature to rise which could be a major drawback of PWM switching. The soft switching phenomena called zero voltage switching (ZVS) and zero-current switching (ZCS) can reduce switching losses. For zero-voltage switching (ZVS), the transistor will be turned on at zero Vds voltage to cut back to activate switching loss. For zero-current switching (ZCS), the transistor is going to be turned off at zero Id current to cut back the put-off switching loss. The soft switching techniques reduce the switching losses enabling high-frequency operation and consequently reducing the system size and hence extending the facility density.

2. BLOCK DIAGRAM



1.Block diagram of Soft Switched interleaved boost converter

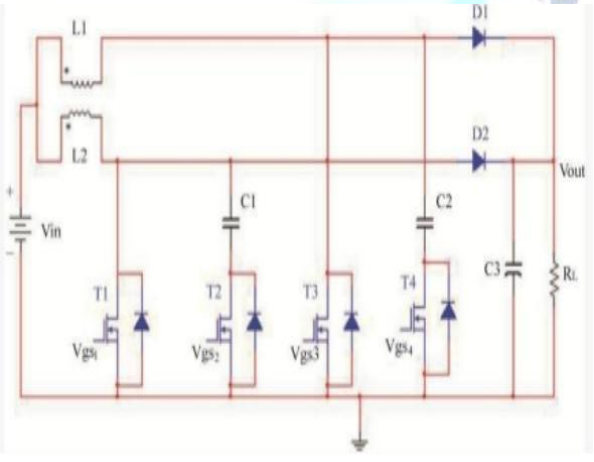
3. CIRCUIT DESCRIPTION & OPERATION

The passive snubber circuits are added to the converter to chop back the stresses to safe levels by limiting the speed of rising (di /dt) of currents through devices at device activate and limiting the speed of rising (dv /dt) of voltages across devices during reapplied forward blocking voltages and shaping of the switching trajectory of the device because it activates and off. The proposed soft-switching interleaved boost converter module. DC DC boost converters are connected in parallel which landsup within the reduction of the size of components, especially inductors. The complete power is split into paralleled converters thereby reducing the strain among the individual converters. During this paper, an N = 2 parallel boost converter structure with one output capacitor is taken under consideration as shown in fig.2. Within the circuit construction, the output current is split into two paths, substantially reducing I2R losses and inductor AC losses. Therefore, higher efficiency is realized. The MOSFETs with appreciable on-state current-carrying capability and off-state blocking voltage capability are potential candidates for power electronic applications. The diodes are placed in antiparallel with the switches. An outsized value of the capacitor is placed at the output to make sure the specified output voltage with negligible harmonics is out there at switching frequency. Fig.2 shows the equivalent circuit of the converter during which the coupled inductor is usually illustrated with three uncoupled inductors.

4. DESIGN GUIDELINES

In the proposed soft switched IBC, the inductors at the face in an IBC are magnetically coupled to enhance the electrical performance.

1. The four switches in Fig. 2 are often divided as two main switches T1 and T3 and two auxiliary switches T2 and T4.
2. The coupled inductor within the boosting stage helps higher current sharing between the switches.
3. The ripple and total harmonic distortions are reduced during this technique without sacrificing the performance and efficiency of the converter.



2.Diagram of Soft Switched Boost Converter

The interleaved boost converter design involves the selection of duty cycle, boost inductances L1 and L2, the values of coupling coefficient k, and the values of snubber capacitances C1 and C2. The calculations are

done by the use of the following equations. The duty cycle is calculated as

Duty cycle D = 1/2(1 -(Vin - Vout)……1

Where,

Vin= Input voltage

Vout= Desired output voltage

η= Efficiency of the converter, estimated 99%

Inductor Ripple Current Estimation:

ΔIL =(0.2 to 0.4) x IO × (Vout/Vin)

ΔIL = Estimated inductor ripple current

Io = Necessary output current

Vout = Desired output voltage

Vin = Input voltage

The conduction losses of the maximum switches and opposite recuperation losses of the diodes are substantially decreased with the aid of deciding on the really well worth of K = 0.98. The essential switches are turn-off, in the course of that duration the snubber capacitors C1 and C2 have a tendency to reduce the turn-off loss. The massive fee of capacitors appreciably reduces the loss. But, successively growing the power garage capacity, will increase the top fee of the prevailing and conduction losses of the switches. So, tradeoff takes place whilst the fee of snubber 's capacitors is calculated.

The proposed converter has the subsequent features:

✓ Low enter modern-day ripple because of interleaved technique.

✓ ZVS activates the energetic switches.

✓ ZCS turns off the energetic switches.

✓ Components voltage rankings are tremendously decreased.

✓ Reduced voltage stresses of switches and diodes.

✓ Extendibility to preferred voltage advantage and electricity level.

The layout equations for the proposed IBC are as follows:

The inductance value can be calculated as

L = (Vin x D) / (fs x ΔIL) ……2

Where, D=Dutycycle,

fs = Switching frequency of the converter,

ΔIL= Estimated inductor ripple current.

Output capacitance is

Co = (Io x D) / (fs x ΔVout)……3

Where,

Io= Necessary output current,

D =Duty cycle,

fs = Switching frequency of the converter,

ΔVout= Desired output voltage ripple.

The output voltage is

$V_o = V_{in} / (1 - D)$ ……4

Where,

Vin = Input voltage

D = Duty cycle

The experiment has been conducted on the designed circuit of a soft switched interleaved boost converter with 10 V input voltage and maintained the load current to 0.1 A. The commutation process is started by the active turn-on of most switches. It's noted that the drain-source voltage Vds1 reaches zero while most switches T1 and T3 were turned ON and thereby zero voltage switching operation was realized. The drain-source current ID1 reaches zero while most switches T1 and T3 were turned OFF and thereby zero current switching operation was realized. Then followed with delay, the identical switching operation was realized when the auxiliary switches T2 and T4 were operated in turned ON and turned OFF conditions.

5. SIMULATION OF SOFT SWITCHED INTERLEAVED BOOST CONDUCTOR

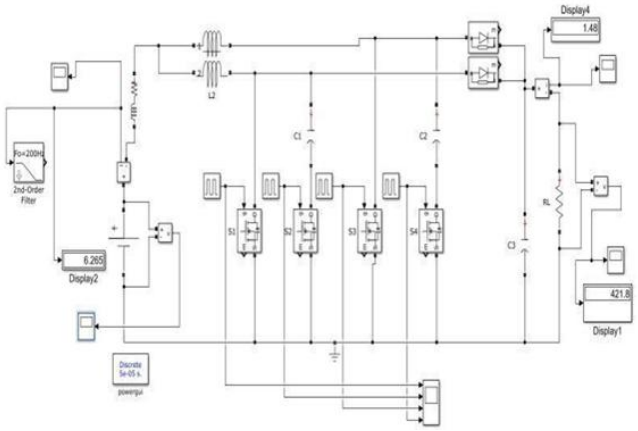


Fig 3 Simulation diagram of soft switched interleaved boost converter

6. SIMULATION RESULTS OF SOFT SWITCHED INTERLEAVED BOOST CONVERTER

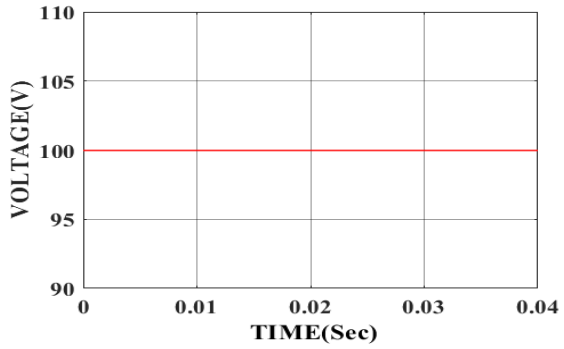


Fig 4 Input voltage waveform of soft switched interleaved boost converter

Input voltage is 100v and this is a constant voltage. Y-axis denoted as voltage . X-axis denotes time. The x-axis limit is 0 to 0.04sec. This is used to calculate the value of the inductor ripple.

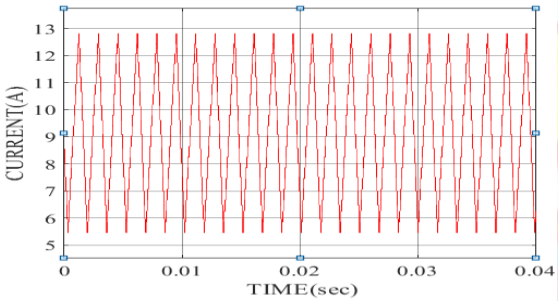


Fig 5 Input current waveform of soft switched interleaved boost converter

Y-axis denoted as current. X-axis denotes time. The x-axis limit is 0 to 0.04sec .The y-axis limit is 5 to 13 and the current value is obtained from this limit range.The input current is 6.265A.This value is used to calculate the inductor ripple value.

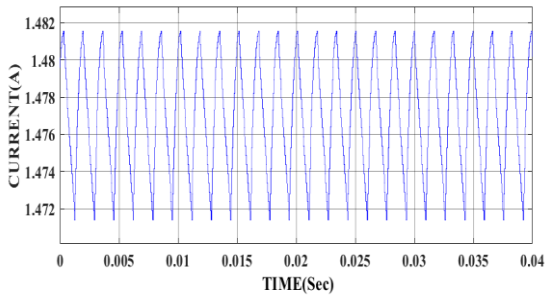


Fig 6 Output current waveform of soft switched interleaved boost converter

Y-axis denoted as current. X-axis denotes time. The x-axis limit is 0 to 0.04sec .The y-axis limit is 1.472 to 1.482 and the current value is obtained
from this limit range.The output current is 1.48A.

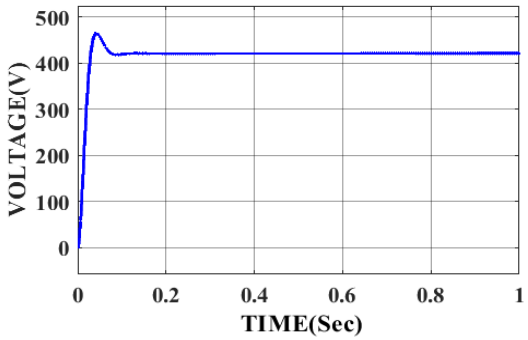


Fig 7 Output voltage waveform of soft switched interleaved boost converter

Y-axis denoted as voltage. X-axis denotes time. The x-axis limit is 0 to 1sec .This is used to obtain the voltage ripple.The minimum and maximum voltage are used to obtain the voltage ripple. The maximum voltage is 422.5V and the minimum voltage is 419V.
calculated the parameters of output ripple value is 1.2A and the efficiency of the converter is 99.64%

7. HARDWARE PROCESS

In soft switch interleaved boost converters consist of four switches. Two switches operate in forward conduction and another two switches operate in reverse conduction. The converter boosts the given voltage to 10 times. For example the input voltage is 10V and the output voltage is 100V.So the specification of the soft switched interleaved converter is different from the other converters. In this project, using the microcontroller is dsPIC30F2010. This microcontroller has 28 pins and four Pulse Width Modulations are used. In four Pulse Width Modulations, only two Pulse Width Modulations are axillary and other Pulse Width Modulations are main.In two Pulse Width Modulation voltage range is 5V. The Pulse Width Modulations connected in the transformer and the input of the Pulse Width Modulations is 12V is stepped down to 5V.It is connected in the next section isolator and drives. The purpose of the isolator and drives is to convert the 5V pulse to 12V pulse and give it to the Metal Oxide Semiconductor Field Emission Transistor. The input of the section is 12V. In a coupled inductor and four Metal Oxide Semiconductor Field Emission Transistors, the

capacitor voltage range is 100V, the load range is 10kΩ, 5W, input voltage is 10V.The alternate current input is converted to direct current.

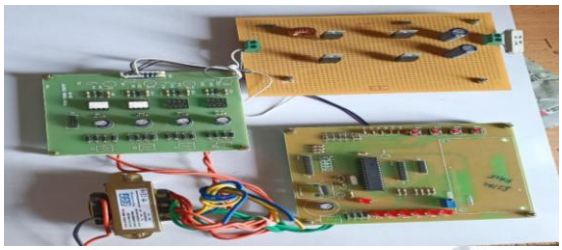


Fig 8 working module of the Soft Switched Interleaved Boost Converter

A.INPUT VOLTAGE

The applied input voltage of the system is 12V.When the switch ON capacitor is energized otherwise the capacitor is de-energized..It boosts the value of some value and gives a 15.3V final value. The multimeter is used to check the input Value. The input is an alternating current(ac).

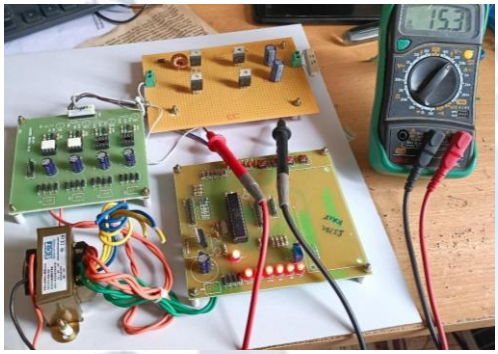


Fig 9 Input Voltage of the Converter

B.OUTPUT VOLTAGE

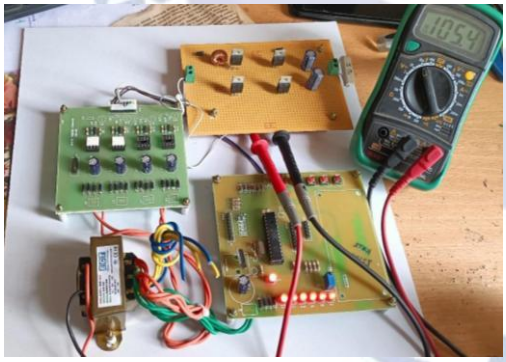


Fig 10 Output Voltage of the Converter

The output voltage of the converter is 105.4V.When the switch ON capacitor is energized otherwise the capacitor is de-energized. The converter boosts the given voltage to 10 times. The multimeter is used to check the output The output is a direct current(dc)

C.PULSE WAVEFORM

Soft Switching Interleaved Boost Converter. The pulse wave is a non-sinusoidal waveform that includes square waves and similarly periodic but asymmetrical waves. The voltage of the waveform is 500mV and time is1.0ms.It takes between the voltage regulator and the microcontroller.

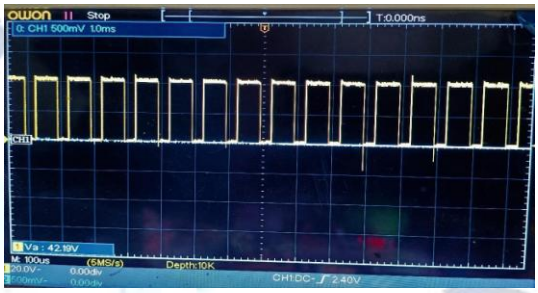


Fig 11 Pulse Waveform

8. CONCLUSION

A simulation implementation of conventional, bridge type, interleaved, and soft switched IBC was described in this article. The output voltage can be kept constant using this simulation, and it is also discovered that interleaved boost has the ability to share input current and reduce ripple current. Furthermore, this converter is designed to work in CCM mode at all times. The proposed converter can offer faster steady state response when the source voltage or load changes by employing Digital PWM approaches. Furthermore, research contributes significantly to the development of high-frequency, high-efficiency soft switching converters for power factor correction (PFC) of electronic power supply used in telecommunication switching systems. By using an FPGA-based digital controller, any one of the many current control techniques, such as average current control, hysteresis control, and non-linear carrier current control, can be implemented digitally

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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