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Design and Implementation of Decoder and MUX using Mixed Logic

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ABSTRACT

Mixed logic designs take prioritized place in logic design approaches which will give a simplified mechanism for the analysis of digital circuits. Also, a mixed logic implementation gives clear idea with regards to the activity of a circuit. Here in this, introduced mixed logic designs like pass transistor dual value logic (DVL), transmission gate logic (TGL), static CMOS. By using CMOS technology, it requires 20 transistors to design 2:4-line decoder but by using mixed logic we can design the same 2:4-line decoder with the use of 14transistors (14T) only. Introducing mixed logic approach a 4:1 MUX was designed by using 2:4-line decoder of mixed logic design. This new approach gives the better operating speed, low power consumption compared to conventional logic design by reducing the transistors activity and simulations are carried out using tanner EDA tools.

KEYWORDS: Mixed logic, Low power MUX, Line decoder, Transmission gate logic (TGL), Dual value logic (DVL) & Static CMOS

1. INTRODUCTION

In most of the integrated circuits, we generally prefer Static CMOS because of complementary nMOS and pMOS networks which results in good performance as well as resistance to noise and device variation. But by using CMOS technology, it requires 20 transistors to design 2:4-line decoder but by using mixed logic we can design the same 2:4-line decoder with the use of 14transistors (14T) only. Pass transistor logic (PTL) was developed as an alternative to CMOS logic. The main difference between the CMOS logic and PTL design is how the inputs are applied. In the PTL inputs are applied on the gates as well as source/drain terminals. PTL can be designed using either of nMOS and pMOS. The DVL has advantages over the PTL such as full swing operation while also maintaining reduced transistor count. A pair of nMOS and pMOS connected in parallel are called TGL.

2–4 Line Decoder: 2-bit input line decoder has 4-bit output. In conventional static CMOS line decoder uses 2 NOT gates and 4 AND gates. Instead of using AND gates we can use NAND gates as they are universal gates. So, for this design it uses 20 transistors for 2–4-line decoder.

4x1 Multiplexer: It consists of 4 input lines and 1 output. The selection line decides which inputs should go to the output. The conventional CMOS design for 4x1 mux uses 2 NOT gates, 4 3-input AND gates and 1 4-input OR gate. The total transistor count for this conventional design 4x1 line multiplexer is 46 Transistors.

2. MIXED LOGIC

CMOS LOGIC:

A static CMOS circuit is composed of two networks: Pull-up network (PUN) - a set of PMOS transistors connected between V_{cc} and the output line. Pull-down network (PDN) - a set of NMOS transistors connected between GND and the output line. The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS).

TRANSMISSION GATE LOGIC:

The PMOS and the NMOS transistors present in the circuit are always connected in parallel which are managed via complementary signals. Combining an NMOS and PMOS back-to-back will make the resulting transmission gates to pass a good active low "0" and also a good active high "1" signal.

DUAL VALUE LOGIC:

The Pass transistor logic is required to reduce the transistors for implementing logic by using the primary inputs to drive gate terminals, source and drain terminals. In complementary CMOS logic primary inputs are allowed to drive only gate terminals. There are several pass transistor logics are developed. The best possible pass transistor logic is Dual Value Logic which is to be consider for our comparisons. DVL is basically derived from DPL. The elimination of redundant branches and rearrangement of signals allows the DVL is advantageous compared to DPL. The speed compensation degrades due to PMOS transistors and straightforward full swing operation make it possible to use DVL logic style.

3. IMPLEMENTATION

3.1 Decoder using CMOS logic

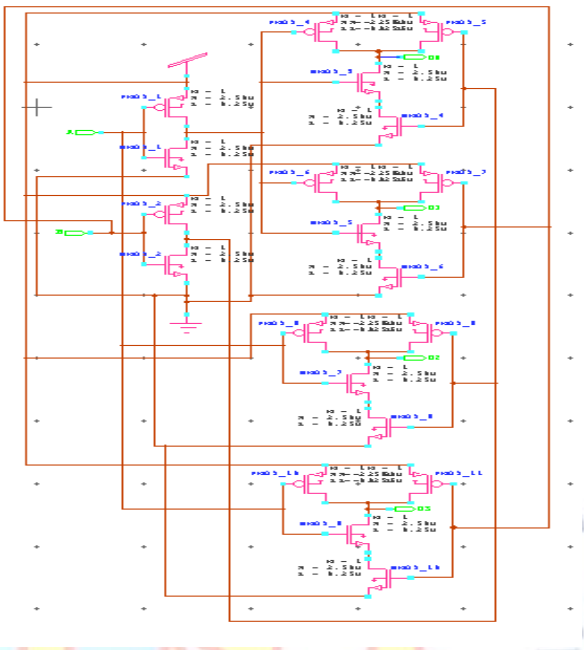

Figure 1: 20T CMOS Decoder

The decoder is the standard CMOS decoder that uses 20 transistors as shown in figure 1. This design requires 20 transistors thus, the power consumption, delay and the complexity are more for larger designs.

3.2 Decoder using mixed logic

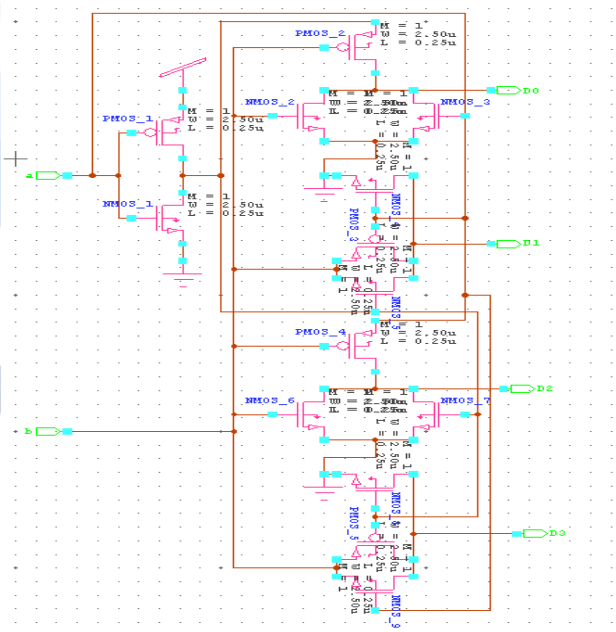

Figure 2: 14T mixed logic Decoder

The mixed logic design for decoder is shown in above figure 2. The mixed logic decoder is designed with 14T. It Reduces transistors count. Hence, low power consumption, delay is reduced and smaller area can be achieved.

3.3 4:1 MUX using CMOS logic

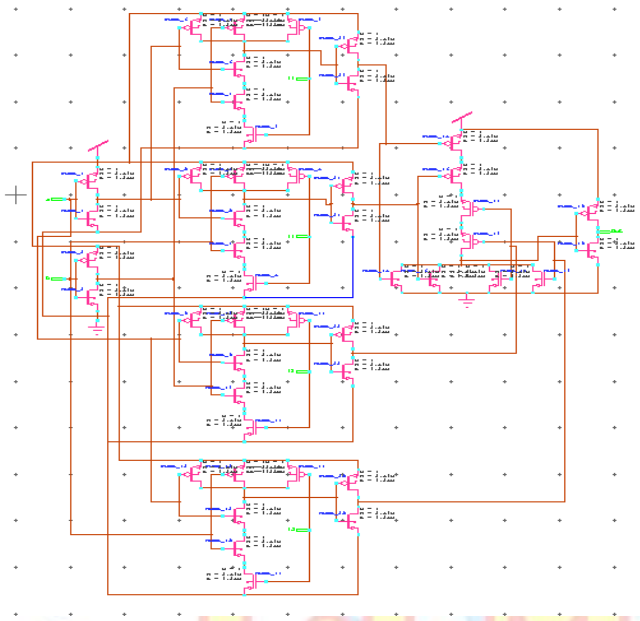

Figure 3: 46T CMOS 4:1 MUX

The 4:1 Mux using CMOS logic is shown in above figure 3. To design CMOS 4:1 MUX total 46 transistors were used. The 46T MUX using AND and OR gates consume more power due to a greater number of transistors.

3.4 4:1 MUX using mixed logic

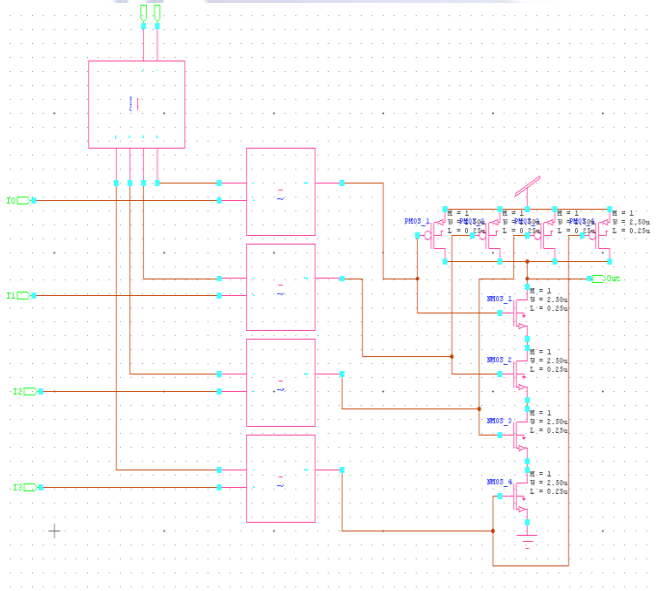

Figure 4: 38T mixed logic 4:1 MUX

The 4:1 MUX using mixed logic is shown in above figure 4. The design has totally 38 transistors using 2:4-line decoder mixed logic style. Instead of AND and OR gates NAND gates are used to design the mixed logic style for 4:1 MUX. It reduces the transistors count when compared to conventional CMOS. Hence, power consumption is low and delay is reduced.

4. SIMULATION RESULTS

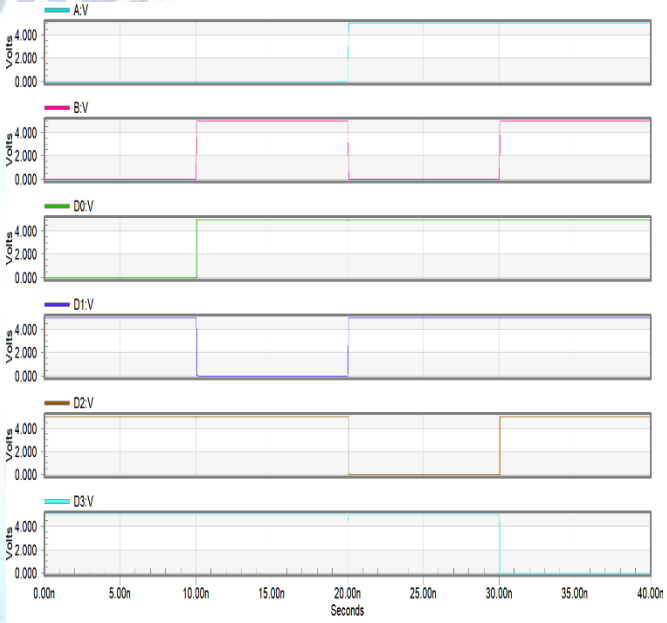

Figure 5: Input and Output waveforms of CMOS Based Decoder using NAND gates

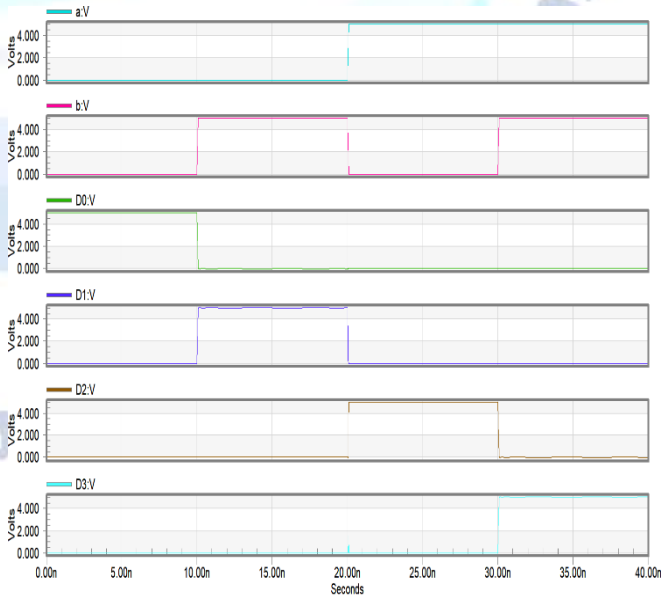

Figure 6: Input and Output waveforms of mixed logic Based Decoder using NAND gates

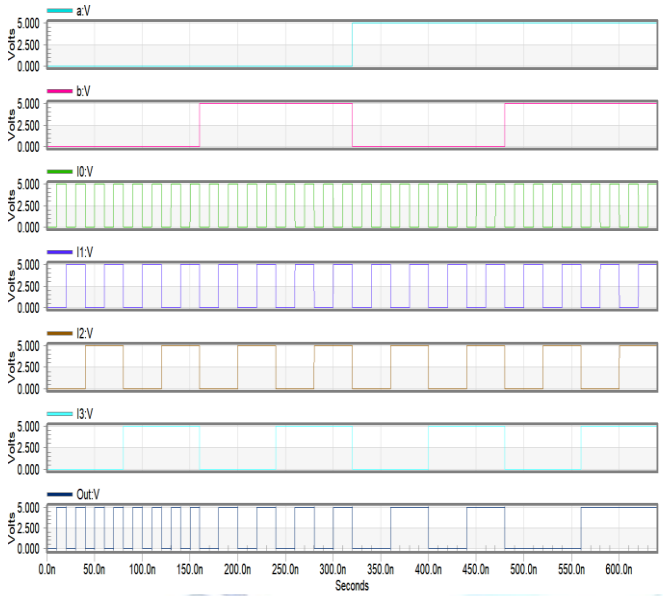

Figure 7: Input and Output waveforms of CMOS Based 4:1 MUX using AND and OR gates

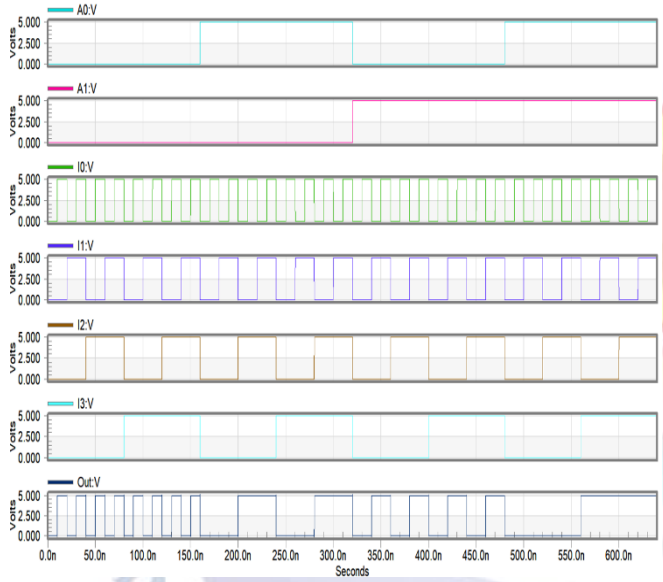

Figure 8: Input and Output waveforms of mixed logic Based 4:1 MUX

4.1 Comparison Table

Table 1: Comparison between CMOS and Mixed logic styles

LOGIC	No. of T	SUPPLY	POWER	DELAY
CMOS	46	5V	4.6893uw	17.0270ns
MIXED	38	5V	2.1655uw	10.0244ns

5. FUTURE SCOPE AND CONCLUSION

5.1 Conclusion

This Paper introduced a mixed logic design for a multiplexer aiming for low power and reduced area in consideration. By using a line decoder, we tried to achieve this low power MUX by using mixed logic design. And instead of AND, OR gates we used NAND gates to further reduce the Transistor count, power consumption and area. The proposed design is compared to the conventional CMOS design. The line decoder is designed with TGL, DVL and the NAND gates are static CMOS, by combining these 3 logics designs we can have a mixed logic design.

5.2 Future Scope

In future the mixed logic design can be implemented in various digital circuits and the sequential circuits. As the proposed designs have proven to work efficiently in terms of various performance parameters thus; the more effective results are expected to be obtained while incorporating these circuits to implement other complex systems in the field of low power VLSI design.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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