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Design and Implementation of 6T SRAM using FINFET for Low Power Applications

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ABSTRACT

Conventional CMOS is used to design SRAM for storing data in memory. Due to the loss of control over the channel, many devices such as logic and memory are facing various problems. These include high power consumption, low leakage current, and short channel effects which results in less reliability and large variations in parameters and increase in manufacturing cost. Due to these issues, it is recommended to use FINFET based SRAM cells instead of conventional CMOS ones.The power dissipation and leakage currents of SRAM cells have been considered as one of the main factors that have to be reduced in order to improve the stability of the cell. There are many low power techniques which are used to reduce the power dissipation and leakage currents. These include MultiThreshold CMOS (MTCMOS), variable threshold CMOS (VTCMOS), Stacking technique, power gating, Self controllable voltage level (SVL) technique etc . In this paper we propose the use of MTCMOS technique to design a FINFET SRAM cell and compare it with FINFET SRAM cell in terms of dynamic power dissipation. All the simulation are done on Synopsis Hspice Tool using 32nm technology.

KEYWORDS: CMOS, FINFET, SRAM, MTCMOS , DYNAMIC POWER DISSIPATION

1. INTRODUCTION

With advancements in the VLSI industry, FINFET SRAM has emerged as a new technology that provides a very low size transistor design to meet the demand for improved storage. The three-dimensional design of the gate, which reduces the gate's control dependencies over conventional drain and source terminals, is the driving force behind this breakthrough technology. The short channel effect is a problem in traditional transistor design that is totally eliminated by the current FINFET design paradigm. Conventional MOSFETs also have a difficulty with arbitrary dopant fluctuations, which is eliminated by the FINFET because it lacks a channel doping mechanism. There are fewer energy points and points for the product of delay and energy in FINFET circuits than in planer CMOS circuits, resulting in lower levels of supply voltage. As a result of the FINFET, voltage stability is improved. Simultaneously, memory storage systems like as SRAM suffer from high cache memory occupancy in the chip region, as well as high chip power consumption.

A. CMOS BASED SRAM

The key component for storing a single bit of binary data is an SRAM cell. In the near future, memory circuits, mostly caches, are expected to comprise more than 90% of the chip silicon area. As a result, its design and testing are both robust and error-free. Because of its low static power dissipation in many circuit topologies, a 6T CMOS

SRAM cell is widely common in the IC sector. Furthermore, the CMOS Cell has better noise margins. Figure 1 depicts a typical MOSFETbased 6-T SRAM cell. It has two cross coupled inverters that create a latch and two n-type access transistors. The word line (wl) is connected to the gate terminal of the access transistors, while the bit line (bl) and bit line bar (blb) are connected to the source terminal. The access transistors must be turned on whenever the memory element is used for a read or write operation. There is a demand that SRAM cells have a broad noise margin and fast speed, yet this poses a big challenge because high speed increases leakage power.

Another issue with typical planar SRAM is that the design idea of SRAM is based on large scaled technology, which results in a smaller size with lower supply voltage. This results in a small voltage difference between the cut-off and supply voltages. This small discrepancy can become tremendously unstable, especially when the design calls for increasing the number of transistors while reducing their size to retain huge storage sites. The stability, power consumption, and access time of an SRAM cell all influence device design of an SRAM.

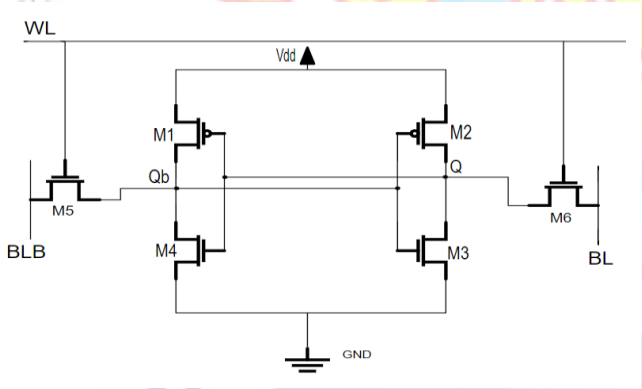

Fig.1. CMOS BASED SRAM CELL

The waveforms of CMOS SRAM Write Operation after performing transient analysis are shown in the below figure.

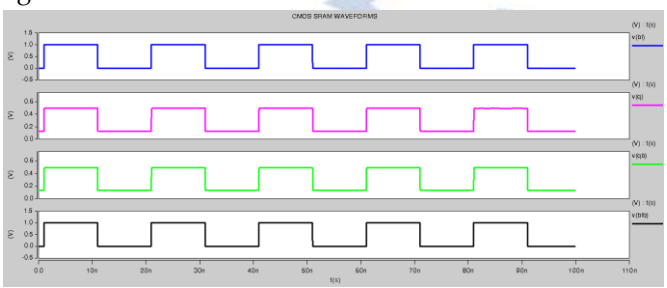

Fig.2.CMOS SRAM WAVEFORMS

The Power Waveform of the CMOS SRAM is shown in below figure.

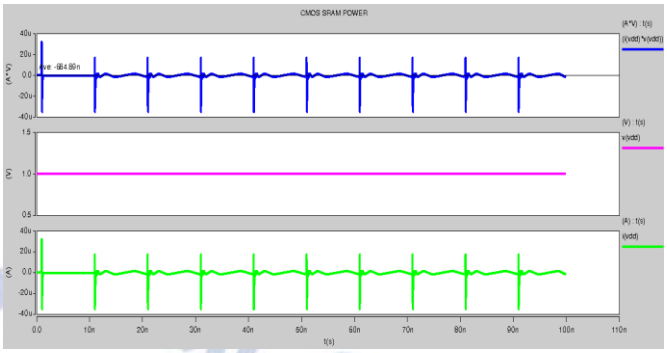

Fig.3.CMOS SRAM POWER WAVEFORM

B. FINFET 6T SRAM CELL

In the future, memories are projected to be a major component of the design. Scaling becomes significantly more difficult and critical as a result of this fact. The electrostatic control of a gate in a FINFET is improved due to gate control from several sides of the fin. Multigate MOSFETs enhance short channel effects such as subthreshold degradation, Vth roll of width length, and drain induced barrier lowering (DIBL). Because quick access times, low power dissipation, and low leakage current are required in memories, FINFET-based SRAM cells are recommended over CMOS-based SRAM cells.Because of their low power dissipation, FINFET-based SRAM cells are more prevalent.

The structure of a FINFET-based 6T SRAM cell differs from that of a traditional 6T SRAM cell.The FINFETS we used here are Independent Gate Mode FINFETs.The circuit contain two FINFET-based access transistors and two crosscoupled inverters as the basic memory element. The word line (wl) is connected to the gate terminal of the access transistors, while the bit line (bl) and bit line bar (blb) are connected to the source terminal.The back gate of the each FINFET is shorted to the source terminal.The access transistors must be turned on whenever the memory element is used for read or write operations. The access transistors are turned on through the word line during writing and reading operations on the SRAM cell, but they are turned off during the hold state. The 6T SRAM cell design based on FinFETs is as shown in fig 4.

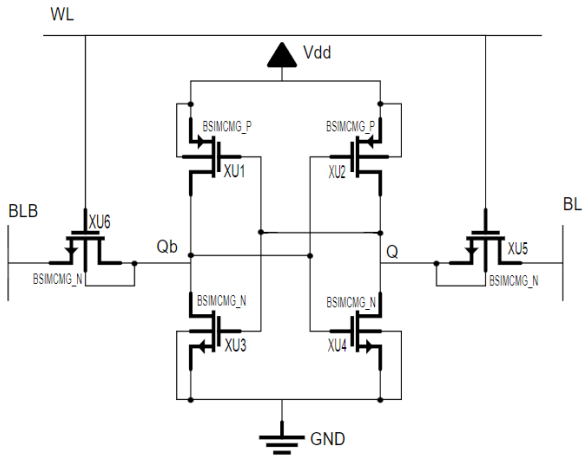

Fig.4.FINFET BASED SRAM CELL

The waveforms of FINFET SRAM Write Operation after performing transient analysis are shown in the below figure.BL and BLB are inputs and Q and Qb are outputs.

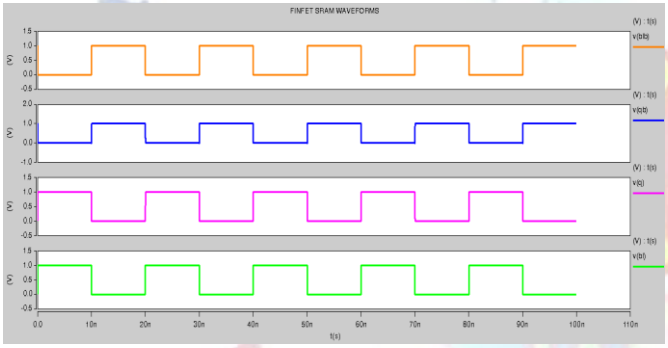

Fig.5.FINFET SRAM WAVEFORMS

The Power Waveform of the FINFET SRAM is shown in below figure.

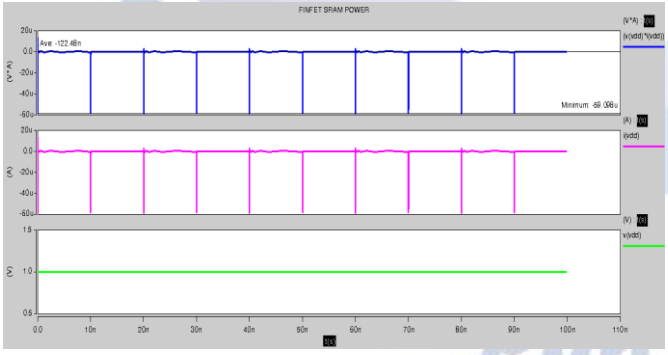

Fig.6.FINFET SRAM POWER WAVEFORM

2. DESIGN TECHNIQUES FOR REDUCING THE LEAKAGE POWER FOR LOW POWER SRAM

Most microelectronic frameworks invest impressive time and energy in a standby state. The vitality of the DC-DC converter to enter or leave a low power mode must be considered deliberately. In the event that the cost of transitioning to and from a low standby power state is sufficiently low then the policy of entering the low power state when the system is in idle state might be adopted. In that place the expected duration of the standby state must be precisely computed and considered when we are using a power management approach. In the following area, techniques are exhibited for decreasing the subthreshold leakage currents that are in STANDBY or ACTIVE model. One such technique is multithreshold CMOS (MTCMOS).

A. MULTITHRESHOLD CMOS (MTCMOS)

Multi-threshod CMOS (MTCMOS) is a type of CMOS device that has transistors with various threshold voltages (Vth), with the purpose of reducing latency or increasing power. The threshold voltage of the transistor is essentially the gate voltage at which an inversion layer forms at the interface between the gate oxide layer and the substrate (body) of the transistor. Low Vth devices flip quickly, making them useful for limiting clock durations on crucial delay lines. Low Vth devices have much higher static leakage power, which is a disadvantage.On non-critical channels, high Vth devices are used to reduce static leakage power. In comparison to low Vth devices, high Vth devices reduce static leakage by ten times.In this MTCMOS SRAM we use the combination of both P type FINFET and N type FINFET.We implement this circuit by having low Vth(Threshold Voltage) as the logic circuit and high Vth devices at the top and bottom of the circuit.

The sleep transistor is turned on in the ACTIVE state.Due to the high threshold voltage of sleep transistors leakage is reduced and the circuit function stays unchanged. The transistor is turned off in the STANDBY state, which disconnects the gate from the ground. It's worth noting that the sleep transistor's threshold voltage needs to be higher to reduce leakage.The sleep transistor will have a significant leakage current if this requirement is not met, making power gating less viable. If the width of the sleep transistor is lower than the combined width of the transistors in the pull down circuit, less leakage may be achieved. The sleep transistor must be purposefully sized to minimise its voltage loss while it is on to ensure the circuit's correct functionality. The voltage loss on the sleep transistor lowers the logic gate's effective supply

voltage. Due to the body effect, it also causes an increase in the threshold voltage of pull down transistors.

B. DESIGN OF MTCMOS FINFET SRAM

Low threshold voltage transistors are isolated from the power source in the MTCMOS approach by using a high threshold sleep transistor on the top and base of the logic circuit. To plan logic, a transistor with a low threshold voltage (low-Vth) is used. The clock signal is used to control the sleep transistors. The clock signal is made high in dynamic mode, causing both high Vth transistors to flip on, providing virtual power and ground to the low Vth logic circuit. The sleep signal is made to go low while the circuit is in standby mode, forcing both high Vth transistors to cutoff and disconnect power supply source (VDD) cables from the low Vth logic circuit. In standby mode, this results in a low leakage current from the power supply source to ground. One disadvantage of the MTCMOS process is the enormous number of sleep transistors, which makes circuit sizing difficult for very large circuits. The schematic of a FINFET-based SRAM CELL using the MTCMOS approach is shown in Figure 7.

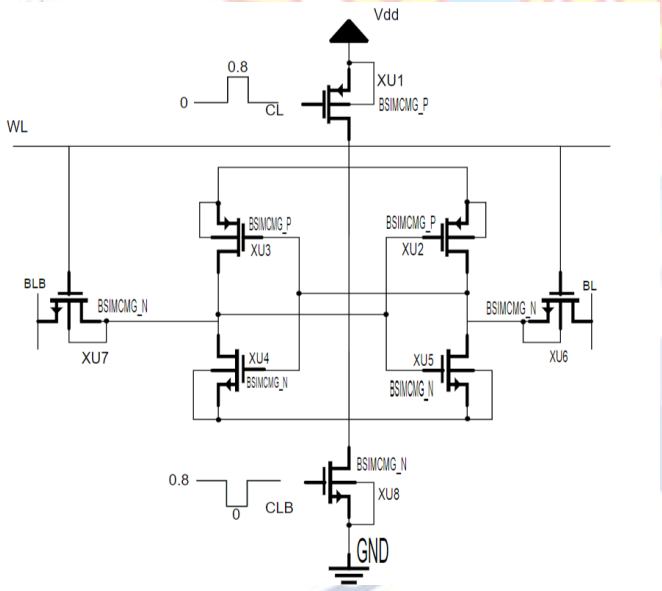

FIG.7.MTCMOS FINFET SRAM CELL

3. IMPLEMENTATION OF FINFET SRAM USING MTCMOS

This technique reduces standby power by using pFET switches with a higher threshold voltage Vthp in between the power supply and the low Vth SRAM cell transistor for disconnecting the power supply, and nFET switches with a higher threshold voltage Vthn in between the ground and the low Vth SRAM transistor for disconnecting the ground from the low Vth SRAM cell for disconnecting the ground from the low Vth SRAM cell. Low Vth transistors can operate at fast speeds and with low switching power dissipation in active mode. When the circuit is in sleep mode, the high Vth sleep transistors are turned off, causing the low Vth transistor to be disconnected from the supply voltage and ground, minimising sub-threshold leakage current. The MTCMOS approach has a number of major drawbacks, including the necessity for extra manufacturing processes for greater Vthp and Vthn, as well as the fact that data cannot be restored by storage circuits based on this technique.

A. WAVEFORMS OF FINFET SRAM USING MTCMOS

The clock pulses cl and clb applied to high threshold voltage circuits shown in the circuit are taken complementary to each other and as shown in the given figure.

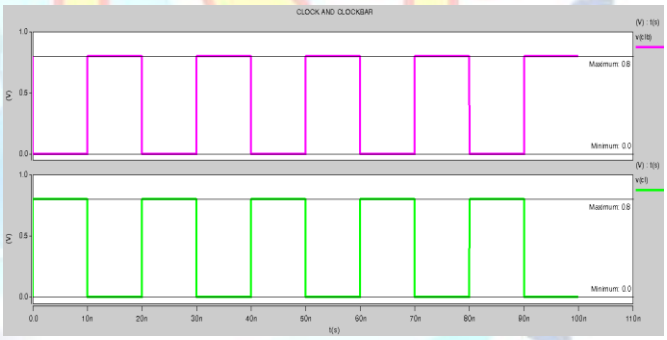

Fig.8. cl and clb for MTCMOS FINFET SRAM

Here we have taken Vdd=0.8 and wl as a pulse of 0 - 0.8 and also bl as 0 - 0.8 and blb as 0.8 - 0 over a period of 100ns. The respective waveforms of MTCMOS FINFET SRAM during WRITE Operation are given below.

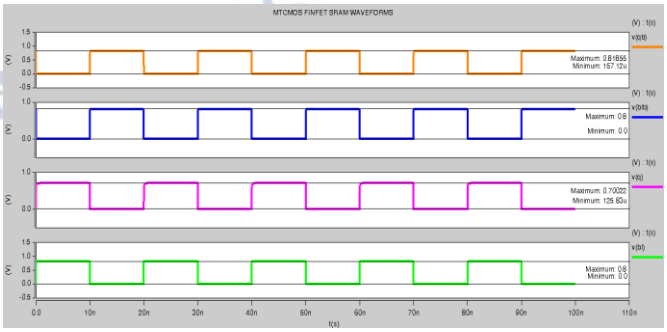

Fig.9.MTCMOS FINFET SRAM WAVEFORMS

The Power Waveform of the MTCMOS FINFET SRAM is shown in below figure.

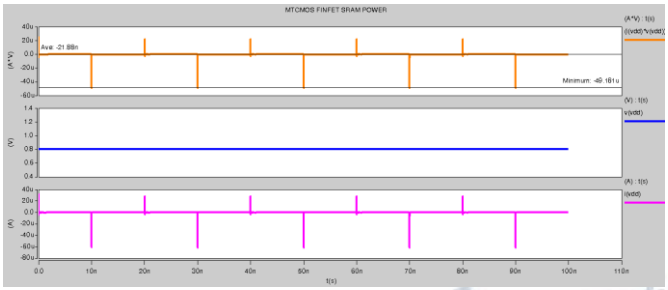

Fig.10. MTCMOS FINFET SRAM POWER WAVEFORM

TABLE I

COMPARISON OF DYNAMIC POWER DISSIPATION OF SRAM IN WRITE OPERATION

S.No	Circuit	Dynamic Power Dissipation
1.	CMOS SRAM	685nw
2.	FINFET SRAM	122nw
3.	MTCMOS FINFET SRAM	22nw

4. RESULTS

The Synopsis HSpice tool is used to simulate MTCMOS FINFET SRAM utilising 32nm technology. The dynamic power dissipation, which is essentially the product of the power supply and the current, is calculated. In the case of MTCMOS FINFET SRAM, the dynamic power dissipation obtained is 21.88nw approximately equal to 22nw. When compared to FINFET SRAM, the MTCMOS method reduces dynamic power dissipation to a greater extent.

5. CONCLUSIONS

This paper describes how to create a FINFET SRAM cell using MTCMOS. Static memory cells are made up of two inverters connected back to back. The second inverter's output is connected to the first inverter's input. Two access transistors are also included. The bit line is connected to the source terminal of access transistors. Only when access transistors are turned on through the word line and turned off during the hold state are write and read operations possible. The sleep transistor is connected to the power supply and low vth circuit or to the low Vth circuit and ground. The dynamic power dissipation is computed by multiplying the current component by the power supply. Each design's operation is justified by proper simulation results. Synopsis HSpice programme was used to design all circuits, which were made in 32nm technology.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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