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Design of low power FinFET circuits using Adiabatic Logic in 32nm technology

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ABSTRACT

Exposure to the Internet of Things (IoT), has increased the urge to design energy-efficient and secure devices.With the increase in wireless devices, leakage power increases, which in turn increases their vulnerability to DPA attacks. These attacks happen whenever there is leakage in the power of a device. By reducing the power leakages, DPA attacks can be reduced, which in turn helps in maintaining secured data transmission between two or more devices. Adiabatic logic is used to encrypt the data by hiding the original data which helps the hackers to get confused. The FinFET based adiabatic logic circuits are energy-efficient and consume low power compared to normal FinFET or conventional CMOS circuits.

In this paper, the proposed adiabatic logic is used to design logic gates such as buffer, and/nand, and xor/xnor circuits. Using 32nm technology these three basic FinFET circuits have been designed. The average power of the circuits has been computed and the reduction in the power consumption has been calculated.

KEYWORDS: Adiabatic Logic, FinFET, Low Power VLSI Design

1. INTRODUCTION

Adiabatic logic is a widely used method to design energy-efficient and secure circuits. It has been demonstrated that adiabatic logic is one of the most promising techniques in dealing with DPA attacks. Techniques such as SymmetricPass Gate Adiabatic Logic (SPGAL) are used in the design of hardware that is secure and consumes minimum power. These systems are most flexible to implement in IoT devices. The drawback of SPGAL is its high leakage power at lower technology nodes. An increase in leakage current decreases the energy-efficiency of the circuits. This in turn makes the device more exposed to DPA attacks. To reduce these attacks low power leakage devices like FinFETs can be used.

The verification of results has been performed through HSPICE simulations in 32nm technology. As compared to conventional CMOS, FinFET based circuits can save energy up to 57% to 60%. Wireless sensor networks and their applications are in great demand in the current day. A circuit contains various components such as transistors, transformers, diodes, batteries, and other components. Each of these consumes a certain amount of power which contributes to the overall power consumption of the circuit. Information or data is leaked through power consumption. Hence, low power-consuming devices are less prone to DPA attacks. This paper presents a new charge recovery logic for resistance against side-channel attacks which are also known as DPA attacks. As FinFET is known for its high speed of

operation, the delay in the complex circuits can be reduced and the aim to design low power consuming circuits can also be acquired.

2. FinFET Device

The FinFET consists of the gate wrapping the channel in all three directions. The FinFET device structure is shown in Fig.1.

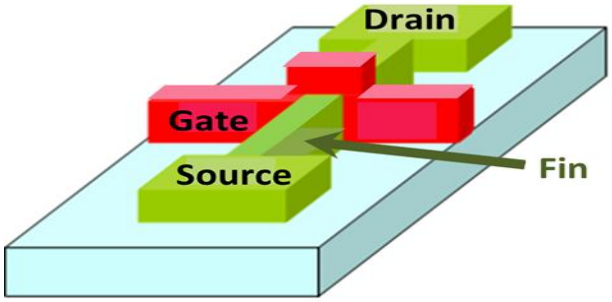

Fig. 1. FinFET Structure

There are two important modes in the FinFET, which are shorted-gate mode and independent-gate mode.

Shorted-gate mode: This mode consists of three terminals, source, gate, and drain. In this mode, the threshold voltage can't be controlled externally, but it occupies less area. In this mode, the front gate and the back gate are shorted so that there will be only one gate as shown in Fig.2.

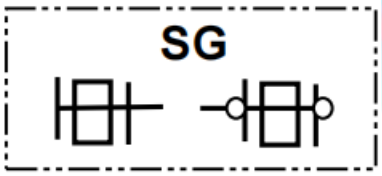

Fig. 2. Shorted-gate mode.

Independent-gate mode: This mode consists of four terminals, source, front gate, back gate, and drain. In this mode, the front and back gates work independently and the threshold voltage can be controlled. In this paper, we are using the independent-gate mode.

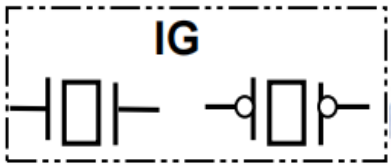

Fig. 3. Independent-gate mode.

3.FinFET based Adiabatic logic

Adiabatic logic is an effective method to recycle the charge stored in the load capacitor using power clocks. The advantage of this method is a reduction in dynamic switching energy loss due to charge recycling. The charging/ discharging of the load capacitors is shown in Fig.4.

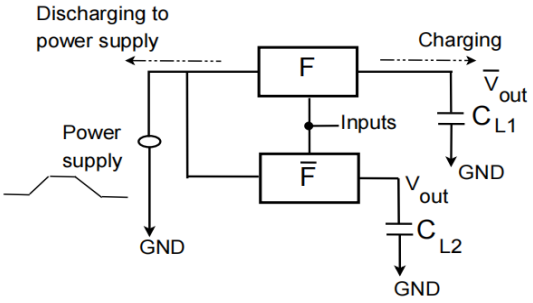

Fig. 4. Adiabatic Working

When a constant current source is supplying the charge, the dissipated energy in an adiabatic circuit is

$$E_{diss} = \frac{RC}{T}\left(CV_{DD}^2\right) \rightarrow (1)$$

In equation (1), C represents the load capacitor. VDD represents the full swing of the power clock. T is the charging and discharging time of the capacitor. Energy dissipation in adiabatic circuits is less than the conventional CMOS. As T approaches infinity, dissipated energy becomes equal to zero.

4. IMPLEMENTATION OF FINFET BASED ADIABATIC LOGIC CIRCUITS AND RESULTS

The schematics of FinFET buffer, FinFET and/nand, and FinFET xor/xnor gates were designed using a .sp file and by performing transient analysis in HSPICE software. The power consumption of the circuits was calculated.

A. Design of FinFET Buffer Gate

The schematic of the buffer circuit with FinFETs in the independent-gate mode has been designed. To build a buffer circuit, a four transistor structure is constructed which is used for the pull-up and pull-down of the transistors.

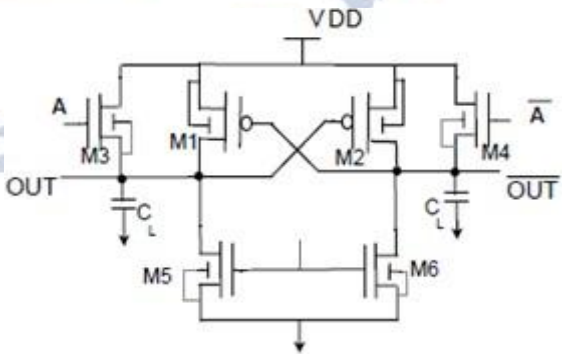

Fig. 5. Schematic of FinFET Buffer

Whenever the input A is high then the OUT is pulled up to Vdd. Hence, A' and OUT' becomes low and vice versa.

The waveforms of the buffer after performing transient analysis were shown in Fig.6 and Fig.7.

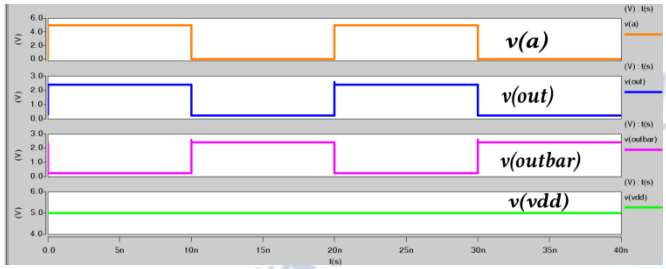

Fig. 6. Voltage waveforms of FinFET Buffer

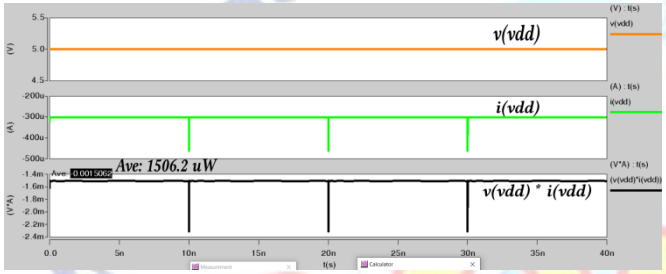

Fig. 7. Power waveform of FinFET Buffer

The average power consumed by the buffer circuit is 1506.2uW.

B. Design of FinFET Buffer Gate with Adiabatic Logic

The schematic of the FinFET buffer with adiabatic logic has been designed as follows. The 32nm technology FinFETs have been used. In the buffer with an adiabatic logic design, a clock pulse is applied as the supply.

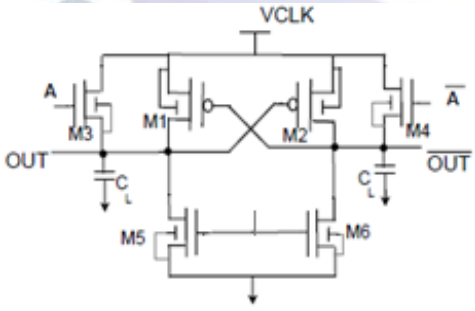

Fig. 8. Schematic of FinFET Buffer with Adiabatic Logic.

The transient analysis was performed for 40ns, the voltage waveforms and the average power consumption wave formof the buffer circuit were shown in Fig. 9 and Fig. 10.

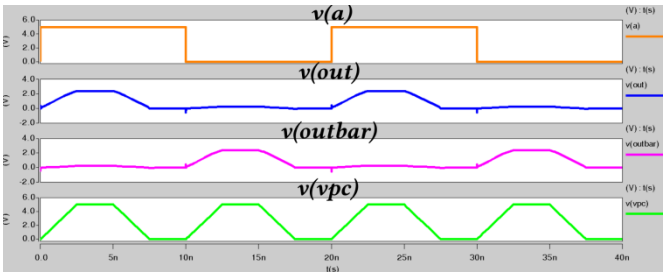

Fig. 9. Voltage waveforms of FinFET Buffer with Adiabatic Logic.

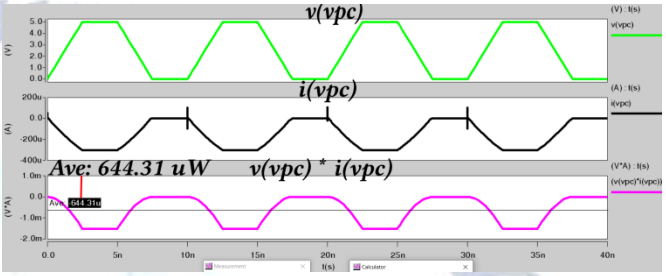

Fig. 10. Power waveform of FinFET Buffer with Adiabatic Logic.

The average power consumption of the circuit is computed to be 644.31uW.

C. Design of FinFET and/nand Gate

The schematic of the and/nand circuit with FinFETs in the independent-gate mode has been designed. To build a and/nand circuit, a four transistor structure is constructed which is used for the pull-up and pull-down of the transistors.

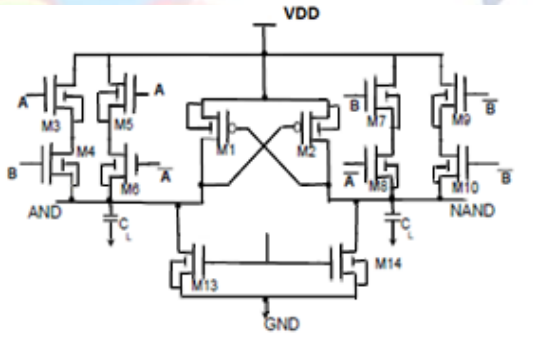

Fig. 11. Schematic of FinFET and/nand.

To secure 'and' output, the output of the left side circuit which is consisting of four transistors should be high, so that the and output is pulled up to the highest voltage. To secure 'nand' output, the output of the right side circuit which is consisting of four transistors should be high, so that the nand output is pulled up to the highest voltage.

The waveforms of the and/nand after performing transient analysis were shown in Fig. 12 and Fig. 13.

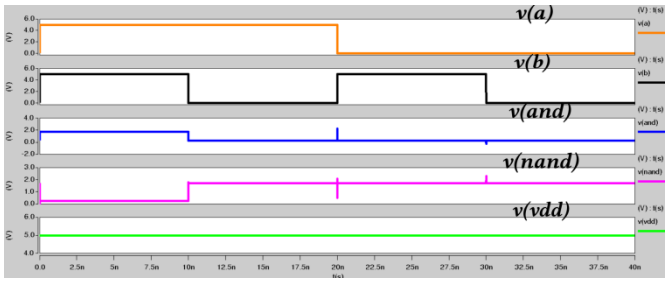

Fig. 12. Voltage waveforms of FinFET and/nand.

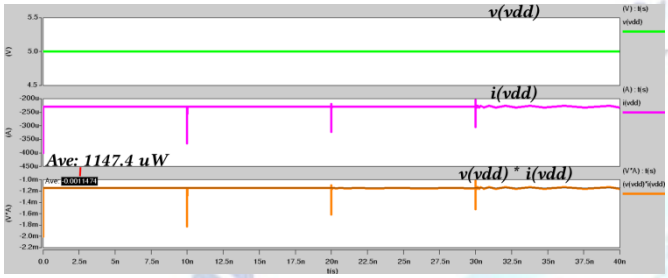

Fig. 13. Power waveform of FinFET and/nand.

The average power consumed by the and/nand circuit is 1147.4uW.

D. Design of FinFET and/nand Gate with Adiabatic Logic

The schematic of the FinFET and/nand with adiabatic logic has been designed as follows. The 32nm technology FinFETs has been used. In the and/nand with adiabatic logic design, a clock pulse is applied as the supply.

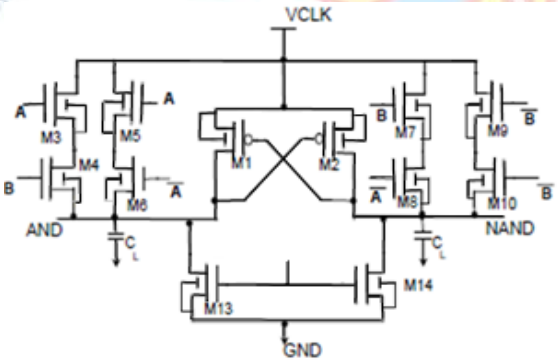

Fig. 14. Schematic of FinFET and/nand with Adiabatic Logic.

The transient analysis was performed, and the wave forms of the and/nand circuit were shown in Fig. 15 and Fig. 16.

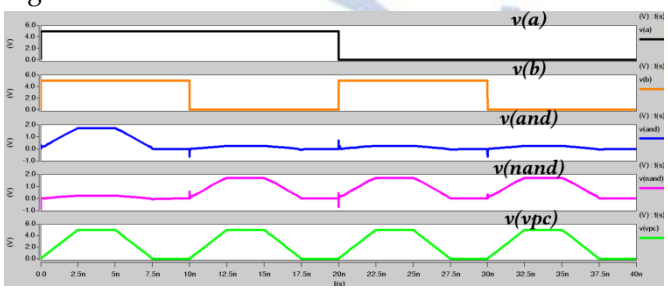

Fig. 15. Voltage waveforms of FinFET and/nand with Adiabatic Logic.

The average power consumption of the circuit is computed to be 489.14uW.

E. Design of FinFET xor/xnor Gate

The schematic of the xor/xnor circuit with finfets in the independent-gate mode has been designed. To build a xor/xnor circuit, a four transistor structure is constructed which is used for the pull-up and pull-down of the transistors.

To secure 'xor' output, the output of the left side circuit which is consisting of four transistors should be high, so that the xor output is pulled up to the highest voltage. To secure 'xnor' output, the output of the right side circuit which is consisting of four transistors should be high, so that the xnor output is pulled up to the highest voltage.

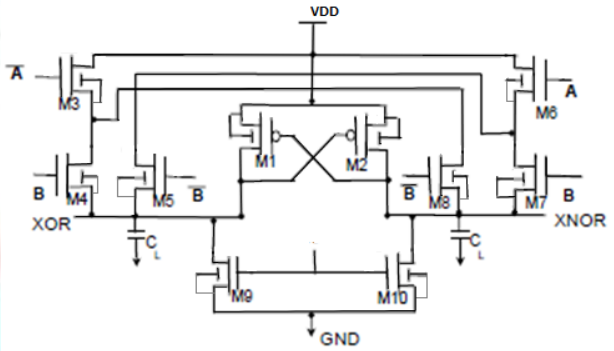

Fig. 17. Schematic of FinFET xor/xnor.

The waveforms of the xor/xnor after performing transient analysis were shown in Fig. 18 and Fig. 19.

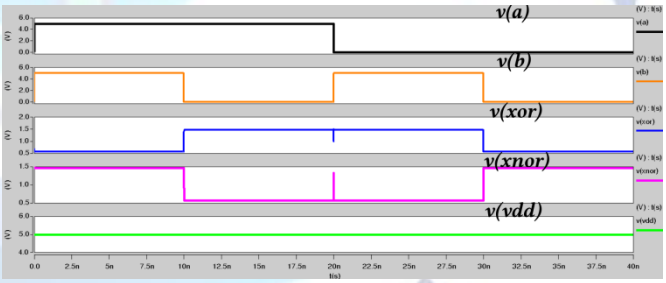

Fig. 18. Voltage waveforms of FinFET xor/xnor.

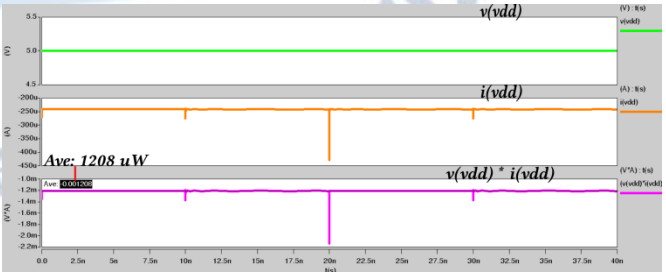

Fig. 19. Power waveform of FinFET xor/xnor.

The average power consumed by the xor/xnor circuit is 1208uW.

F. Design of FinFET xor/xnor Gate with Adiabatic Logic

The schematic of the FinFET xor/xnor with adiabatic logic has been designed as follows. The 32nm technology FinFETs have been used. In the xor/xnor with adiabatic logic design, a clock pulse is applied as the supply.

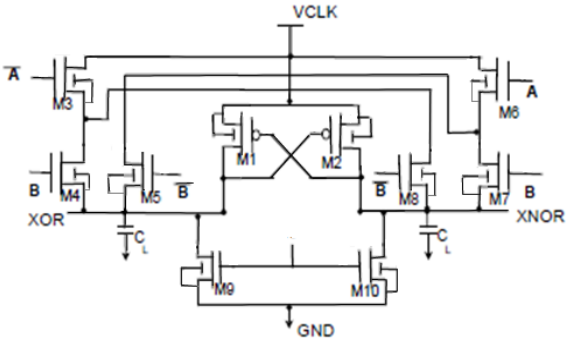

Fig. 20. Schematic of FinFET xor/xnor with Adiabatic Logic.

The transient analysis was performed, and the waveforms of the xor/xnor circuit were shown in Fig. 21 and Fig. 22.

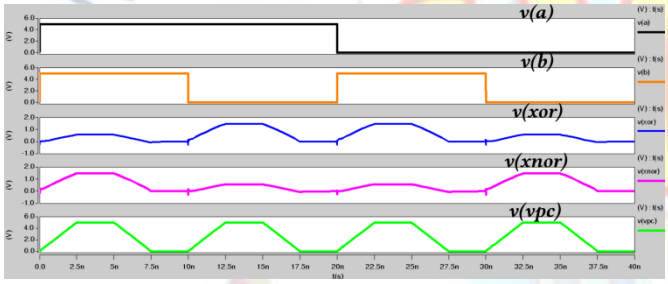

Fig. 21. Voltage waveforms of FinFET xor/xnor with Adiabatic Logic.

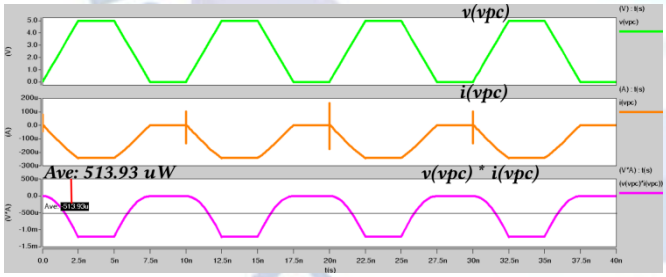

Fig. 22. Power waveform of FinFET xor/xnor with Adiabatic Logic.

The average power consumption of the circuit is computed to be 513.93uW.

Circuit	*Without Adiabatic*	*With Adiabatic*	*Power consumption Reduction*
Buffer	1506.2 uW	644.31 uW	57.22%
AND/NAND	1147.4 uW	489.14 uW	57.37%
XOR/XNOR	1208 uW	513.93 uW	57.46%

5. FUTURE SCOPE AND CONCLUSION

The project is aimed to design low power consuming circuits which can be used to reduce power utilization in the devices. In this paper, three circuits - buffer, and/nand, and xor/xnor circuits were designed using FinFETs. They were designed using FinFET 32nm technology. The average power of the three circuits was computed. For buffer, the average power consumption was found to be 1506.2uW without adiabatic logic and 644.31uW with adiabatic logic. The power reduction is 57.22%.For, and/nand the average power consumption was found to be 1147.4uW without adiabatic logic and 489.14uW with adiabatic logic. The power reduction is 57.37%. For xor/xnor, the average power consumption was found to be 1208uW without adiabatic logic and 513.93uW with adiabatic logic. The power reduction is 57.46%.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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