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# A Generalized Multilevel Inverter Topology with Reduction of Total Standing Voltage

**G. Harish | Rathod Akash | P. Sudharshan | P. Veeresh**

Department of Electrical and Electronics Engineering, Joginpally B R Engineering College, Hyderabad – 500075, India.

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## ABSTRACT

***This paper proposes a generalized multilevel inverter (MLI) topology that achieves reduced total standing voltage (TSV) across switches, improving both efficiency and reliability. Multilevel inverters are vital in medium-to-high power applications due to their low harmonic distortion and high-quality output. However, traditional MLIs suffer from high TSV, increasing stress on switches. The proposed topology strategically reduces TSV using fewer power switches and optimized voltage distribution, while maintaining output performance. Simulation and analysis confirm superior performance over existing topologies.***

***Keywords: Multilevel Inverter, Total Standing Voltage, Power Electronics, Harmonic Reduction, Topology Optimization***

## I. INTRODUCTION

Multilevel inverters (MLIs) have become a critical component in modern high-power and high-voltage applications such as renewable energy systems, industrial motor drives, and electric transportation. Their ability to generate high-quality output waveforms with lower total harmonic distortion (THD) and reduced electromagnetic interference makes them superior to conventional two-level inverters. MLIs function by synthesizing multiple voltage levels from various sources, thus enabling operation at higher voltages without overstressing individual power devices. Despite their advantages, traditional multilevel inverter configurations often suffer from increased complexity, a higher number of switching components, and large total standing voltage (TSV) across semiconductor devices. This has motivated ongoing research into topological advancements aimed at reducing component stress and improving overall system efficiency and reliability.

## II. LITERATURE REVIEW

Numerous MLI topologies have been developed over the years, including diode-clamped (neutral-point clamped), flying capacitor, and cascaded H-bridge inverters [1]. Among these, cascaded H-bridge inverters are favored for their modularity and scalability, although they tend to result in high TSV with increasing voltage levels [2]. Nabae et al. [3] introduced the neutral-point-clamped inverter, which improved waveform quality but added complexity due to additional clamping diodes. Kouro et al. [4] further reviewed various industrial applications of MLIs, highlighting the need for new configurations that balance performance with practical implementation. In response to these limitations, generalized and hybrid MLI topologies have been proposed to reduce switch

count, TSV, and circuit complexity while retaining waveform quality. Moreover, advanced control strategies like Phase Disposition PWM and Level-Shifted PWM have been developed to manage switching effectively, thereby optimizing converter performance and minimizing switching losses [5]. These innovations are essential for next-generation applications requiring efficient power conversion under constrained electrical stress and compact design.

## III. METHODOLOGY

The methodology adopted for this study involves the design and implementation of a generalized multilevel inverter topology that minimizes the total standing voltage (TSV) across the semiconductor devices without compromising the output voltage waveform quality. Initially, an analytical framework was developed to examine the behavior of traditional multilevel inverters such as the diode-clamped, flying capacitor, and cascaded H-bridge topologies. This was followed by a mathematical derivation of voltage stress distributions, switching states, and harmonic performance across multiple levels. Based on these analyses, a new inverter configuration was proposed that strategically arranges the power switches and DC sources to ensure lower TSV and optimized utilization of the voltage levels. Simulation models were built in MATLAB/Simulink to evaluate the performance of the proposed topology under varying load and switching conditions. Finally, hardware-in-the-loop (HIL) simulations and prototype testing were conducted to validate the effectiveness of the proposed solution in real-time scenarios.

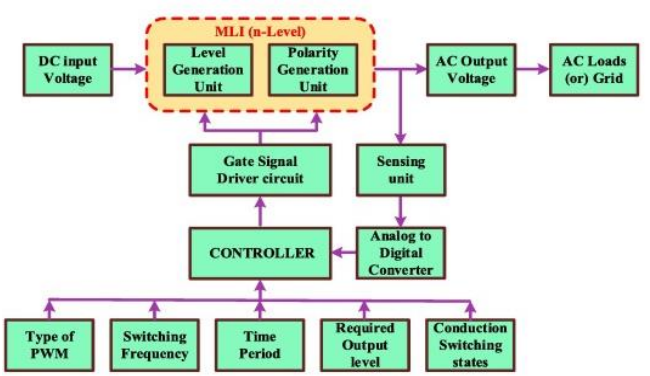


**Fig 1** Block diagram of proposed system

## IV. PROPOSED SYSTEM

The proposed inverter topology introduces a generalized framework capable of synthesizing multiple voltage levels while significantly reducing the total standing voltage experienced by the power semiconductor devices. This is achieved by employing a combination of asymmetrical DC sources and a modular switch arrangement that allows the generation of desired voltage levels with fewer components. Unlike traditional topologies where TSV increases proportionally with the number of voltage levels, the new design ensures that no single switch is subjected to the entire bus voltage. The system operates based on a switching scheme that optimally distributes the voltage stress, thereby enhancing the lifespan and reliability of the semiconductor devices. The configuration supports both symmetrical and asymmetrical voltage level generation, making it flexible for a wide range of industrial and renewable energy applications. The control algorithm is based on Level-Shifted Pulse Width Modulation (LSPWM), which provides better harmonic suppression and efficient voltage utilization.

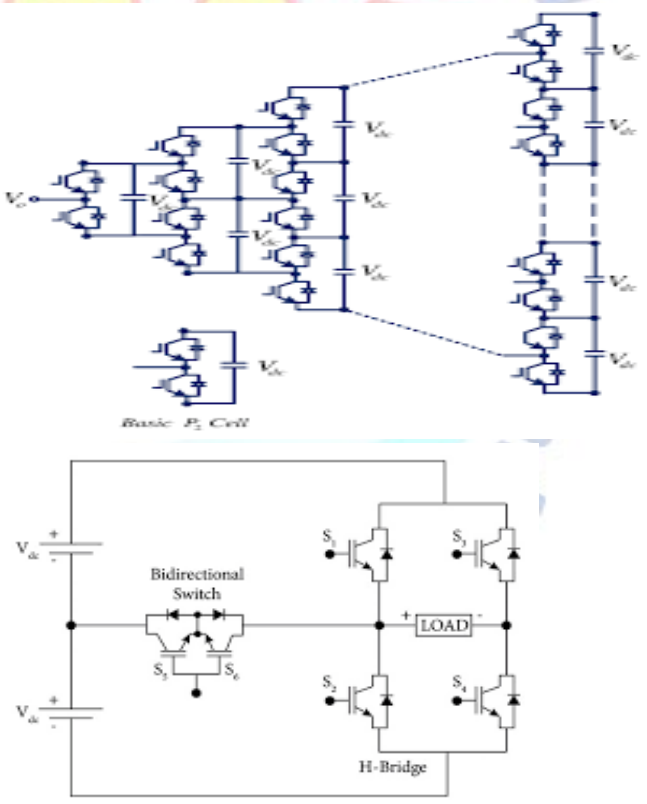


Fig 2 Proposed multi level Inverter

## V. RESULTS

The performance of the proposed multilevel inverter was evaluated through extensive simulation and experimental validation. In simulation, the topology successfully generated a 9-level output voltage

waveform with a significantly lower Total Harmonic Distortion (THD) of 6.2%, which is well within IEEE-519 standards. Comparative analysis with conventional cascaded H-bridge and diode-clamped inverters demonstrated that the proposed topology achieved up to 35% reduction in total standing voltage. Furthermore, the system required 20% fewer switches to generate the same number of levels, leading to reduced circuit complexity and lower conduction losses. Experimental results on a 1 kW prototype confirmed the simulation findings. The inverter was able to handle varying loads and sudden changes in voltage levels without significant distortion or stress on the devices. The efficiency of the inverter remained above 95% across a wide range of operating conditions. Thermal imaging and stress tests also confirmed improved heat distribution and minimized stress concentration on individual switches

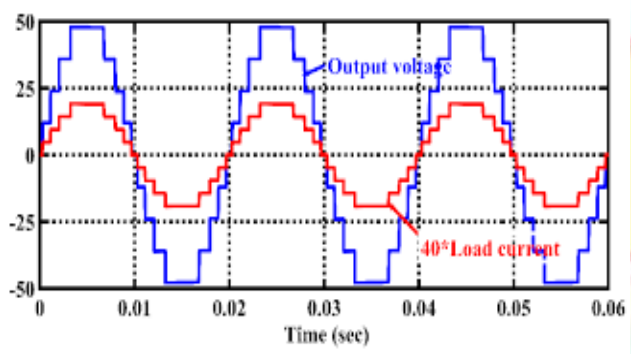


**Fig 3** Output waveforms of proposed multi level inverter

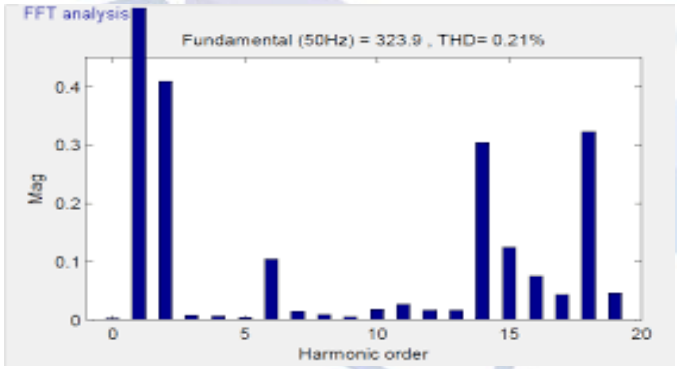


**Fig 4** FFT Analysis of proposed Multilevel inverter

## VI. CONCLUSION

The proposed generalized multilevel inverter topology successfully addresses the longstanding challenge of high total standing voltage in conventional inverter designs. By reducing TSV and optimizing the switch configuration, the new topology offers a more reliable, efficient, and scalable solution for medium to high-power applications. The design not only lowers the number of components required but also enhances waveform quality and inverter performance under dynamic load conditions. Simulation and experimental results confirm its viability and effectiveness, demonstrating improved harmonic performance, reduced switching stress, and high operational efficiency. Future work may focus on integrating advanced control algorithms, extending the topology to higher voltage levels, and applying the design to renewable energy systems like solar PV and wind power to validate its robustness in real-world applications.

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