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Non-Isolated High Step-Up DC-DC Converter with Minimum Switch Voltage Stress

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ABSTRACT

A new high step-up DC-DC converter topology combining a charge pump mechanism with a standard inductor- based Buck cell is here presented. Its main advantages are: minimum switch voltage stress, given by the input voltage, and reduced energy in the magnetic element compared to a conventional Boost converter designed for the same voltage gain. The proposed topology is derived through a modification of the basic voltage-doubler charge pump cell that, thanks to a coupled inductor, allows to make the flying capacitor voltages dependent on the switch duty-cycle. Both capacitor charging and discharging paths benefit from the inherent leakage inductance of the coupled inductor, with consequent soft diode turn off with no reverse recovery problems and ringing free operation. A proper design of the Buck inductance permits a quasi-square- wave operation, thus allowing a zero-voltage turn on of the switches. Suitable design criteria are proposed so as to achieve the desired converter operation mode, without need for any iterative process. Experimental results based on a 44V to 400V - 300W prototype confirm the theoretical analysis and expectations, showing a quite flat efficiency curve that stays above 90% down to one tenth of the nominal power.

KEYWORDS: *DC-DC converter 1, Boost converter 2, step-up DC-DC converter 3, switch voltage stress 4, step-up DC-DC converter*

1. INTRODUCTION

The usage of fossil fuels, such as oil, coal, and gas results in the serious environmental mental pollution, which have a great influence in the world. Meanwhile, there is a big contradiction between the fossil fuel supply and the global energy demand. Energy shortage and environmental pollution have been the major obstacles for human being development. How to find renewable energy sources is becoming urgent.Renewable sources are one of the significant players in the world's energy portfolio, and it will make one of the biggest contributions to electricity generation.Renewable energy systems generate low voltage output; thus, high step-up dc/dc converters are widely employed in many renewable energy applications, including fuel cells, wind power, and photovoltaic systems. Unfortunately, the output voltages of the renewable systems are relatively low. In order to satisfy the high bus voltage requirements for the full-bridge, half-bridge, or multilevel grid inverters , the sources has to be connected to series in order to bring out a grater voltage ratio , which again suffers from the voltage mismatches and the module level mismatch issues .

Large duty cycles result in high current stress in the boost switch. Theoretically, conventional step-up converters, such as the boost converter and flyback converter, cannot achieve a high step-up conversion with high efficiency because of the resistances of elements or leakage inductance Moreover to boost raise the voltage boost the converters would require a larger duty cycle . Large duty cycles result in high current stress in the boost switch.Renewable energy systems are been widely used to generate energy due to their clean generation .

Unfortunatley the renewable energy generations cannot offer a high voltage ratio compared to the grid.In order to connect the renewable generators to grid compatable , a high gain dc-dc converters are required .Implementing such dc-dc converters occupy high space and leads in higher cost.

2. CONVERTER TOPOLOGIES

A.Conventional Boost converter

In order to meet the grid requirements a converter with a high step up gain ratio and the high efficiency are more important. To achieve high voltage gains, classical boost and buck-boost converters require large switch duty ratios. Theoretically, conventional step-up converters, such as the boost converter and flyback converter, cannot achieve a high step-up conversion with high efficiency because of the resistances of elements or leakage inductance Moreover to boost raise the voltage boost the converters would require a larger duty cycle . A high step-up DC-DC converter topology combining a charge pump mechanism with a standard inductor based Buck cell is presented.

The proposed topology is derived through a modification of the basic voltage-doubler charge pump cell .A coupled inductor, is used to make the flying capacitor voltages dependent on the switch duty-cycle.Both capacitor charging and discharging paths benefit from the inherent leakage inductance of the coupled inductor, with consequent soft diode turn off with no reverse recovery problems and ringing free operation

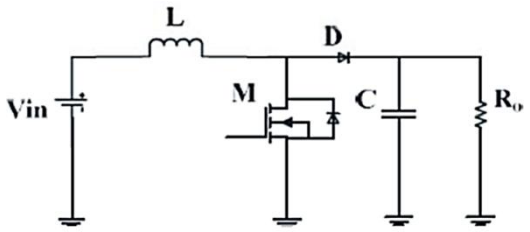

Fig 1. Classical boot converter.

The maximum voltage gain that can be achieved is constrained by the parasitic resistive components in the circuit and the efficiency is drastically reduced for large duty ratios. There are diode reverse recovery problems because the diode conducts for a short period of time. Also, larger ripples on the high input current and output voltage would further degrade the efficiency of the converter.

Typically high frequency transformers or coupled inductors are used to achieve high voltage conversion ratios, the transformer design becomes more complicated and the leakage inductances increase for achieving larger gains, as it requires higher number of winding turns. This leads to voltage spikes across the switches and voltage clamping techniques are required to

limit voltage stresses on the switches. Consequently, it makes the design more complicated.

Theoretically, conventional step-up converters, such as the boost converter and flyback converter, cannot achieve a high step-up conversion with high efficiency.

Because of the resistances of elements or leakage inductance, more over the conventional step-up converters with a single switch are unsuitable for high-power applications given an input large current ripple, which increases conduction losses.

The conventional step-up converters, are un suitable to achieve a high gain due to their resistances of elements or leakage inductance; also, the voltage stresses are large, these converters are unsuitable to operate at heavy load given a large input current ripple, which increases conduction losses.To achieve high voltage conversion ratios, a new family of high voltage gain dc-dc power electronic converters has been introduced.

A conventional interleaved boost converter for high step-up and high-power application is a suitable approach, by modifying the converter structure could make the converter which makes it suitable to operate

under the high gain conversion state.The conventional interleaved boost converter is an excellent candidate for high-power application and power factor correction.

Unfortunately, the step-up gain is limited, and the voltage stresses on semiconductor components are equal to output voltage. Hence, based on the aforementioned considerations, modifying a conventional interleaved boost converter for high step-up and high-power application is a suitable approach. A high step-up DC-DC converter topology combining a charge pump mechanism with a standard inductor based Buck cell is presented.

The proposed topology is derived through a modification of the basic voltage-doubler charge pump cell .A coupled inductor, is used to make the flying capacitor voltages dependent on the switch duty-cycle. Both capacitor charging and discharging paths benefit from the inherent leakage inductance of the coupled inductor, with consequent soft diode turn off with no reverse recovery problems and ringing free operation

B. Modified fly back converter

There has been a lot of modifications are being applied with the conventional converters to proposed for high gain converter design , in this numerous interleaved structures and some asymmetrical interleaved structures are found to be suitable for improving the voltage gain ratio Modifying a boost–fly back converter, shown in Fig.is one of the simple approaches to achieving high step-up gain; this gain is realized via a coupled inductor.The performance of the converter is similar to an active-clamped fly back converter; thus, the leakage energy is recovered to the output terminal. An interleaved boost converter with a voltage-lift capacitor is shown in the fig 1.3 which consists a voltage multipler module to lift the voltage level .

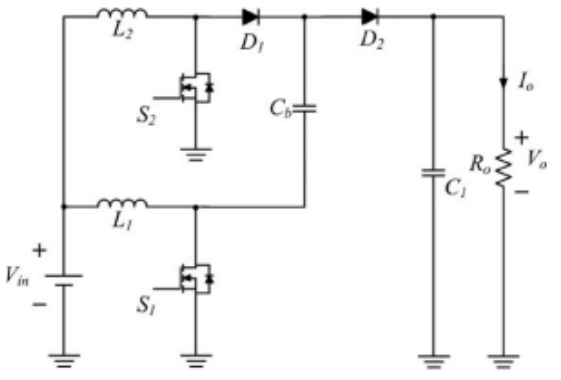

Fig 2 voltage lifting scheme with a modified

This approach is highly similar to the conventional interleaved type, with a additional voltage lifting scheme ,It obtains extra voltage gain through the voltage-lift capacitor, and reduces the input current ripple, which is suitable for power factor correction (PFC) and high-power applications.

Later an asymmetrical interleaved high step-up converter that combines the advantages of the aforementioned converters is proposed, which combined the advantages of both is presented which contains the both voltage lifting and step up gain with a minimum duty ratio control .

C.Interleaved converter with voltage multiplier module

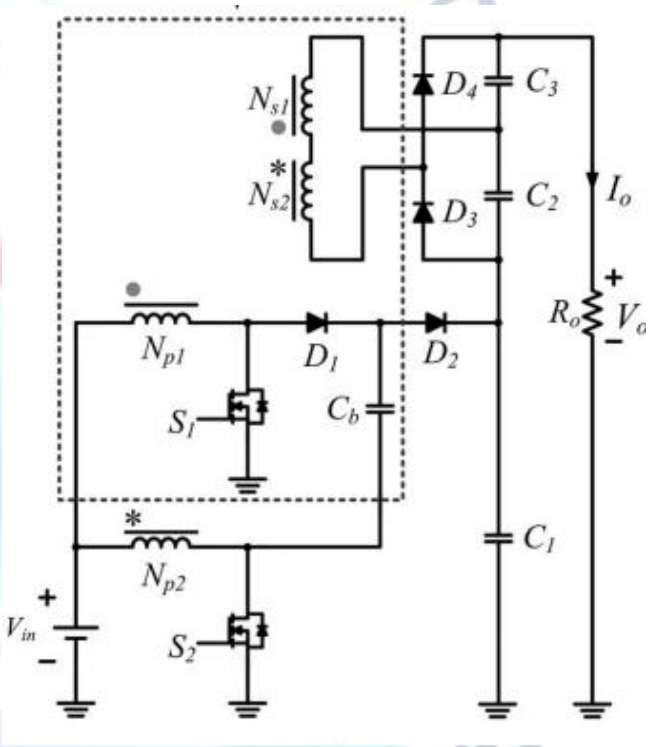

Fig 3 Interleaved boost converter with a high step-up conversion and a voltage multiplier module.

The high step-up interleaved converter with a voltage multiplier module is shown in Fig.3 . The voltage multiplier module is composed of two coupled inductors and two switched capacitors and is inserted between a conventional interleaved boost converter to form a modified boost–fly back–forward interleaved structure. When the switches turn off by turn, the phase whose switch is in OFF state performs as a fly back converter, and the other phase whose switch is in ON state performs as a forward converter.

Primary windings of the coupled inductors with Np turns are employed to decrease input current ripple, and secondary windings of the coupled inductors with

Ns turns are connected in series to extend voltage gain. The turn ratios of the coupled inductors are the same. converter operates in continuous conduction mode (CCM), and the duty cycles of the power switches during steady

Later a converter based on the conventional interleaved boost converter integrated with a voltage multiplier module, and the voltage multiplier module is composed of switched capacitors and coupled inductors. The coupled inductors can be designed to extend step-up gain, and the switched capacitors offer extra voltage conversion ratio. In addition, when one of the switches turns off, the energy stored in the magnetizing inductor will transfer via three respective paths; thus, the current distribution not only decreases the conduction losses by lower effective current but also makes currents through some diodes decrease to zero before they turn off, which alleviate diode reverse recovery losses .

D.High step up interleaving boost converter .

High step-up interleaved converter with a voltage multiplier module is shown in Fig. 1.5. The voltage multiplier module is composed of two coupled inductors and two switched capacitors and is inserted between a conventional interleaved boost converter to form a modified boost–fly back–forward interleaved structure

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A conventional interleaved boost converter for high step-up and high-power application is a suitable approach, by modifying the converter structure could make the converter which makes it suitable to operate under the high gain conversion state.The conventional interleaved boost converter is an excellent candidate for high-power application and power factor correction.

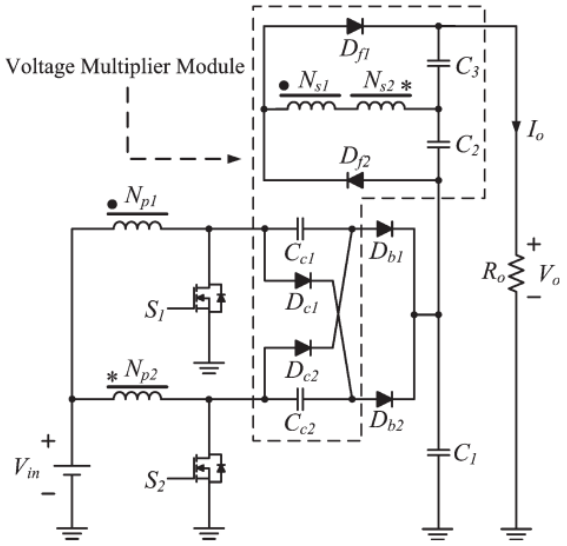

Fig 4 A modified interleaved high step up converter with a voltage multiplier module

3. TOPOLOGY DESIGN

The resonant capacitors Cr1and Cr2are not only used as a part of the resonant tank.the rectifier and connected to the negative potential of the output voltage V

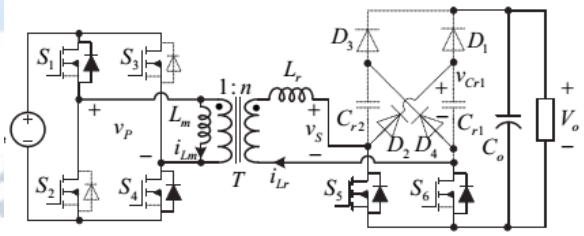

Fig.5 Topology Design

This design has a Cr1, Cr2 resonant capacitors, Lr a resonant inductor, D1and D3are output diodes, D2and D4are regenerative diodes, Tis a high frequency transformer.S1and S2are the active switches through which the output power can be regulated. The resonant

tank is composed of three elements, Cr1, Cr2and Lr .The converter can be operated either in buck or boost mode based on the input voltage .The inductor Lm is the magnetizing inductance of the transformer, and n is the secondary to primary turns ratio of the transformer T.

The resonant capacitors Cr1and Cr2are not only used as a part of the resonant tank, but also used to double the output voltage, which is similar to the voltage multiplier..Phase-shift control strategy is employed to regulate the output voltage and power.Full bridge resonant voltage multiplier with isolated dc –dc conversion is designed.In the circuit Cr1and Cr2are resonant capacitors, Lr is a resonant inductor.D1and D3are output diodes, D2 and D4 are regenerative diodes,. Tis a high frequency transformer for isolation.S1- S4 are the active switches through which the output power can be regulated.S5and S6are placed on the underside of the rectifier and connected to the negative potential of the output voltage Vo.

4. METHODOLOGY OF PROPOSED SYSTEM

A. Influence Of Non-Ideal Back-Emf On Commutation Point Detection And Optimal Commutation Control

The influence of non-ideal back-EMF on the detection of sensorless commutation point is firstly analyzed. Then, the electromagnetic torque fluctuation and efficiency of the motor commutated at different commutation points driven by square current are compared, and the optimal commutation control method is proposed. In addition, for the low inductor motor with non-ideal back-EMF and buck converter front-end drive structure, an integrated nonlinear model of motor and drive circuit including precise back-EMF parameters is established. Based on the nonlinear model, the feasibility of model linearization is analyzed. The linearization method based on input-output feedback method is proposed, and a steady speed controller based on linearization model is designed. Figure 4.1 shows the ideal and non-ideal back EMF

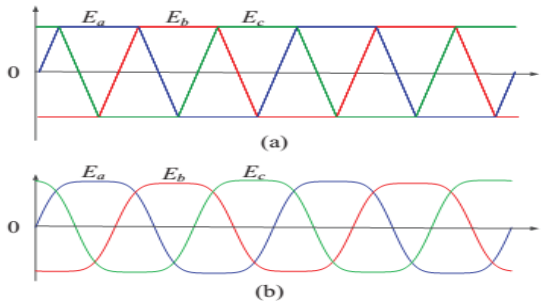

Fig 6 Back-EMF of BLDCM. (a) Ideal trapezoidal back-EMF. (b) nonideal actual back-EMF.

B. *Deviated commutation points detected by virtual neutral points method due to non-ideal back-EMF*

In the virtual neutral point-based position sensor-less ZCP detection method, when the neutral point voltage is un-measurable, three Y-type connected resistor network are used to provide a virtual neutral voltage signal as shown in Fig.6. Where, g denotes ground, n denotes the neutral point of the three-phase windings, and s denotes the virtual neutral point

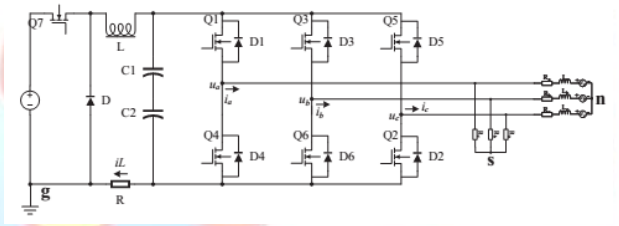

Fig 6 Schematic diagram of zero-crossing detection method based on virtual neutral point

The terminal voltage mathematic model of the BLDC motor is written as (4.1).

$$U_{xg} = L_x \frac{di_x}{dt} + R_x i_x + E_x + U_{ng} \quad (1)$$

where *Uxy* represents the voltage difference between *x* and *y* , *Lx*, *Rx*, *ix*, *Ex* represent the inductance, resistance, phase current and back-EMF of phase *x*, respectively. Here, the three-phase resistance and inductance are treated as constant and equal. The harmonic form expression of the three-phase non-ideal back-EMF of the BLDCM is as (2)

$$\begin{cases} E_a = \omega_e k_e e_a(\theta_e) \\ E_b = \omega_e k_e e_b(\theta_e) \\ E_c = \omega_e k_e e_c(\theta_e) \end{cases} \quad \text{.....(2)}$$

Where

$$\begin{cases} e_a(\theta_e) = \sum_{m=1}^{\infty} A_{am} \sin(m(\theta_e)) + D_a \\ e_b(\theta_e) = \sum_{m=1}^{\infty} A_{bm} \sin\left(m\left(\theta_e - \frac{2\pi}{3}\right)\right) + D_b \\ e_c(\theta_e) = \sum_{m=1}^{\infty} A_{cm} \sin\left(m\left(\theta_e + \frac{2\pi}{3}\right)\right) + D_c \end{cases}$$

ωe represents the electromagnetic speed, ke represents the back-EMF coefficient, θe represents the electrical angle position, Axm represents the mth harmonic coefficient of the x phase back-EMF, Dx represents the DC offset of the x phase back-EMF, and ex represents the x phase back-EMF waveform shape function. The corresponding coefficients can be obtained by offline measurement. According to Kirchhoff's law, the terminal voltage can also be expressed as (3).

$$U_{xg} = U_{xs} + U_{sg} \quad \text{.....(3)}$$

The following constraint equations can be obtained according to the Y-type connection

$$U_{sg} = \frac{1}{3}(U_{ag} + U_{bg} + U_{cg}) \quad \text{.....(4)}$$

$$U_{ng} = \frac{1}{3}(U_{ag} + U_{bg} + U_{cg} - E_a - E_b - E_c) \quad \text{.....(5)}$$

The sensorless ZCP detection method based on the virtual neutral point compares the terminal voltage with the virtual neutral point voltage to obtain ZCPs of the non-conducting phase back-EMF. Taking the phase A as an example, when phase A is the non-conductive, the detected voltage difference in virtual neutral point based method can be obtained as (4.6).

$$U_{as} = U_{ag} - U_{sg} = \frac{1}{3}(2E_a - E_b - E_c) \quad \text{..(6)}$$

Similarly, phase B and C are as (7), respectively.

$$\begin{aligned} U_{bs} &= U_{bg} - U_{sg} = \tfrac{1}{3}(2E_b - E_c - E_a) \\ U_{cs} &= U_{cg} - U_{sg} = \tfrac{1}{3}(2E_c - E_a - E_b) \end{aligned} \quad \text{.....(7)}$$

By taking (2) into (6) and (7) and ignoring the third and above harmoniccomponents that have less influence on the ZCPs detection, detailed actual detected voltage can be expressed as the equations at the bottom of the page. It is well known that odd harmonics are the main components in trapezoidal wave signals, while second or other even harmonics are very few. So, after neglecting three or more harmonics, only the fundamental and DC components are left when calculating the influence of actual measured voltage on ZCP. Thus, the actual detected ZCPs can be obtained by making them equal zero. Moreover, the theoretically ideal commutation point should be the intersection of two adjacent back-EMFs, that is, the points where $Ea = Eb$, $Eb = Ec$, $Ec = Ea$. By comparing the phase relationship between the detected ZCPs and the ideal commutation points, the phase angle of the detected ZCPs deviating from the ideal ZCPs $\phi z1{-}6$ can be obtained.

C. *Comparison of different commutation points on instantaneous torque*

Considering the extremely low inductance value, the inconsistent current change rate during the commutation process caused by the inductance can be ignored. Thus, under the square current drive mode, only two phases are turned on at any time. Then, the instantaneous torque Te of the motor can be expressed as (8)

$$\begin{aligned} T_e &= \frac{E_x i_x + E_y i_y}{\omega_m} = p\frac{E_x i_x + E_y i_y}{\omega_e} \\ &= pk_e(e_x i_x + e_y i_y) = pk_e e_{xy}(\theta_e)\, i_m \end{aligned} \quad \text{.....(8)}$$

where, $\omega m$is the mechanical speed, p is the pole pairs, exy (θe) is the back-EMF difference shape function of phase x and y at position θe, and im is the DC-link current.

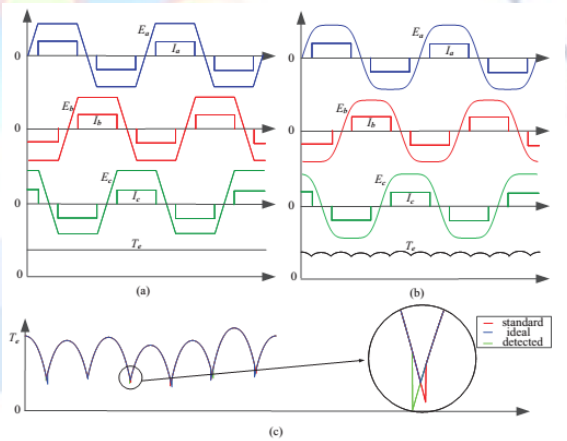

Fig 7 Currents and torque waveform of BLDCM driven by square wave current. (a) ideal back-EMF. (b) non-ideal back-EMF. (c) torque waveforms commutated by different commutation points

Ignoring the commutation process, AB interval is defined as the phase A and B conduction interval, where current flowing from phase A to phase B. Similarly, each cycle can be divided into six intervals, namely AB, AC, BC, BA, CA and CB. The back-EMF difference shape function exy (θe) at different intervals

are listed in Table 4.1. For current closed-loop control, it can be seen that the backEMF models in each interval are different and nonlinear in Fig. 7, which makes it difficult to control the current waveform in the traditional square wave current drive mode. Fig.7(c) shows the instantaneous torque waveforms of the motor commutated according to commutation points by different methods. Obviously, standard and detected commutation points will increase the fluctuation of instantaneous torque near commutation points under non-ideal back-EMF BLDCM. Although these fluctuations are not enough to cause huge speed fluctuations for large inertia motors, they will also affect the current waveform and influence steady speed accuracy.

D. *Optimal commutation control*

From the above analysis, it can be concluded that among the three commutation points, the motor commutated according to the ideal commutation point has the lowest torque fluctuation and the highest average torque and efficiency. In addition, besides the influence of non-ideal back EMF on the phase deviation of ZCP detection method, the phase delay introduced by LPF in various signal processing circuits is the main part of commutation deviation. LPF cut-off frequency used to eliminate noise interference to avoid false detection is very low, so a large phase delay is introduced. Based on the analysis of commutation deviation, this paper presents a new optimal commutation method. The optimal commutation method is an improved commutation compensation method, which considers low-pass filter delay and non-ideal back-EMF factors.

The proposed optimal commutation method consists of the following steps: 1) Estimate LPF delay phase: The LPF is generally approximated to a first-order inertia unit as $LPF(s) = s+ \omega\omega\ c\ c$, ωc is the cutoff frequency speed, then LPF delay phase ϕLPF can be estimated according to the phase characteristics ϕLPF = −arctan($\omega e/\omega c$). 2) Calculate deviation phase $\phi z1–6$: firstly, obtain the actual back-EMF waveforms by offline measurement at constant speed and normalize back-EMF waveform function.

Then, a 1- 2-9-1 structure 4 layers feed-forward back propagation neural network is used for fitting the accurate back-EMF waveform function. The back-EMF harmonic coefficients can be obtained through performing Fourier decomposition for the fitted back EMF function.

5. SIMULINK MODEL

Figure 8 show the resonant based high gain converter with half bridge rectifier in the front end followed by high frequency transformer with the resonant cell and voltage doubler circuit at the end

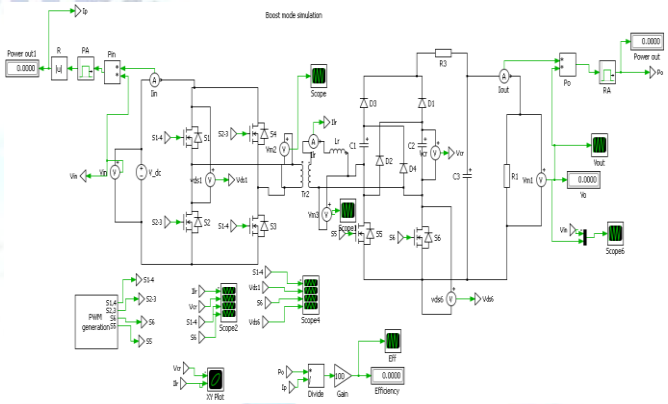

Fig 8: Simulink model of Resonance based High gain converter-

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Figure 8 shows the boost mode Input and output voltages and PWM signal of the switches in the front full bridge rectifier and back end voltage multiplier circuit.

The steady state waveforms of the resonant inductor, resonant capacitor and driving voltages of S1and S6 in the boost mode. It can be seen that the driving signal of S1, vGS1, lags the driving signal of S6, vGS6, which means $d_{\varphi P}<1$ and the converter operates in the boost mode.

The primary side switches S1 & S4 operates with a duty of 50% whereas S2 & S3 operates with phase shift control of 1μs with 30% duty. The secondary side switches operates with 45% duty.

The soft switching patterns for the primary side S1 and secondary side switch S6 which operates with the static zero voltage switching pattern , makes the primary conversion more efficient , after the secondary becomes zero.

6. SIMULATION RESULT

This paper presented a high step-up topology featuring minimum switch voltage stress as well as reduced magnetic energy, compared with an equivalent

gain conventional Boost converter. The conversion process explores both a magnetic coupling and a charge pump mechanism to efficiently transfer The conversion efficiency (power stage only) was calculated measuring input and output powers using digital multimeters (Keysight 34461A), for input/output voltages and output cur- rent, while the input current was read directly on the DC power supply Chroma 62050P-100-100. The overall relative error on the efficiency calculation is lower than 0.5%, the main contribution coming from the input current measurement (0.1% of reading plus 0.1% of range). The measured efficiency at different input voltage values and for two different power constant levels is shown in values above 95% are achieved at nominal power except at the lower part of the input voltage range (Vg = 42V). Here, the slight efficiency reduction is caused by the different operating condition mentioned above according to which Tr1/2 > (1 − Dmax)Ts, that is causing an increase of S1 turn-on losses, as revealed by the vDS2(t) waveform in Fig. 7a. At lower output current values, the efficiency remains above 90% down approximately to one tenth of the nominal power, as revealed by the measurement reported in Fig. 13 for two different input voltage values (Vg = 44V and Vg = 48V).

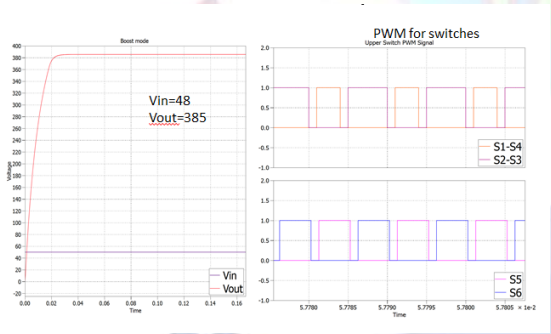

Fig 9 : Boost mode output

The relative losses distribution between the different components was calculated based on the stress analysis reported in Section IV at the nominal operating point, and the result is shown in Fig. 14. The total power loss was estimated as PEstimated Loss = 10W, lower than the measured one PMeasured Loss = 15.8W. As we can see, turn-off switching losses have been considered too, even if the commutation time intervals are very difficult to predict.

This is because the switching node transition is affected by the huge MOSFET's output capacitance (roughly 3.4nF each), that acts as a loss- less snubber, especially at the S2 turn off, where the switched current is quite low (≈ −2.5A from Fig. 8). However, the forecasted total S1 losses of 1.37W are not unrealistic, since the temperature measured on the device package in the same operating point was 83◦C without forced air circulation (ambient temperature TA ≈ 20◦C). With a thermal resistance from junction to ambient of the TO263-7 package ranging between 40K/W with 6cm2 of cooling area and 62K/W with minimal footprint, it means a dissipated power in the range 1÷1.6W. Turn-on switching losses have been neglected for both switches, thanks to the quasi-square-wave operation imposed by a proper selection of the magnetizing inductance Lb, even if this condition is not completely met for S1, as can be inferred from the rising edge of voltage vDS2(t) in Fig. 7b. However, the small switched current and residual voltage (≈ 10V), give a negligible contribution to the overall losses. The core loss was estimated based on the manufacturer data of the used N87 ferrite material.

7. Conclusion

The high RMS current value flowing in the devices, which is the price to pay for having the minimum switch voltage stress, makes the control of any parasitic resistance in the current path crucial in order to limit the conduction losses. This is the reason why the input and the buck stage capacitances were implemented by connecting in parallel more lower value capacitors, as revealed in table II. For the same reasons, the SiC diodes used in the experimental prototype are not the best choice for this circuit, where they are naturally turned off by the resonant current id. Looking at their voltage stress (see table III), lower voltage rating and, consequently, lower voltage drop Si devices could be used for a better overall efficiency.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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