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A Survey on Fault Tolerant Capability against Open Circuit Faults in Multilevel Inverter

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ABSTRACT

With the increase in the number of power electronic components, Multilevel Inverter offers better output quality, less stress on the semiconductor switches, decreased total harmonic distortion etc. However, low reliability of the power electronic components poses a serious threat for proper functioning of the inverter. Thus, increasing the reliability of the inverter with reduced device count has become an important research aspect. Owing to the above statements, a five-level inverter topology is made fault tolerant by the addition of a redundant leg. This architecture has lesser switches and is able to operate satisfactorily under both types of fault i.e. open and short circuit failure. For any five-level inverter topology, the presented redundant leg architecture can achieve satisfactory output waveforms under faulty conditions. The verification of the presented topology is evaluated by the obtained experimental results.

I.INTRODUCTION

Renewable energy sources, which are naturally replenished, are gaining widespread attention in both research and industrial sectors owing to the fast depletion of the conventional energy resources such as fossil fuels [1]. Continuous development in the semiconductor industry has led to the increased efficiency and high output capability of the solar energy [2]. The maximum power from photo voltaic (PVs) is extracted through the optimization techniques [3]. A two-stage process, DC-DC converter boosting the low array voltage is followed by the inversion stage. In order to reduce the losses, the conventional inverters are being replaced by Multilevel Inverters (MLI). MLI topologies result in better output voltage quality owing to increased number of levels in the output voltage waveform. This inadvertently leads to reduction in the harmonic content as well [4], [5]. The advantages offered by the MLI are in direct proportion with the number of output levels which is in direct proportion to the number of power switching devices utilized. Therefore, MLI with reduced device count has attracted a lot of attention from the research industry [6], [7]. As confirmed in [8], semiconductor switches have the maximum probability to develop failure when compared with the rest of the power electronic components. It is because of this reason that for such MLI topologies which have less component count might not function as required when the fault is developed on its switches. Therefore, the research community has now focused on adding fault tolerance characteristics to such MLI topologies which have lesser component count.

In the recent years, many topologies have been proposed on the fault tolerance characteristics of the MLI topology [9], [10], [11], [12], [13]. In [14], a high number of power devices are required to incorporate fault tolerant characteristics which are its biggest demerit. Also, at times of fault on the outermost switches, rated power cannot be delivered. Along with that, the topology has a very low Level to Switch Ratio (LSR) and fails to deliver during multiple switch failure. In [15], the topology cannot sustain multiple switch failure. The redundant leg is composed of switches of different voltage ratings. Implementation of three bidirectional switches along with a low LSR value makes the topology less attractive. Reference [16] has proposed a fault tolerant topology. The main drawbacks in [16] are that the inner leg switches of the Neutral Point Clamped (NPC) leg are not fault tolerant. In order to maintain the output voltage at rated value, center-tap transformer is used which increases the cost of the system. Also, it cannot sustain multiple switch failure. In [17], the topology proposed is modular and achieves single switch fault tolerance by utilizing a cross connected architecture comprising of TRIACs. But the proposed topology fails to deliver the output at times of multiple switch failure. Also, the topology has a very low LSR. Though the solution proposed in [18] claims tolerance to multiple switch failure, it fails to operate when fault occurs on switches from different NPC legs. Owing to the above discussed shortcomings, this paper has focused on presenting a new MLI topology which is capable of delivering satisfactory post-fault characteristics. This architecture has reduced device count and tolerance capabilities. The presented architecture can tolerate all kinds of faults i.e. faults occurring in open switch mode and short switch mode. For any five-level inverter topology, the proposed redundant leg architecture can deliver rated output conditions under faulty conditions. The verification of the presented topology is evaluated by the obtained experimental results.

1. Healthy Operation of Proposed Topology

This section proposes a novel fault tolerant architecture which is able to tolerate fault in hybrid five-level inverter topology. Figure 1 represents the schematic diagram of the proposed topology.

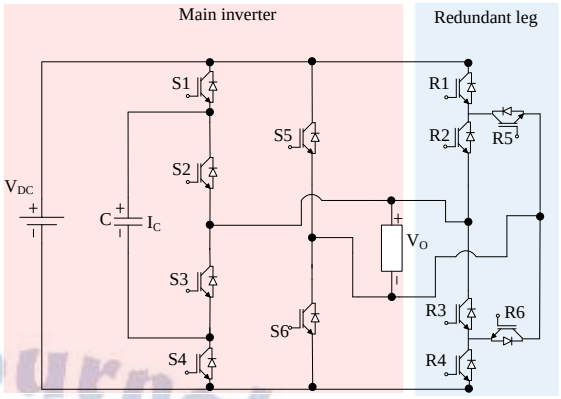


Fig 1: Proposed Fault Tolerant Multilevel Inverter

"Main inverter" and "Redundant leg" architectures are the two main parts of the presented MLI topology which is capable of tolerating faults owing to the hardware addition to the five-level main inverter topology. Under the main inverter topology, it comprises of conventional flying capacitor leg capable of generating three level voltage waveform on its own, whereas the second leg in the architecture comprises of the conventional cascaded H-bridge leg. For the addition of fault tolerance characteristics, a novel hardware based redundant leg is presented in this paper. The proposed architecture comprises of a combination of six switches which are attached in a way which corresponds to the conventional active neutral point clamped (ANPC) leg architecture. For the healthy conditions, a five-level waveform of load voltage is obtained when measured.

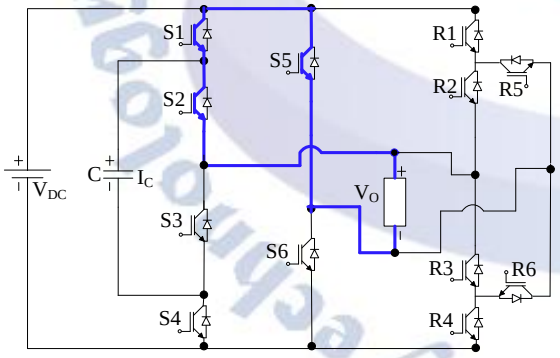
TABLE 1: Main inverter switching scheme representation

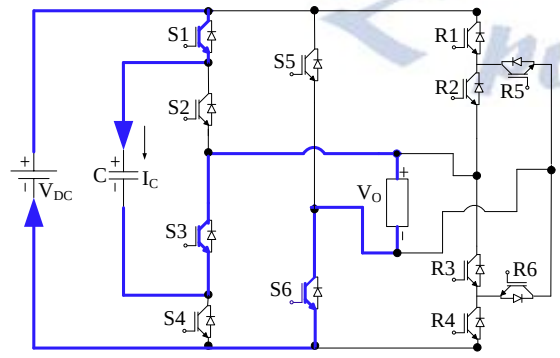
Voltage index	Output voltage	Switching State	State of capacitor voltage
V1	Vs	S1,S2,S6	-
V2	Cv	S2,S4,S6	D
	(Vs-Cv)	S1,S3,S6	C
V3	0	S1,S2,S5	-
		S3,S4,S6	
V4	-Cv	S1,S3,S5	D
	-(Vs-Cv)	S2,S4,S5	C
V5	-Vs	S3,S4,S5	-
C= Charging of the capacitor D= Discharging of the capacitor			

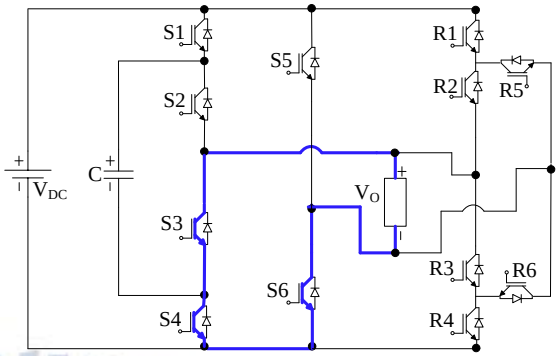
Table I depicts the main inverter switching paths incorporated in the proposed MLI topology. Also, Table I describes about the effect on capacitor voltage. As can be observed from Table I, 'V2' and 'V4' voltage levels have inherent redundant paths. These paths have inverse effect on the capacitor voltage. This inherent characteristic of the main inverter topology results in self-voltage balancing of the capacitor. Figure 2 represents the current path through different switching paths under both directions of load current.

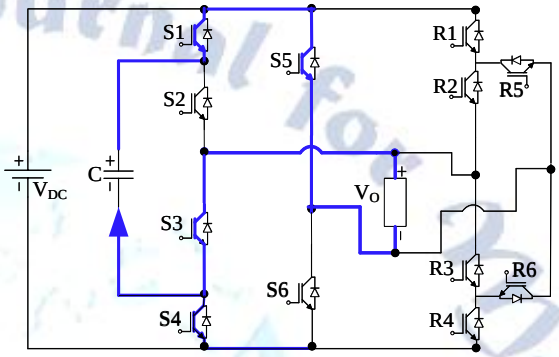
II. FAULT CLASSIFICATION ANALYSIS

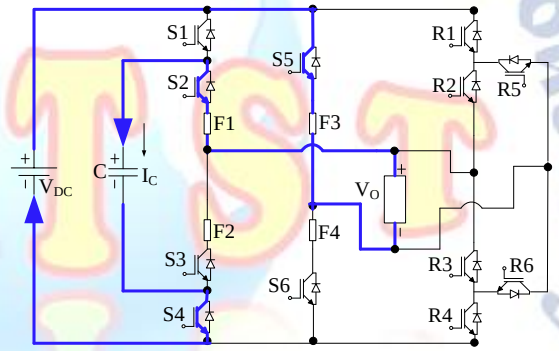
Since the main inverter topology incorporated in the presented fault tolerant topology is made up of conventional FC and CHB legs, the fault study is carried out on the individual switches of those two legs. Both single and multiple switch fault scenarios can be handled by the proposed topology. Owing to the redundant leg addition to the main inverter topology, the proposed topology is able to generate the five-level output voltage waveform. In order to achieve the operation under short circuit failure, fast acting fuses are added across all four terminals connected across the load which belongs to the main inverter topology. The blowing of the fuses under heavy current results in the formation of open circuit failure as the short circuit failure is removed, and the same can be handled in the same way as an open circuit failure.

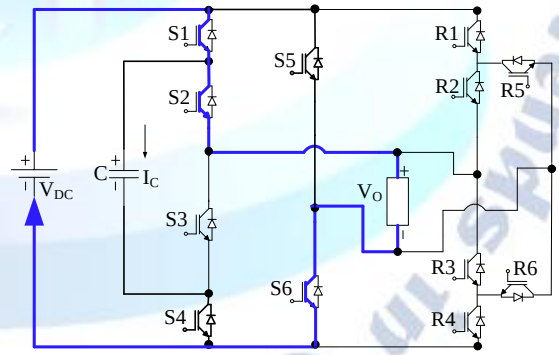


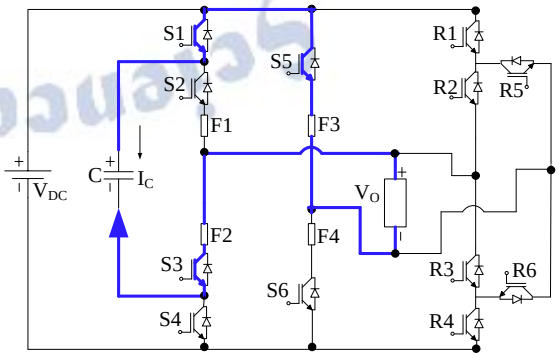












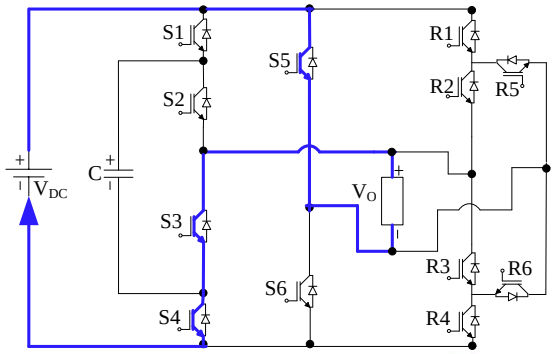


Fig 2: Current representation corresponding to switching states as mentioned in Table 1

Faulty consideration on Single Switch

TABLE 2: Individual voltage level availability post single switch fault consideration

Faulty device	Output voltage level status				
	V1	V2	V3	V4	V5
S1	0	1	1	1	1
S2	0	1	1	1	1
S3	1	1	1	0	0
S4	1	1	1	1	0
S5	1	1	1	0	0
S6	0	0	1	1	1
"0", "1"= Inability/Ability to generate the corresponding voltage level					

When the fault is considered on single switch, the designed ANPC redundant leg enables for achieving the post-fault characteristics equivalent to pre-fault one. The generation of middle voltage levels is achieved by activating the available path from the redundant paths corresponding to V2 and V4. The only thing to be kept in mind is that the self-voltage balancing of the capacitor has to be achieved at the end of each fundamental cycle. Thus, it can be said that the flying capacitor would achieve self-voltage balancing without getting effected. The proposed topology is able to achieve the pre-fault characteristics under faulty conditions.

Power Loss Evaluation

In order to evaluate the efficiency of the MLI, power losses have to be evaluated. With the increased magnitude of power losses, the junction temperate of the semiconductor devices will increase which might result in the thermal runaway of the devices. In general, there are three operating modes under which semiconductor switch operates:

1. Blocking mode
2. Conduction mode
3. Switching mode

When operating under the blocking mode, high magnitude of voltage is impressed upon the semiconductor terminals. However, under this mode, a very small magnitude of losses occurs. It is due to this that the blocking mode is not considered while evaluating the losses. In the conduction mode, the semiconductor switch is in ON state. The losses under this mode are evaluated by the magnitude of current flowing through switches as well as the anti-parallel diode. The magnitude of losses is being controlled by two major factors which are the internal resistance of the switch and the diode, and the forward voltage drop. When finding out the losses pertaining to switching losses, the instantaneous current through the switch during the transition and the switching frequency determines the switching losses.

III. CONDUCTION LOSS EVALUATION

The conduction losses of the semiconductor switches are evaluated for the 'ON' state. Since the semiconductor switch would conduct current under both directions of load current i.e. through the switch and through the anti-parallel diode, the losses would have to be evaluated for both switch and the diode. In order to evaluate the conduction losses for the entire topology, individual loss corresponding to each switch is evaluated and summed up. One thing to note is that the conduction losses only depend on the duration of the activation of semiconductor switch, and not on the switching frequency. The equation for evaluating the conduction losses is given as follows:

$$P_{cond.[IGBT]} = V_{F.V.D.} \times I_{average,[DS]} + r_{DS,[ON]} \times I^{2}_{R.M.S.,[DS]} \quad (1)$$

$V_{F.V.D.}$: Voltage drop of the switch under forward condition

$I_{average,[DS]}$: The magnitude of average value of current through drain to source

$r_{DS,[ON]}$: Drain to source 'ON' state resistance

$I_{RMS,[DS]}$: Drain to source RMS current under the 'ON' state

In a similar way, the anti-parallel diode also contributes to the conduction losses. The power losses due to the anti-parallel diode can be evaluated by multiplying the 'ON' state voltage drop and the average magnitude of current, also by multiplying the 'ON' state resistance value with the RMS value of current. The equation governing the conduction losses for the anti-parallel diode is given as follows:

$$P_{cond.[Diode]} = V_{D.} \times I_{Diode,[average]} + r_{Diode,[ON]} \times I^{2}_{R.M.S.,[Diode]} \quad (2)$$

V_D : Forward voltage drop of the diode

$I_{Diode,[average]}$: Average value of diode current

$r_{Diode,[ON]}$: Diode resistance under the 'ON' state

$I_{R.M.S.[Diode]}$: RMS value of the current through the diode

For any semiconductor based topology, the conduction losses are in direct proportion to the number of conducting switches i.e. the number of devices in the 'ON' state. Therefore, if an attempt is to be made to decrease the conduction losses, number of semiconductor switches conducting at any given instance should be reduced. For the presented topology, only three devices are turned on at any given instance which is one less when considering the conventional MLI topologies (5 level CHB, NPC and FC topologies). Also, under the faulty conditions, it is ensured that minimum numbers of switches are 'ON' at any given instance.

Switching Loss Evaluation

Apart from the conduction losses, the other major share of losses in any power electronics topology is being contributed by the switching losses. These types of losses occur when the transition is being made from on to off state and vice versa. In regards to this, the switching losses are in direct proportion to the switching frequency. When the switch changes its state from on to off or vice versa, both current and voltage magnitude are non-zero, which lead to the power losses. Under the 'ON' state, the forward voltage drop across the semiconductor switch reduces whereas the magnitude of current i.e. collector current increases. For the time taken by the switch to reduce the value of forward voltage drop to zero, losses would be encountered. The vice versa situation occurs when the switch makes the transition from on to off state. One thing to be noted is that during the estimation of power switching losses, both voltage and current waveforms are treated to be in the linear approximation range. Equation 3 and 4 represents the switching loss of the jth switch for both on and off state respectively.

$$E_{ON} = \int_{0}^{t_{on}} V(t) \times i(t) dt$$

$$= \int_{0}^{t_{on}} \left[\left(\frac{V_{bv,j}}{t_{on}} \times t \right) \left(\frac{-I}{t_{on}} \times (t - t_{on}) \right) \right] dt$$

$$= \frac{1}{6} \times V_{bv,j} \times I \times t_{on}$$

$$P_{Loss(swt\_on),j} = \frac{1}{6} \times V_{bv,j} \times I \times t_{on} \times f_{sw} \quad (3)$$

$V_{bv,j}$: Blocking voltage of j^{th} switch,

I: Magnitude of current under on state

t_{on} : Time interval under switch 'ON' transition

f_{sw} : Switching frequency.

In a similar way, the power losses under the transition of switch from on to off state is evaluated as given in the following equation:

$$P_{Loss(swt\_off),j} = \frac{1}{6} \times V_{bv,j} \times I^{o} \times t_{off} \times f_{sw} \quad (4)$$

$V_{bv,j}$: Magnitude of the blocking voltage of the j^{th} switch,

I^0 : Instantaneous value of current under the off state

t_{off} : Time period during the off state

Adding equation 3 and 4 gives the following equation:

$$P_{Total(swt\_loss)} = \frac{1}{6} \times (V_{bv,j}) \times f_{sw} \times (t_{on} + t_{off}) \times (I + I^{o}) \quad (5)$$

It can be observed from equation 5 that the total power losses primarily depend on two factors only, these are the switching frequency and the voltage blocking.

$$P_{Total(swt\_loss)} \alpha (V_{bv,j}) \quad (6)$$

$$P_{Total(swt\_loss)} \alpha (f_{sw}) \quad (7)$$

For the presented topology, the switches corresponding to the CHB leg have a voltage blocking requirement of Vdc, whereas the switches corresponding to the FC leg have a voltage blocking requirement of Vdc/2 only. In a similar way, the blocking voltage requirement can be evaluated for ANPC leg and it has been found out that four out of six switches have a blocking voltage requirement of Vdc/2 only whereas the rest of the two switches have a voltage requirement of Vdc.

IV. RESULTS OF PROPOSED FIVE LEVEL INVERTER TOPOLOGY

The simulation results proposed topology are obtained in MATLAB/SIMULINK for healthy as well as all faulty cases studied previously. The OPAL-RT results are taken for verification of simulation results of this fault tolerant top ology and are shown in the sections given below.

Simulation and Real Time Validation

The simulation results are obtained in MATLAB/Simulink for an R-L load with R=20Ω and L= 30 mH. The topology is operated with DC voltage source having magnitude, Vs= 50V. Sinusoidal pulse width modulation (SPWM) strategy is being implemented for the generation of gating signals, having modulation frequency equal to 50Hz whereas the carrier frequency is set at 1 kHz. The output voltage, output current and capacitor voltage during healthy as well as single and various above-mentioned faulty case are shown below. The experimental results are also carried out for same ratings except an input voltage source value Vs= 100 V and carrier frequency of 2000 Hz.

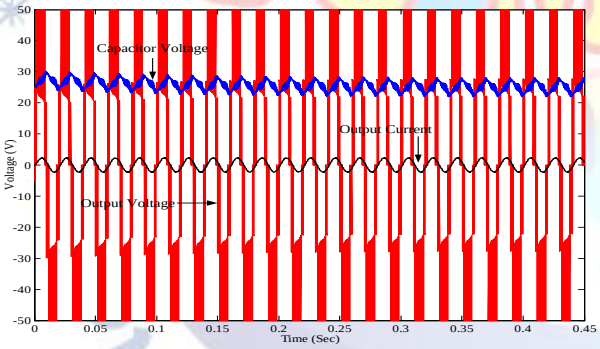


Fig 4 Simulation Results for main inverter topology under Healthy Condition

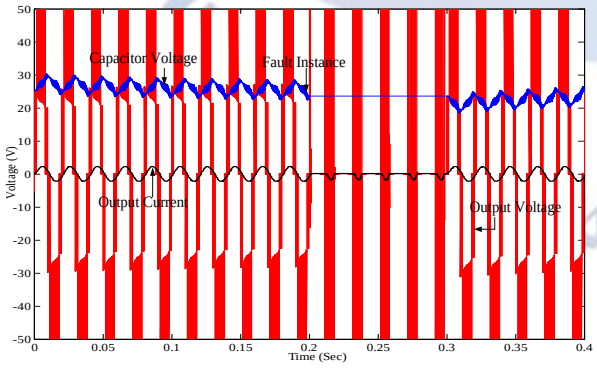


Fig 5 Simulation Result under single switch fault condition

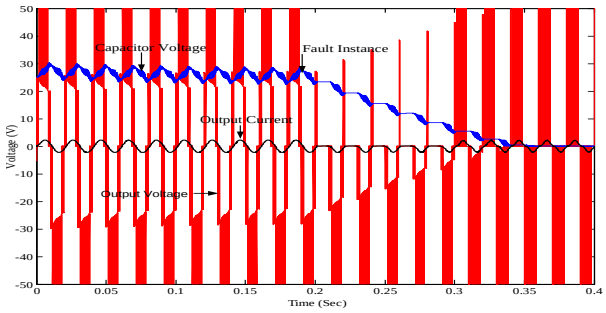


Fig 6 Simulation Result under multiple switch failure on FC leg

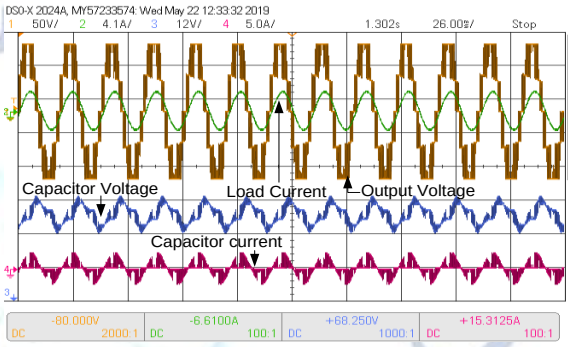


Fig 7 OPAL-RT Result for the Proposed Topology under no fault scenario.

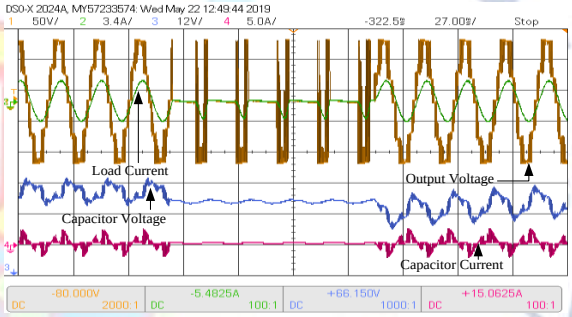


Fig 8 Output Waveforms under single switch fault condition on the proposed inverter.

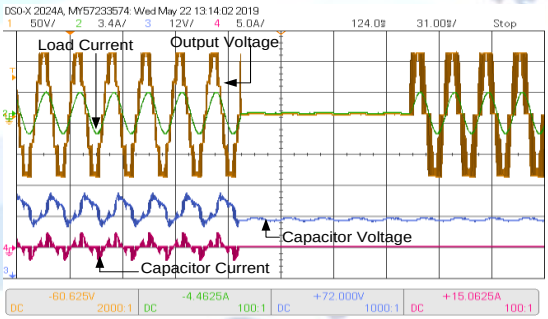


Fig 9 Opal-Rt results under the case of Multiple Switches Fault.

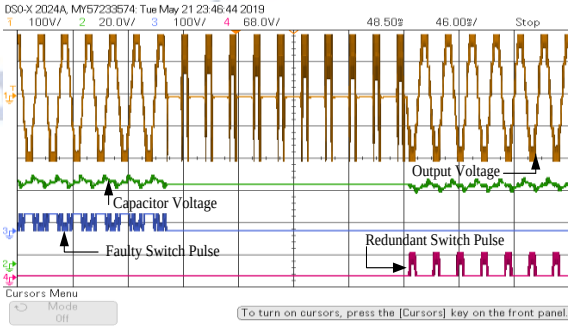


Fig 10 Opal-Rt result with capacitor voltage, faulty switch pulse, and redundant switch pulse under single switch fault scenario.

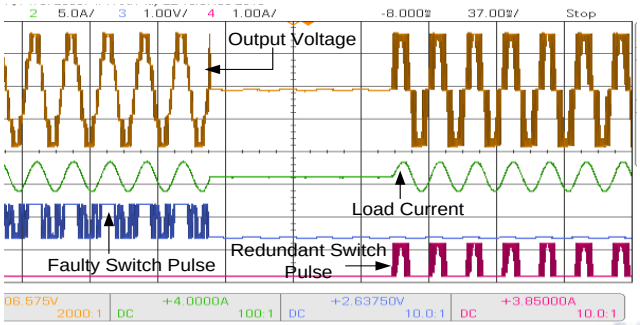


Fig 11 Opal-RT results under multiple switch fault scenario.

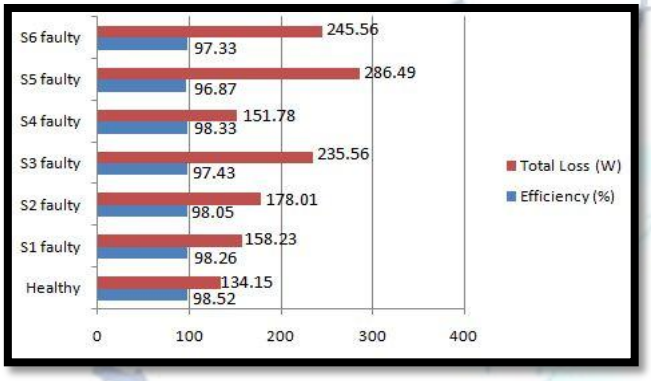


Fig 12 Total losses and efficiency of the presented inverter topology under both healthy and faulty condition.

V. CONCLUSION AND FURTHER DEVELOPMENT

The reliability of inverter is a prominent factor in multilevel inverters, as it ensures the continuity in healthy operation of inverter. In regard to this concern, a fault tolerant architecture of topology adopted for fault detection is proposed in this work which is shown in fig 4.1. This architecture has reduced device count and tolerance capabilities for both open as well as short circuit failure occurring on single and multiple switch/es. The redundant active neutral point clamped (ANPC) leg has equal blocking voltage when compared with main inverter architecture and delivers pre-fault output voltage for both single and multiple switch fault scenario. Also, the presented ANPC architecture as the redundant leg would enable fault tolerant characteristics to any conventional five level inverter topologies.

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