A Control Scheme of a Multilevel Inverter for Integration of Photo Voltaic Generating System with the Utility System

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Abstract: This paper proposes a design and analysis of single-phase five-level and seven-level grid connected inverter for photovoltaic systems, with a novel pulse width- modulated (PWM) control scheme and repetitive sequence method. In seven level grid connected inverter system, three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output- voltage levels (Vdc, 2Vdc/3, Vdc/3, 0, −Vdc, −2Vdc/3, −Vdc/3) from the dc supply voltage.

Keywords: Multilevel inverters, photovoltaic (PV) system, grid connected, pulse width-modulation (PWM), control system, repetitive sequence.

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INTRODUCTION

Today Photovoltaic (PV) Power system are becoming more and more popular,with the increase of energy demand and the concern of environmental pollution around the world .Four different system configuration are widely developed to grid connected power applications. The centralized inverter system,the string inverter system ,the multi string inverter sytem and the module integrated inverter sytem.The most important design constraint ooof thhhrre PV DG Is to obtain a high voltage gain. Fortypical PV module, the open-circuit voltage is about 21 V and the maximum power point (MPP) voltage is about 16 V. And the utility grid is 220 or 110 Vac. Therefore, the high voltage amplification is obligatory to realize the grid-connected function and achieve the low total harmonic distortion (THD).

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching,but it could also unfortunately increase switching losses, acoustic noise and level of interference to other equipment. Improving its output waveform reduces its harmonic content and hence, also the size of the filter used and the level of electromagnetic interference (EMI) generatedby the inverter's switching operation.

This paper recounts the development of a novel modified H-bridge 1-phase multi-level inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. Comparing the five-level inverters, seven-level inverters obtained more sinusoidal waveform. By using repetitive sequence method with grid frequency, a seven-level inverter is analyzed.

PROPOSED MULTILVEL INVERTER TOPOLOGY

2.1 Seven level Inverter Topology

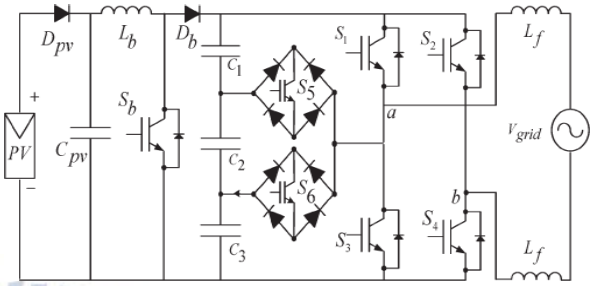

Fig.2.1 Proposed single-phase seven-level grid-connectedinverter for photovoltaic systems

The proposed single-phase seven-level inverter was developed from the five-level inverter in. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by *C*1, *C*2, and *C*3, as shown in Fig. 2.1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter.

The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid.

A filtering inductance *Lf* was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (*V*dc, 2*V*dc/3, *V*dc/3, 0, −*V*dc, −2*V*dc/3, −*V*dc/3) from the dc supply voltage.

The proposed inverter's operation can be divided into seven switching states, as shown in Fig. (a)– (g).Fig(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. (b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage.

The required seven levels of output voltage were generatedas follows.

1. Maximum positive output (*V*dc): *S*1 is ON; connecting the load positive terminal to *V*dc, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is *V*dc. Fig.(a) shows the current paths that are active at this stage.

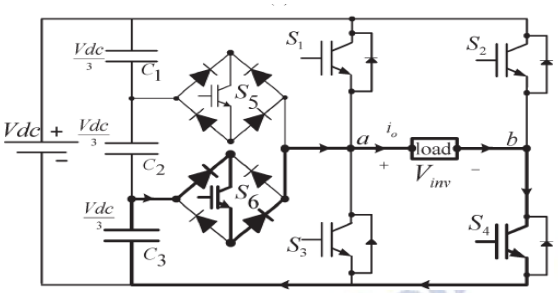

Fig 2.1(a). Switching combination required to generate theoutput voltage (*V*ab)

*V*ab = *V*dc.

2. Two-third positive output (2*V*dc/3): The bidirectional switch *S*5 is ON, connecting the load positive terminal, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 2*V*dc/3. Fig.(b) shows the current paths that are active at this stage.

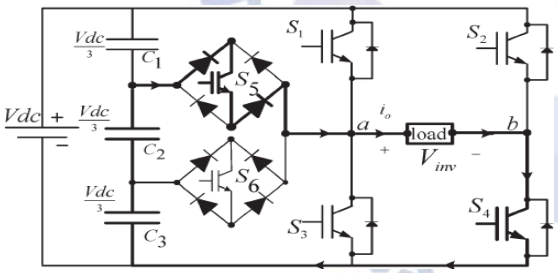

Fig 2.1(b). Switching combination required to generate theoutput voltage (*V*ab)

*V*ab = 2*V*dc/3.

3. One-third positive output (*V*dc/3): The bidirectional switch *S*6 is ON, connecting the load positive terminal, and *S*4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is *V*dc/3.
Fig. (c) Shows the current paths that are active at this stage.

Fig 2.1(c). Switching combination required to generate theoutput voltage (*V*ab)*V*ab = *V*dc/3.

4. Zero output: This level can be produced by two switching combinations; switches *S*3 and *S*4 are ON, or *S*1 and *S*2 are ON, and all other controlled switches are OFF; terminal *ab* is a short circuit, and the voltage applied to the load terminals is zero. Fig. (d) shows the current paths that are active at this stage.

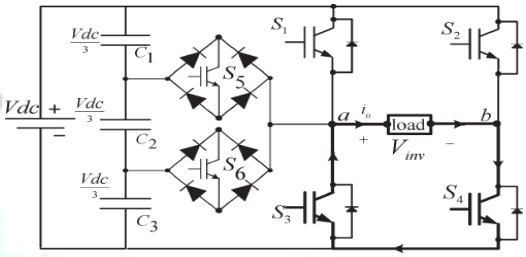

Fig 2.1(d). Switching combination required to generate theoutput voltage (*V*ab)*Vab* =0.

5. One-third negative output (−*V*dc/3): The bidirectional switch *S*5 is ON, connecting the load positive terminal, and *S*2 is ON, connecting the load negative terminal to *V*dc. All other controlled switches are OFF; the voltage applied to the load terminals is −*V*dc/3. Fig. (e) Shows the current paths that are active at this stage.

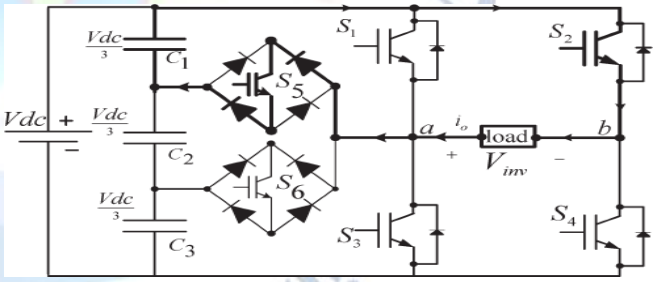

Fig 2.1 (e). Switching combination required to generate theoutput voltage (*V*ab)*V*ab = −*V*dc/3.

6. Two-third negative output (−2*V*dc/3): The bidirectional switch *S*6 is ON, connecting the load positive terminal, and *S*2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −2*V*dc/3. Fig. (f) shows the current paths that are active at this stage.

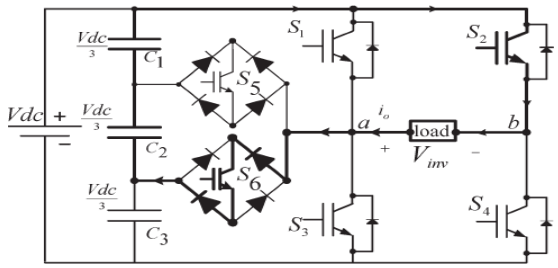

Fig 2.1(f). Switching combination required to generate theoutput voltage (*V*ab)*Vab* = −2*V*dc/3

7. C onnecting the load negative terminal to *V*dc, and *S*3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminalsis −*V*dc. Fig. (g) Shows the current paths that are active at this stage.

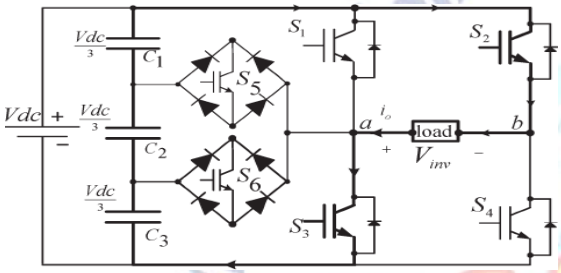

Fig 2.1(g). Switching combination required to generate theoutput voltage (*V*ab)*V*ab = −*V*dc.

Output voltage according to the switches on-off conditions:

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

Table 2.1 shows the switching combinations that generated the seven output-voltage levels (0, −*V*dc, −2*V*dc/3, −*V*dc/3, *V*dc, 2*V*dc/3, *V*dc/3)

PWM MODULATION:

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (*V*ref1, *V*ref2, and *V*ref3) were compared with a carrier signal (*Vcarrier*). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal.

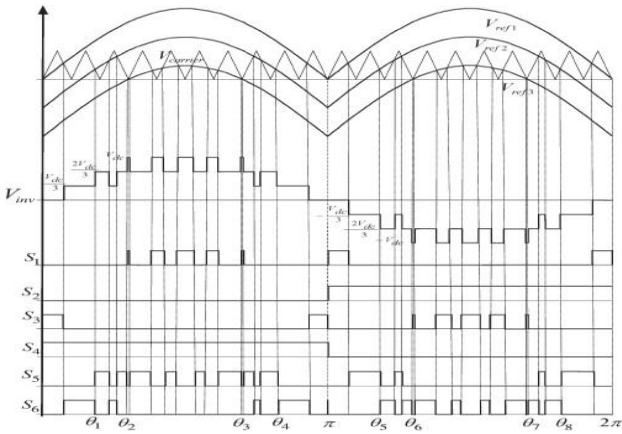

Fig 3.1: Switching pattern for the single-phase seven-level inverter.

If *V*ref1 had exceeded the peak amplitude of V carrier, *V*ref2 was compared with V carrier until it had exceeded the peak amplitude of V carrier. Then, onward, Vref3 would take charge and would be compared with V carrier until it reached zero. Once *V*ref3 had reached zero, *V*ref2 would be compared until it reached zero. Then, onward, *V*ref1 would be compared with V carrier. Fig. 3.1 shows the resulting switching pattern. Switches *S*1, *S*3, *S*5, and *S*6 would be switching at the rate of the carrier signal frequency, whereas *S*2 and *S*4 would operate at a frequency that was equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 3.2 shows the per unit output-voltage signal for one cycle. The six modes are described as follows:

Mode 1: $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$

Mode 2: $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$ Mode 3: $\theta 2 < \omega t < \theta 3$

Mode 4: $\pi < \omega t < \theta 5$ and $\theta 8 < \omega t < 2\pi$

Mode 5: $\theta 5 < \omega t < \theta 6$ and $\theta 7 < \omega t < \theta 8$Mode 6: $\theta 6 < \omega t < \theta 7$.

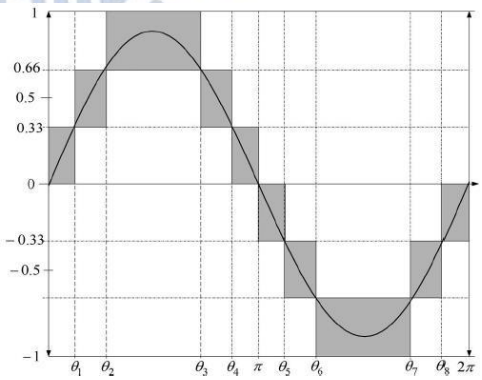

Fig 3.2. Seven-level output voltage (*V*ab) and switchingangles

CONTROL SYSTEM:

As Fig 4.1.Shows, the control system comprises a MPPT algorithm, a dc-bus voltage controller, reference- current generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, alsounder the presence of grid voltage harmonics.

The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owingto its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle.

If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm willoscillate around it.

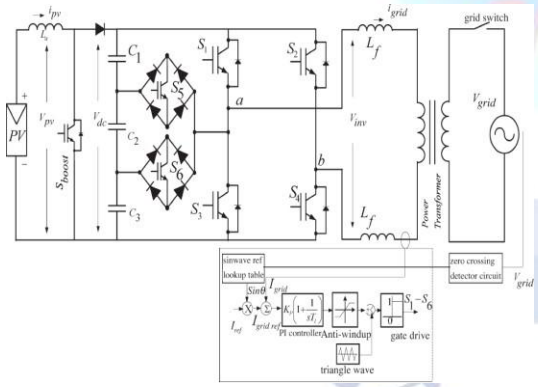

Fig 4.1 Seven-level inverter with closed-loop control algorithm

The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage *V*dc was controlled in the dc- ac seven-level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels.

To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (Vgrid). For this, the grid period and phase must be detected.

The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port on eZdsp board TMS320F2812.

A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current *I* grid, was sensed and fed back to a comparator that compared it with the reference current Igridref. *I*gridref is the result of the MPPT algorithm. The error from the comparison process of *I* grid and *I*gridref was fed into the PI controller.

The output of the PI controller, also known as Vref, goes through an anti-windup process before being compared with the triangular wave to produce the switching signals for *S*1–*S*6. Eventually, *V*ref becomes *V*ref1; *V*ref2 and *V*ref3 can be derived from *V*ref1 by shifting the offset value, which was equivalent to the amplitude of the triangular wave. The mathematical formulation of the PI algorithm and its implementation in the DSP are discussedin detail in.

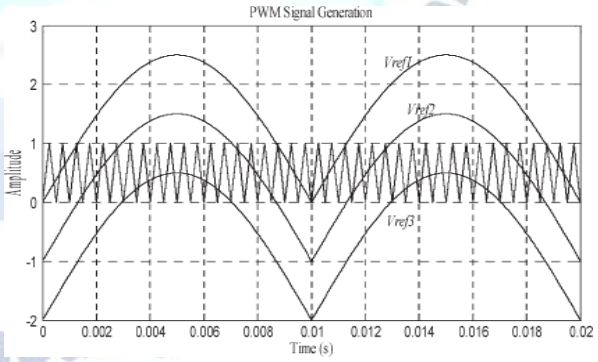

Fig 4.2: PWM switching signal generation.

SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (V_{ref1}, V_{ref2}, and V_{ref3}) against a triangular carrier signal.

Subsequently, the comparing process produced PWM switching signals forswitches S_1–S_6,

One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches S_5 and S_6 also operated at the rate of the carrier signal. shows the simulation result of inverter output voltage V_{inv}.

The dc-bus voltage was set at 300 V (> $2V_{grid}$; in this case, $V_{grid\surd}$ was 120 V). The dc-bus voltage must always be higher than 2 of V_{grid} to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between M_a =

0.66 and M_a = 1.0. V_{inv} comprises seven voltage levels, namely, V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, and $-V_{dc}/3$. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage. As I_{grid} is almost a pure sine wave at unity power factor, the total

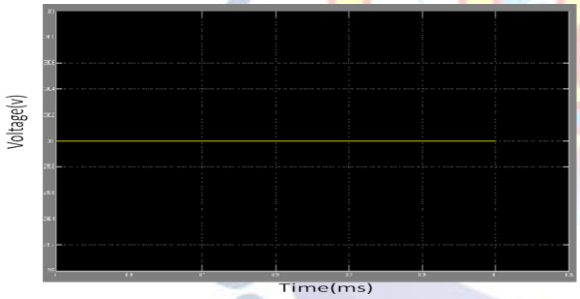

Fig.5.1: output voltage of boost converter harmonic distortion (THD) can be reduced compared with the THD in.

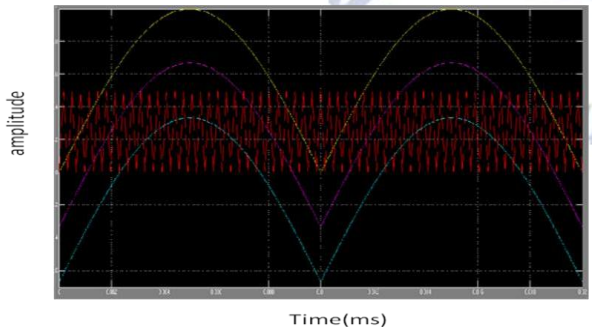

Fig.5.2 pulse width modulation switching signal generation

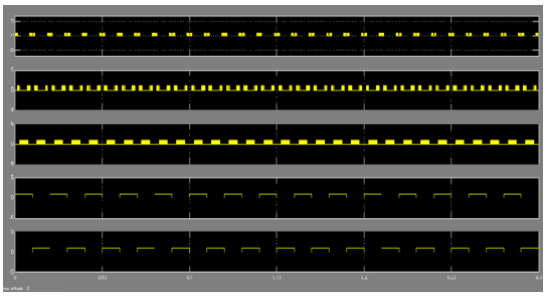

Fig.5.3 pulse width modulation switching signals

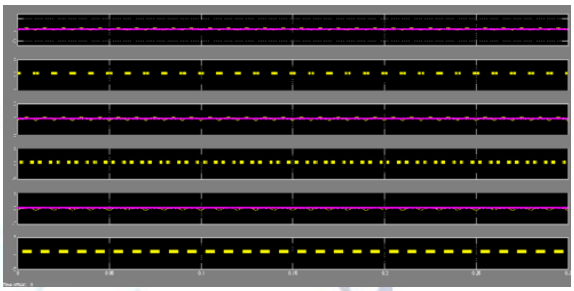

Fig.5.4 pulse width modulation switchingsignals for s1 to s6

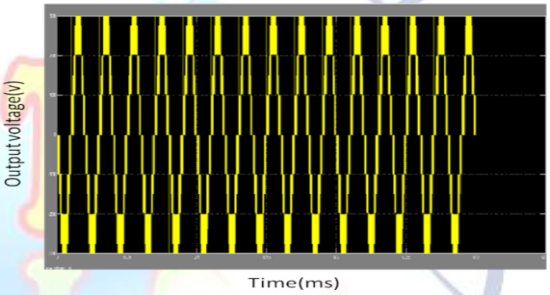

Fig.5.5 Experimental results for seven levels ofoutput voltage

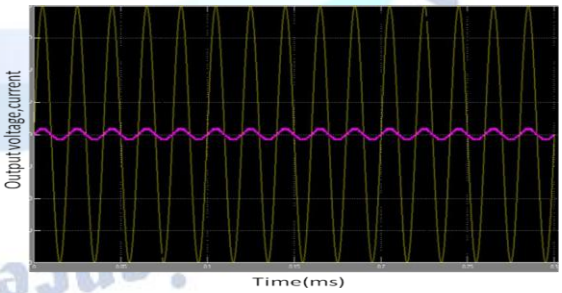

Fig.5.6 Experimental results for grid voltage andgrid current that are in phase

CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel

inverter was analyzed in detailed. By controlling the modulation index, the desired number of levels of the inverter output voltage can be achieved. Finally, a seven-level multilevel converter with reduced number of switches is proposed. By using repetitive sequence method with grid frequency, a nine-level inverter is analyzed.

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