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International Journal for Modern Trends in Science and Technology, 7(05): 206-211, 2021

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST0705035
Available online at:http://www.ijmtst.com/vol7issue05.html

Quasi Power Factor Correction for High Efficient AC/DC Converter

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To Cite this Article
Ankamreddi Venkataramana; K.Narendrababu and D Ravi Kishore. Quasi Power Factor Correction for High Efficient AC/DC Converter. *International Journal for Modern Trends in Science and Technology* 7, 206-211 (2021).

Article Info
Received on 26-April-2021, Revised on 17-May-2021, Accepted on 26-May-2021, Published on 28-May-2021.

ABSTRACT

Harmonic pollution and low power factor in power systems caused by power converters have been of great concern. To overcome these problems several converter topologies using advanced semiconductor devices and control schemes have been proposed. This investigation is to identify a low cost, small size, efficient and reliable ac to dc converter to meet the input performance index of UPS. The performance of single phase and three phase ac to dc converter along with various control techniques are studied and compared. This project presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the lowfrequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. Since the use of a single inductor, the cost z reduced a lot and the efficiency of the system is improved. The power factor is maintained constant by using a buffer capacitor in parallel to the system for compensating the inductive components. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. Finally an R- load is applied and simulation results are presented

1. INTRODUCTION

Conventional offline power converters with diode capacitor rectifiers have resulted in distorted input current waveforms with high harmonic contents. To solve these problems, so as to comply with the harmonic standards such as IEC 61000-3-2, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improving the power factor is a two-stage power conversion approach .The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed .These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation. Usually, the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation. A detailed review of the single stage PFC converters is presented.

Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate dc bus voltage stress. To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented in which a high frequency ac voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current (Fig.1.1). The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source.

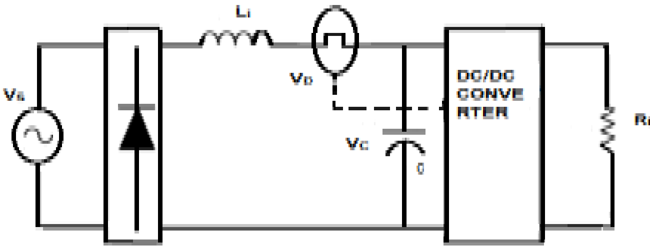

Fig.1.1 General Circuit diagram of dither rectifier with PFC cell.

Another technique based on parallel connection of this dither signal is presented however; the harmonic content can meet the regulatory standard by a small margin. A new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values.

PROPOSED QUASI-ACTIVE PFC CIRCUIT

In this project, a new technique of quasi-active PFC is proposed. The PFC cell is formed by connecting the energy buffer ( ) and an auxiliary winding ( ) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor operates in DCM such that a lower THD of the input current can be achieved.

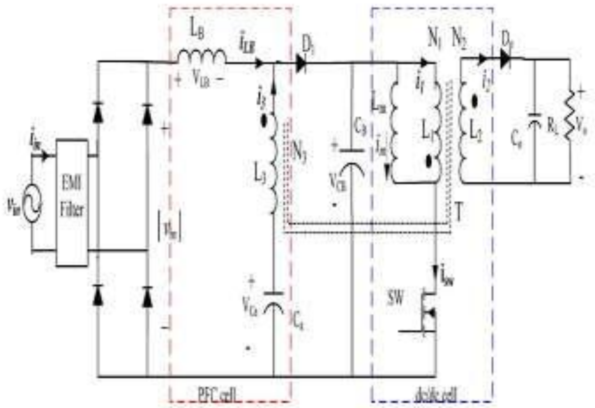

Fig. Proposed quasi-active PFC circuit diagram

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 2.2, the circuit comprised of a bridge rectifier, a boost inductor , a bulk capacitor Ca in series with the auxiliary windings , an intermediate dc-bus voltage capacitor ,and a discontinuous input current power load, such as fly back converter. The fly back transformer (T) has three windings , , and . The secondary winding = 1 is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with highfrequency pulsating source. The quasi active PFC cell can be considered one power stage but without an active switch.

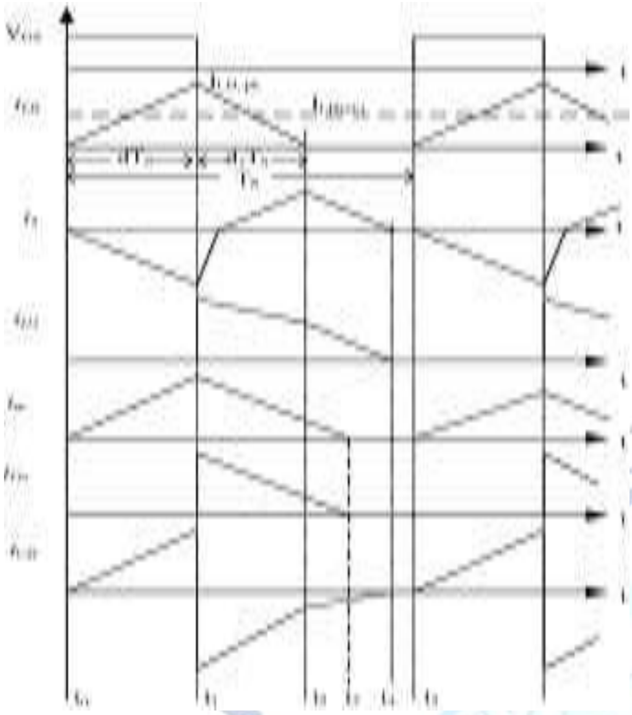

Fig key switching waveforms of the PFC circuit. To simplify the analysis, the following assumptions have been made. 1.All semiconductors components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively. 2.The power transformer does not have the leakage inductances because of the ideal coupling. 3.All the capacitors are high enough so that the voltage across them is considered constant. 4.Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

Conventional circuit Drawbacks

Low output power
Low efficiency
Poor power factor
More input current harmonics

Advantages of Conventional Circuit

Less voltage spike
High output power
High efficiency
Improve the input power factor
Reduce the input current harmonics

Applications of Conventional Circuit

Battery charging
Battery operated Electric vehicle
Telecom applications
Power supply for DC motor

Power Factor Correction

The cosine of the angle between voltage and current in an Ac circuit is stated as the Power factor. There is normally a phase difference Ø among the voltage and current in an Ac circuit. If the circuit is inductive, the current lags after the voltage and power factor is denoted as lagging. Where leading is stated as, the current leads the voltage and the power factor in the capacitive circuit.The ratio of real power to apparent power is the standard definition of power factor. With the cosine angle between them the real or average power is calculated as the product of the voltage and current magnitudes multiplied, whereas the product of the root mean square values for the apparent power.

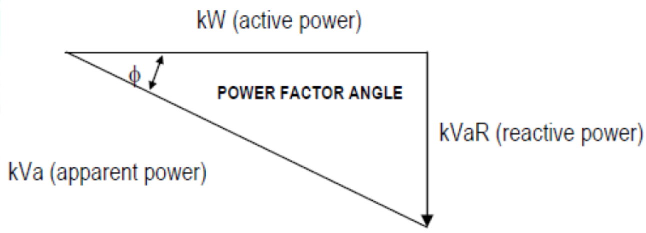

Fig 1: Power Triangle

Power Factor is usually specified as a number between 0 and 1, and is equal to the ratio of reactive power to active power, or Cosine φ, as presented above. The increase in power factor number makes the system more efficient. Thus, a system with a Power Factor of 0.9 is much more efficient than the power factor with 0.6.

$$\text{Power Factor} = \frac{Real\ Power}{Apparent\ Power}$$

A high power factor is generally required in a transmission system to decrease transmission losses and to improve voltage regulation at the load. To regulate the system power factor to close to 1.0 is often needed. The load produces purely sinusoidal current and voltage in a linear system. By only the phase difference between voltage and current the power factor is found out. When two sinusoidal signals are considered with the same frequency, power factor can be clear in terms of the phase angle between them, i.e.,

$$Power\ Factor = \cos \emptyset$$

The phase angle representation alone is not valid, because of the non linear performance of the active switching of power devices in non linear systems similar to power electronic systems. Typical biased line current draws a non linear load from the line. The *PF* for sinusoidal voltage and non-sinusoidal current can be said as

$$\text{Power Factor} = \frac{V_{rms}\, I_{1rms}}{\mathrm{V_{rms}\, I_{rms}}} \cos\emptyset$$

$$\text{Power Factor} = \frac{I_{1rms}}{\mathrm{I_{rms}}} \cos\emptyset$$

$$\text{Power Factor} = \mathrm{K_f} \cos\emptyset$$

Where, K_f is given as the purity factor or the distortion factor

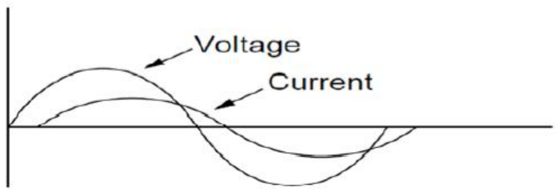

Fig 2: Traditional poor power factor (the current either leads or lags the voltage)

Poor Power Factor should be modified as it considerably raises costs. The purpose of a power factor correction circuit is to power the converter to look alike a resistive load to the line. A resistive load has zero degree phase displacement amongst its current and voltage waveforms (and no added harmonics).

Rectifier and Boost Converter

The circuit scheme of the proposed power factor correction converter consists of an full wave bridge AC-DC rectifier and a modified boost converter. From a sinusoidal ac input waveform a rectified ac output generated is the purpose of the full wave rectifiers. It ensures this by means of the nonlinear conductivity characteristics of diodes to direct the path of the current.

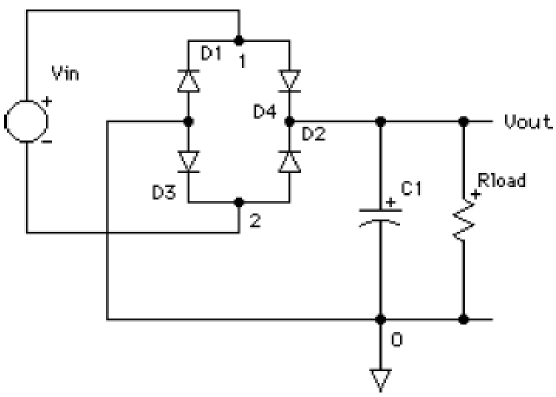

Figure 3. Filtered full wave rectifier

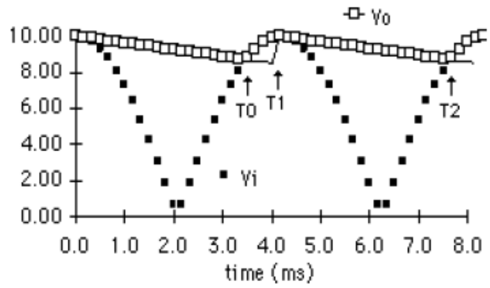

Figure 4. Output (Vi) and input (Vo) of a filtered full wave rectifier

The filtered full wave rectifier is obtained from the FWR by calculating a capacitor during the output. The FWR output is the outcome of the addition of a capacitor. The output is presently a pulsating dc, during a peak to peak variation is recognized as ripple. The input voltage magnitude and frequency be obtained during the magnitude relies of the ripple, through the filter capacitance, as well as the load resistance.

For the duration of the time period since T0 to T1, the diode D1 (or D3, based on the segment of the signal) is forward biased then Vi > VC1 (inexact the forward biased diode as a short circuit). When the capacitor C1 get charged due to the voltage across the load R increases. Starting from] T1 to T2, the D1 and D2 diodes are biased reversely (open circuit) as Vcap>Vi, and then the capacitor get discharge over the load R during a time constant of RC seconds. Along a capacitor discharge arc the voltages among times t1 and t2 set. Through which the output voltage is,

$$V_{0ut}(t) = V_{mx} e^{\frac{-t+t1}{RC}}$$

The peak to peak (pp) ripple is indicating as the voltage difference between Vmax and Vmin

$$V_{Ripp}(pp) = V_{out}(t1) - V_{out}(t2) = V_{mx} - V_{mn}$$

$$= V_{mx}\left[1 - e^{\frac{-t2+t1}{RC}}\right]$$

If C is huge, such that RC >> T2 - T1, we can estimate the exponential

$$1 - e^{\frac{-t2+t1}{RC}} \text{ as } 1 + \frac{-t2+t1}{RC}.$$

Then t2 - t1 ~ t/2, somewhere t is the period of the sine wave, now

$$V_{Ripp}(pp) = V_{mx}\frac{t}{2RC} = \frac{V_{mx}}{2fRC}$$

After the rectification of dc voltage is deposit to the boost converter using snubber circuit. A boost converter is just like a particular kind of power converter ,here the output DC voltage is greater than that of the input DC voltage. This kind of circuit is used to 'step-up' a source voltage is greater than that the regulated voltage, leasing one power supply to offer different driving voltages. It is a part of switching-mode power supply, its including as a minimum two semiconductor switches (a diode and a transistor) and least one energy storage factor. After the transistor is conducted , the conventional boost converter current is being drawn in excess over the inductor and at the present, the energy is being stored in the inductor. When the transmission of current through the inductor cannot change immediately when transistor stops conducting the inductor voltage flies back or reversed.

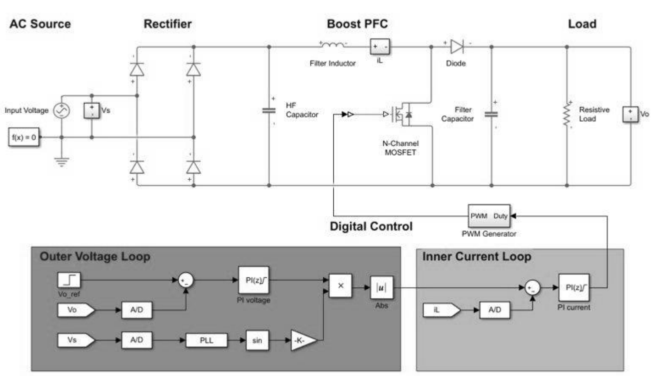

Fig 5: Simulink model of digitally controlled boost power factor correction.

Simulation Diagram:

The proposed simulation circuit shows how to correct the power factor using a PFC pre-converter. This technique is useful when non-linear impedances, such as Switch Mode Power Supplies, are connected to an AC grid. As the current flowing through the inductor is never zero during the switching cycle, the boost converter operates in Continuous Conduction Mode (CCM). The inductor current and the output voltage profiles are controlled using simple integral control. During start up, the reference output voltage is ramped up to the desired voltage.

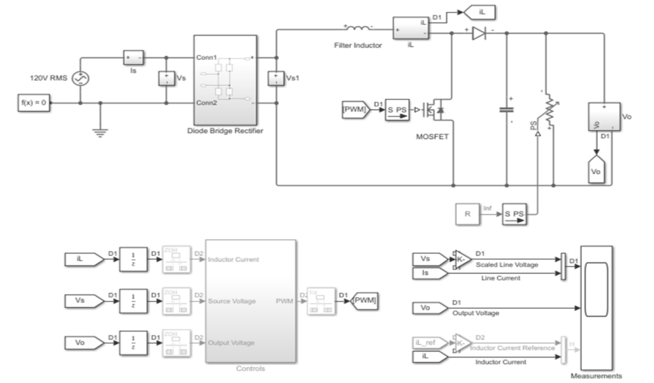

Fig 6: Simulation Circuit for Power Factor Correction for Continuous conduction mode

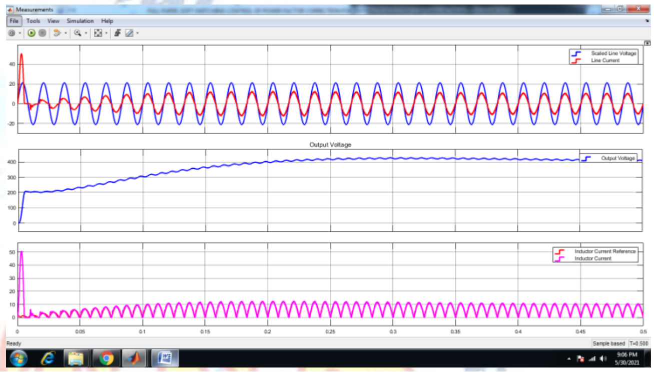

Fig 7: Simulation Results (a)line voltage and current (b)output voltage and (c) Inductor reference and actual current

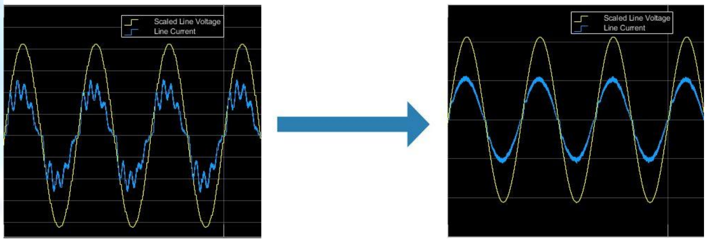

Fig 8 : Harmonic distortion in line current (blue) and after power factor correction (yellow).

Conclusion

The main objective throughout the project is to improve the Power Factor with active snubber circuit for the parallel boost converter. Simulations were initially done for conventional boost converter with snubber circuit. The changes in the input current waveform were saw and calculated. A PFC circuit having a parallel boost converter i.e. dual boost converters arranged in parallel was designed with soft switching which is provided by the active snubber circuit. For this idea, only one auxiliary switch and one resonant circuit is operated. The main switches and all the other semiconductors are switched by ZVT and ZCT techniques. The active snubber circuit is applied to the parallel boost converter, which is fed by rectified universal input ac line. This latest PFC converter is achieved with 200 V ac input mains. The diode is added in order to the auxiliary switch path to avoid the incoming current stresses as of the resonant circuit to the main switch. It is noticed that the Power Factor and the efficiency is better for Dual Boost Converter Circuit. Finally, 98% efficiency at full load is achieved and the power factor is reached to 99.97% for the proposed converter. Due to the main and the auxiliary switches have a common ground, the converter can easily control. The proposed new active snubber circuit can be simply functional to the further basic PWM converters and to all switching converters. The proposed converter does not need any further passive snubber circuits.

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