International Journal for Modern Trends in Science and Technology, 7(05): 72-80, 2021

ISSN: 2455-3778 online
DOI: https://doi.org/10.46501/IJMTST0705011
Available online at:http://www.ijmtst.com/vol7issue05.html

Multicarrier PWM Based Control of Modular Multilevel Inverter with Grid Connected Solar PV System

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To Cite this Article
Saminathan S & Dr. Ranjithkumar K. Multicarrier PWM Based Control of Modular Multilevel Inverter with Grid Connected Solar PV System. *International Journal for Modern Trends in Science and Technology* 7, 72-80 (2021).

Article Info
Received on 16-April-2021, Revised on 28-April-2021, Accepted on 03-May-2021, Published on 09-May-2021.

ABSTRACT

In this work, a new modular multilevel inverter topology is introduced for a single phase grid connected Photovoltaic system. This multilevel inverter use less number of switches to generate seven levels compared to other conventional multilevel inverters. This requires only one isolated dc source to operate. So it is suitable for renewable energy application. This inverter is designed by submodule configuration; each sub module contains two switches and one DC link capacitor. The sub modules will be added to the inverter depending on number of levels. The voltage balancing of DC link capacitor is carried out by Y matrix PWM technique. Because of Y matrix PWM technique, the inverter gets a self capacitor voltage balancing ability. So there is no need of external devices required for balancing the voltage of capacitor. A PLL for grid integration and LCL filter are designed and integrated with this inverter. The simulation of proposed system is carried out by MATLAB/ SIMULINK and performance of THD is monitored as per standards

KEYWORDS: *Phase locked loop (PLL), Total Harmonic distortion (THD), Pulse Width Modulation (PWM)*

I. INTRODUCTION

In these days, scarcity of electricity is increased throughout the world. So we require more energy without affecting environment. The photovoltaic energy generation is suitable for these requirements. When PV system is connected to grid, the inverter act as a major part to convert DC into AC. Generally lot of inverter topologies is used to convert DC into AC. In these Multi level inverter topologies is very important one. Because, multilevel inverter has become indispensable for most power electronic application in medium and high voltage ranges. Multilevel converters cannot only achieve high power ratings, but also enable the use of renewable energy, such as photovoltaic, wind, and fuel cell can easily interface with multilevel inverter system for high power applications. Besides the advantages of obtaining lower THD and reducing the total dv/dt across the semiconductor switches, it can be any number of levels to suit the high voltage and power application demands.

The neutral point clamped topology, flying capacitor topology and cascaded H bridge multilevel inverter topology are some basic topologies of multilevel inverter. In addition to these topologies, the major modulation strategies for switching on and off the switches in the multilevel inverter are the sinusoidal pulse width modulation (SPWM), selective harmonic elimination pulse width modulation (SHE-PWM), space vector pulse width modulation (SVM).

II. LITERATURE SURVEY

Hosseinzadeh, et al [1] discusses the multilevel inverter with reduced no of switches and it explains the operations and compares its performance with conventional strategies. Nirmal mukundhan, et al [2] discusses the operation and modelling of standalone PV power generators with isolated zeta converter for DC to DC conversion.

Albert Alexander stonier, et al [3] discusses the various faults in PV system and also explains to overcome the faults in entire PV system by using intelligent controller. Gabriel, et al [4] discusses the general procedure and conditions to calculate the parameter values of LCL filters. Qichen Yang, et al [5] discusses the modular multilevel converter (MMC) by using Y matrix PWM technique. Liu,et al [6] discusses the clean view about the Y matrix PWM technique and implement in the MMC. Jiang, et al [7] discusses the comparative study of three topologies of Multilevel inverter (MLI) and also discusses the sine PWM technique.

Appana dekka, et al [8] explains design procedures, control techniques, types of MMC and it will give a clear idea about Y matrix PWM technique. Sandeep, et al [9] discusses the overview of MLI with reduced no of switches and it has been developed from the reversing voltage topology.Zhang, et al [10] discusses the emerging trends of multilevel inverter and examining the different MLI. Gayathri devi, et al [11] explains the various voltage balancing techniques of DC link capacitor by using various external circuits. Narimani et al [12] discusses the new method of capacitor voltage balancing without use of lookup table and this technique balances the dc link capacitor voltage based on minimum energy property.

III. MODELLING OF PROPOSED INVERTER

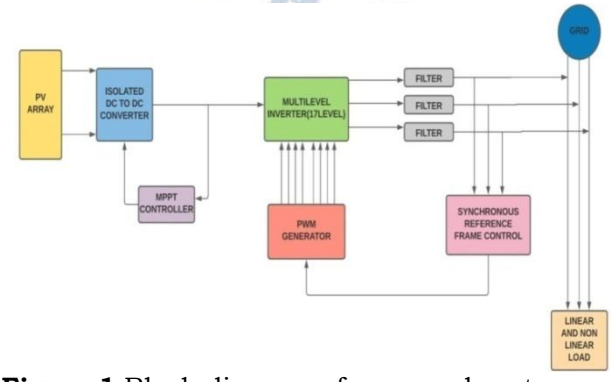


Figure 1 Block diagram of proposed system

The block diagram of an Enhanced multilevel inverter with grid connected PV system is shown in Figure 1. The PV array and isolated DC to DC converter with MPPT controller form the DC source for Multilevel inverter. Then Multi level inverter helps to convert the DC into AC. The switches of multilevel inverter are triggered by Y matrix PWM technique. After conversion of DC into AC, the filter is helps to eliminate the harmonics. After filtering the output of the inverter is connected to the Grid.

Before interconnection with Grid, the synchronization of supply and grid is carried out by Phase locked loop (PLL). From the PLL, the exact position of Grid voltage is sensed. Because of these PLL data, the PWM generation is carried outto turn on and turn off the inverter switches

3.1 MULTILEVEL INVERTER

The newly developed proposed multilevel inverter is shown in Figure 2. The proposed inverter is uses less no of switches compare to other conventional methods. This inverter is designed based on submodule configuration. In each submodule two switches and one DC link capacitor are there. Depending on no of levels, the submodules will be added to the inverter. This inverter only requires only one isolated DC source. . The no of levels m=2S+1. Where, S=no of sub modules. In this case, we require three stages (VDC, 2DC, 3VDC) of input. So we require three submodules to produce seven levels. Totally this proposed inverter requires ten switches and three link capacitors to produce 7 levels. The six switches are placed in the submodules and another four switches are used to switch the positive and negative cycle to generate AC signal.

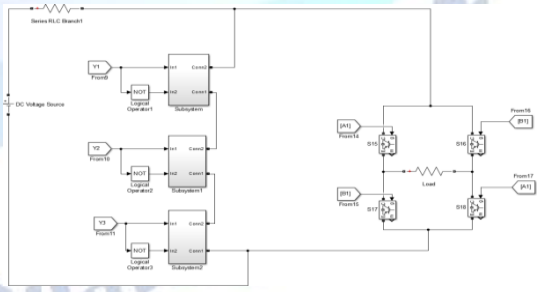


Figure 2 Simulation diagram of proposed inverter

3.2 HALF-BRIDGE SUBMODULE

The principal advantage of the topology of the half bridge submodule is its versatility and reduced switch number. The submodule half-bridge (HB) is also called a chopper unit. The half bridge submodule circuit configuration is shown in Figure

3. It is composed of two antiparallel diode IGBT devices and one DC capacitor (C).

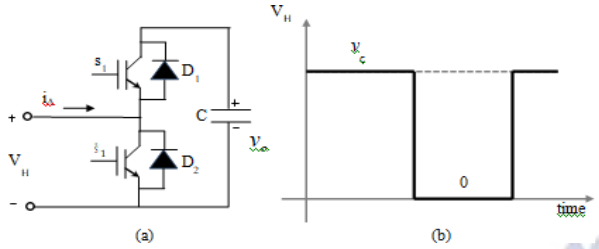


Figure 3 Half bridge submodule

The two IGBT devices were worked complementarily to control the voltage of the DC capacitor at such a rate of Vc. The voltage of the DC capacitor is provided by the

$$Vc = \frac{1}{C}\int_0^t ic(t)dt \qquad (1)$$

The current of a DC capacitor in terms of AC current (i_A) as well as theswitching state of a upper switch S1 is given below

$$i_c = s_1 i_A \qquad (2)$$

Capacitor is charging or releasing relying upon the bearing of the currentthrough the submodule. The submodule is supposed to be INSERTED if S1 is ON, In the contrary case, the submodule is BYPASSED if S1 is OFF. The output voltage of the half bridge submodule has two voltage levels, "0" and "Vc," as can be seen in Figure 3.2(b). The output voltage of the sub module (VH) is equivalent to the capacitor voltage Vc whenever the top switch S1 is "ON." throughout this mode the voltage of the DC capacitor boosts for the positive side of the current and falls in the negative path of the current. When the upper switch S1 is "OFF," the output voltage VH is identical to "0." within that mode the DC capacitor voltage stays unchanged, irrespective of current path. The appropriate switching status is outlined in Figure 4. The half-bridge submodule output voltage can be defined in terms of the DC capacitor voltage and the switching condition of thetop switch S1as

$$V_H = S_1 v_c \qquad (3)$$

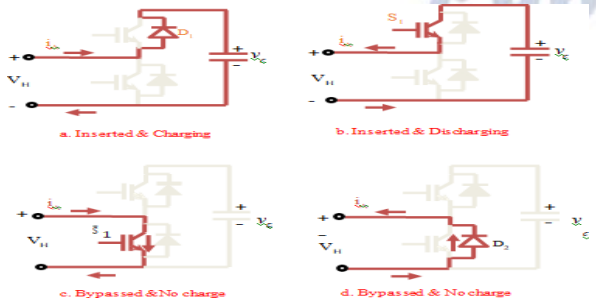


Figure 4 Working of half bridge submodule

3.3 Y MATRIX PWM TECHNIQUE

There is lot of PWM techniques used to trigger the conventional multilevel inverters. These methods are phase disposition, phase opposition disposition, Alternate phase opposition disposition, carrier overlapping, variable frequency carrier, switching frequency optimal. But in the proposed inverter these methods are not possible. Because of these methods, in each sub module DC link capacitor voltage goes to unbalanced condition. This is the main disadvantage of the conventional PWM techniques. So we move on Y matrix PWM technique to achieve the capacitor voltage balancing.

After some arithmetic operation of Phase Opposition and disposition technique we get required Y matrix switching function. By using Y matrix PWM technique the switches of inverter will be turned on and turned off by all the possible ways to achieve corresponding level. When the output of PWM block is „1" the sub module will be inserted in the inverter otherwise the sub module will be bypassed from the inverter.

The table 1 shows all the possible ways to achieve different levels of inverter. In this Y1 includes all possible patterns of sub modules whenever the inverter voltage will achieve the level 1 voltage. Y2 includes all possible patterns of sub modules whenever the inverter voltage is achieve level 2. Similarly Y3 includes all possible patterns of sub modules whenever the inverter voltage will achieve the level 3. During this transition the capacitors C1, C2 and C3 is connected to the inverter according to the switching pattern of each sub modules

Table 1 switching function of different switches

Matrix	Levels	S1	S2	S3	S4	S5	S6
Y0	0Vdc	0	0	0	1	1	1
Y1	1Vdc	0	0	1	1	1	0
	1Vdc	0	1	0	1	0	1
	1Vdc	1	0	0	0	1	1
Y2	2Vdc	0	1	1	1	0	0
	2Vdc	1	0	1	0	1	0
	2Vdc	1	1	0	0	0	1
Y3	3Vdc	1	1	1	0	0	0

The corresponding matrixes are getting from the switching function table.

$$Y0 = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \qquad Y3 = \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}$$

$$Y1 = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \qquad Y4 = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$$

3.4 DESIGN OF LCL FILTER

Grid filters, also known as line filters, are connected between power inverter and the utility grid. The two main functions of a grid filter are: 1) to reduce high frequency harmonics caused by the PWM modulation to improve the power quality supplied to the grid, and 2) coupling the impedances between two voltage sources, power inverter and utility grid, preventing occurrence of short circuit by connecting directly power inverters to the grid.

Some of the techniques used to control harmonics injection to the grid are magnetic flux compensation, injection controlled of harmonics in the current, multilevel converters and passive filters. The passive filter topology is simple and inexpensive compared to other filtering techniques. L and LCL filters are the most used topologies for passive grid filters. L filter consists of an inductor connected in series between the inverter and the grid. Attenuation of the L filter is -20dB/dec over the full frequency range. When the L filter is used, switching frequency in the inverter must be high, allowing the L filter to reduce the total harmonic distortion (THD) with reasonable size, weight, and cost.

The LCL filter is composed of two inductors and one capacitor shown in Figure 5. Attenuation of the LCL filter is -60dB/dec for the higher order harmonics to the resonant frequency. The LCL filter reduces current and voltage harmonics in the inverter output more effectively compared with L filter.

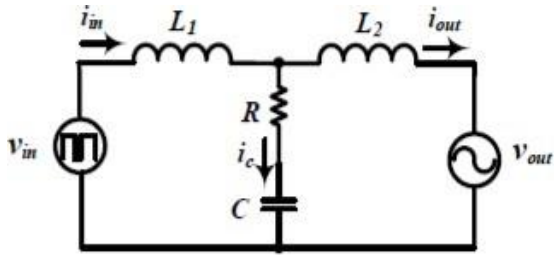


Figure 5 Circuit diagram of LCL filter

3.4.1 DESIGN OF INVERTER SIDE INDUCTOR

$$L1 \leq \frac{0.05 * Vline * \delta}{\Delta iout * fsw}; L1 \leq 46.8mH; \qquad (4)$$

L1=46mH

Vline- Line voltage

□- Maximum width of PWM

Δiout- Maximum ripple current (20% of rated current)

3.4.2 DESIGN OF GRID SIDE INDUCTOR

The range 5 <$XL1$ /$XL2$ < 10 allows to reach low amplitude ripples in the output current, preserving low volume, low weight and low cost in the inductors. The following equation allows calculating approximate value of the inductor L_2,

$$\frac{1}{10} * L_1 \leq L_2 \leq \frac{1}{5} * L_1$$

4.68≤L2≤9.3

According to the condition L2 is taken as,

L_2=9mH

3.4.3 DESIGN OF CAPACITOR

Capacitor value is selected to achieve increased attenuation near to switching frequency, producing a low reactance at the grid frequency. The capacitor must absorb little reactive power to the grid frequency, preventing a significant increase of current in the inductor $L1$.

Reactive power in capacitor (QC) can be calculated by the following expression

$$Qc = 2 * \pi * fnet * C * Vline2 \qquad (5)$$

To maintain low QC in comparison with the nominal active power of power inverter (P), QC is selected such that

$$15\% \; of \; P \leq Qc \leq 25\% \text{ of } P$$

The value of capacitor is calculated by below formula, in this reactivepower Qc is taken as 20% of P,

$$C = \frac{0.2 * P}{Qc} \qquad (6)$$

Capacitor impedance at switching frequency should be lower than impedance of the inductor L2, allowing high frequency harmonics to be

mitigated by the presence of the capacitor C. Such that

$$\frac{1}{10} * XL2 \leq XC \leq \frac{1}{5} * XL2$$

According by this condition Capacitor value "C"

$$C = 20uF$$

is taken as,

3.4.4 DESIGN OF DAMPING RESISTOR

Resistance to passive damping can be selected with the following equation,

$$R = \frac{1}{3} * Xc = \frac{1}{3} * \left(\frac{1}{2*\pi*f0*C}\right) = 2.5ohm \qquad (7)$$

3.4.5 SELECTION OF RESONANCE FREQUENCY

Resonance frequency ($f0$) must be selected to be located away from harmonics generated by the power inverter. The frequency $f0$ can be selected with the equation

$$500 \leq fo \leq 5000$$

$$10 * fnet \leq f0 \leq \frac{1}{2} * Tswitch \qquad (8)$$

3.5 MULTILEVEL INVERTER WITH GRID SYNCHRONIZATION

The inverter is synchronized with grid by using PLL and current control scheme is shown in Figure 6. The PLL is helps to find the phase angle of the grid and the current controller is helps to inject the maximum current into the grid. The algorithm of overall control scheme is as following, when the PLL detects the frequency and phase of the grid voltages, the phase angle is used to be a reference for the two phase transformation of the grid voltages and the output currents. Then the reference current and actual current are compared by current controller. Then the voltage reference is generated and it is given to the PWM generator. By the comparison of reference voltage signal and carrier signal the PWM pulse is generated. So the converted voltage of inverter should be matched with voltage of grid and current should be injected into grid.

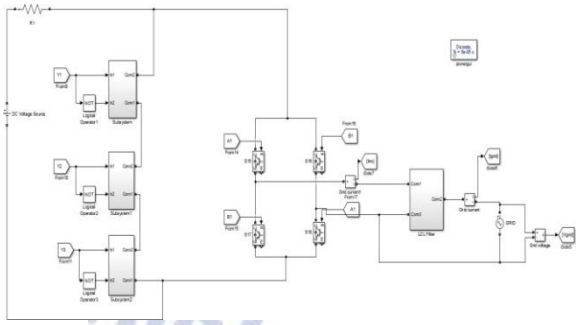


Figure 6 Simulation diagram of grid connected inverter

3.5.1 PHASE LOCKED LOOP (PLL)

The inverter output current that is injected into the grid must be synchronized with the grid voltage. The objective of the synchronization algorithm is to extract the phase angle of the grid voltage. The PLL is the most common synchronization algorithm for extracting the phase angle of the grid voltage. The phase locked loop (PLL) is a closed loop frequency control system. The main function of PLL in grid-connected system control is to create the angle θ of the d-q coordinates and synchronize the output voltage fromthe PV system with grid voltage and current.

The PLL is implemented in synchronous (dq) reference frame shown in Figure 7. „V" is the sensed grid voltage which is then transformed into DC components by connecting the two first order filter in series and transformation (αβ→dq). And the q component of voltage is compared with the reference and error passes through PI controller. The nominal grid frequency is added to the output of the PI controller, and the sum passed through an integrator to get the grid voltage angle θ. By this we find the phase angle of the grid voltage.

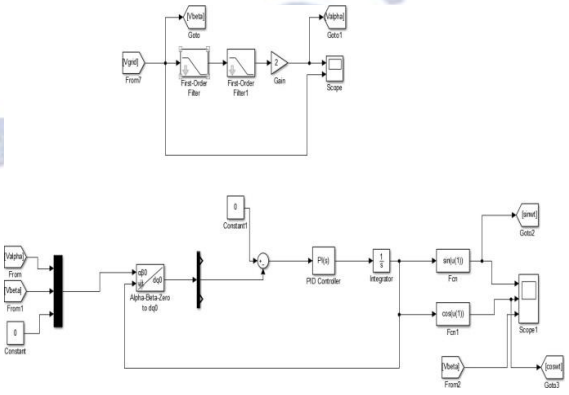


Figure 7 Simulation diagram of Phase Locked loop

3.5.2 TUNING OF PI CONTROLLER USED IN THE PLL

Set K_i =0 and K_p =1 (start with less than 1 if needed) and run the simulation. Look at the scope at the output of the PI controller. If the oscillations are under damped, increase the K_P to 1.1 (or more) while still keeping K_i =0 until you get sustained oscillation at the output of the PI controller shown in Figure 8. Note the value of the K_p at which you get sustained oscillation and take it as K_u. Also note down the time period of sustained oscillation and note it as T_u shown in Figure 9.Now find the new value of K_p and K_i by using the Tyreus-Luyben correction formula and feed it into the PI controller to get the required output voltage.

Tyreus-Luyben correction formula:

Proportional gain k_p = 0.31*k_u = 0.31*1.4 = 0.434

Integral gain $ki = \frac{kp}{2.2*Tu} = \frac{0.434}{2.2*0.00112} = 176.13$ (9)

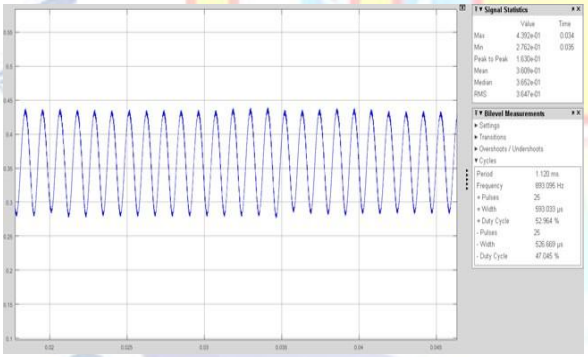


Figure 8 Showing at K_p =1.4, sustained oscillations are achieved (note it downas K_u)

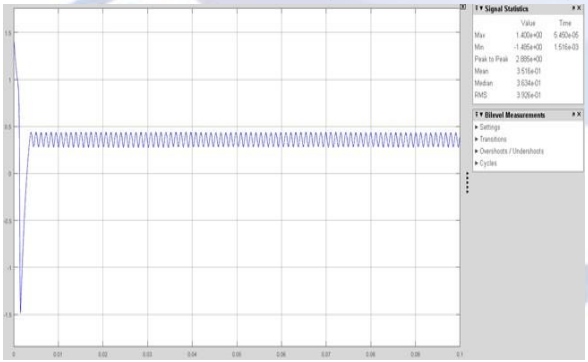


Figure 9 Showing the time period of undamped oscillation as 1.12ms (T_u)

3.5.3 TUNING OF PR CONTROLLER USED IN CURRENT CONTROLLER

A proportional resonant controller is used for the replacement of PI controller. It will perform in the grid integration system well compare to PI controller. PR controller introduces an infinite gain at the fundamental frequency and it helps to achieve zero steady state error quickly. This is the main advantage of PR controller compare to PI controller.

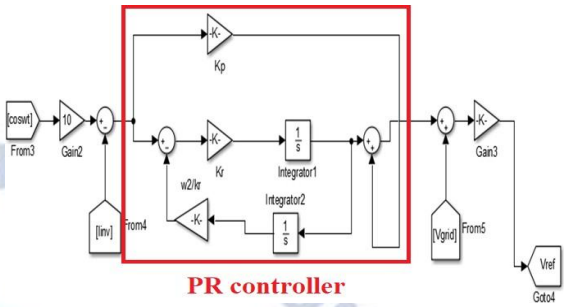


Figure 10 Current controller

The gain values of PR controller are the parameters to achieve zero steady state error quickly. The Gain values represented as K_P, K_r and w^2 /K_r shown in Figure 10. The gain value of K_P is depends on filter parameter (L1).

Filter parameters: L1=46mH; L2=9mH; C=20uF

Set controller time constant as 150uS

Value of K_P =Inductance (L1)/ time constant=20.33

Value of Kr=100 (directly takes as constant value)

Value of w^2 /K_r= $(2*pi*f)^2/K_r$=986.83

The corresponding gain values are used to achieve the zero steady state error. Because of this, the current controller injects the constant current into the grid continuously without error. The current controller also controls active and reactive power injection into the grid.

IV. RESULTS AND DISCUSSION

4.1 OUTPUT VOLTAGE OF INVERTER

The Figure 11 shows the output voltage waveform without filtering. At this condition the inverter input voltage is set to 300V. Because of proposed inverter the output voltage is switched in 3voltage levels by using different switching functions. The output voltage of inverter contains harmonics. So the passive filter is connected to the output side of inverter and it removes the harmonics considerably.

The Figure 13 shows the output voltage waveform with filtering. After filtering the output voltage looks like pure sine waveform. The performance of THD is monitored by FFT analysis tool from MATLAB/SIMULINK. From the FFT analysis output voltage without filtering and with filtering is shown in Figure 12 and Figure 14 respectively. The FFT analysis shows THD of inverter output voltage of 20% before filtering and 1.74% after filtering.

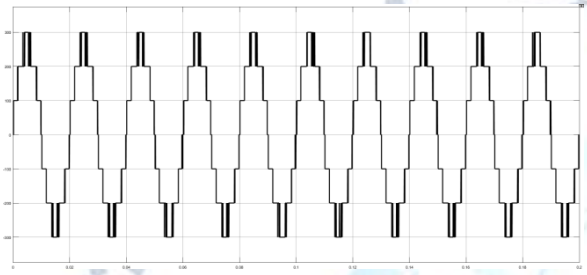


Figure 11 Output voltage waveform without filter

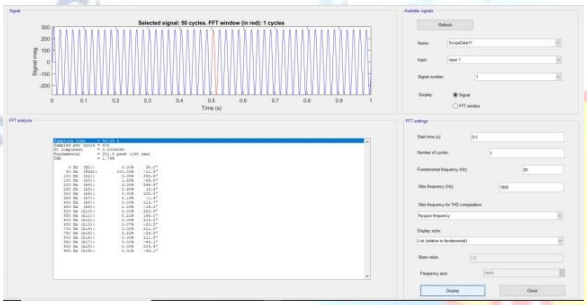


Figure 12 FFT analysis of output voltage without filtering

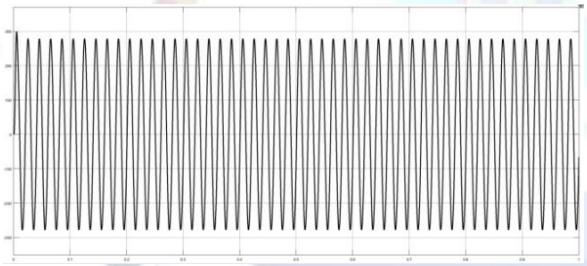


Figure 13 Output voltage waveform with filtering

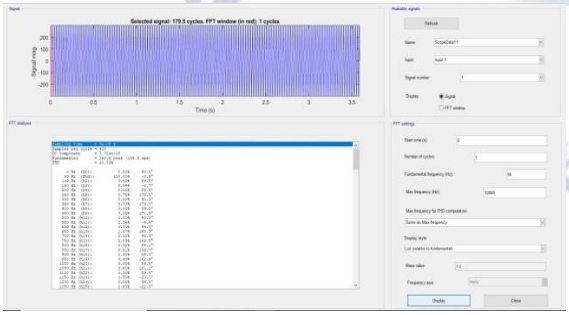


Figure 14 FFT analysis of output voltage with filtering

4.2 SWITCHING PULSES

The Figure 15 shows the multicarrier PWM technique- Phase opposition and disposition technique. By the comparison of reference signal and carrier signal the PWM signals are generated. After some processing of Phase opposition and disposition technique, the switching pulses based on Y matrix PWM for each submodule are generated as shown in Figure 16. It gives three different switching pulses separately in each submodule.

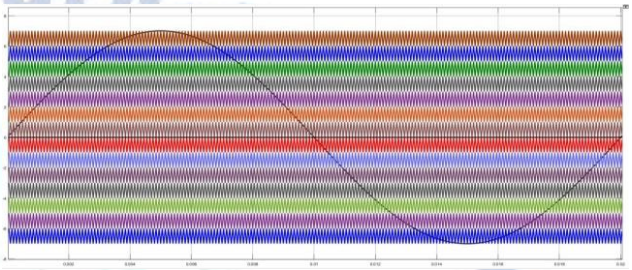


Figure 15 Multicarrier PWM: Phase opposition and disposition technique

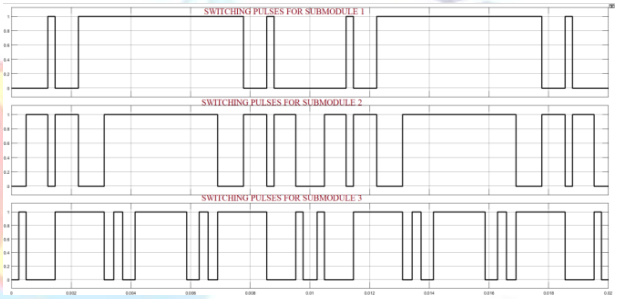
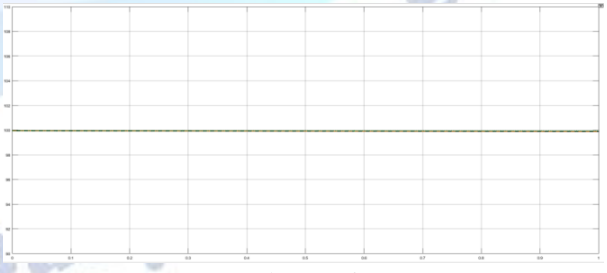


Figure 16 Switching pulses for each submodule

4.3 DC LINK CAPACITOR VOLTAGES

In sub module configuration, capacitor voltage balancing is an important task to rectify. By using Y matrix PWM technique the voltage balancing of DC link Capacitor is achieved. The figure 17 shows voltage of three sub module capacitors (C1, C2 and C3).



. **Figure 17** Capacitor voltages

4.4 OUTPUT OF PLL

The PLL helps to synchronize the inverter into grid. Single phase grid voltage is converted into αβ coordinates to find the phase angle. The αβ transformation of grid voltage is shown in Figure 18 The „α" coordinate is phase shifted by 90 degree from „β" coordinate. This will be achieved by

placing two first order filters in series with grid voltage.

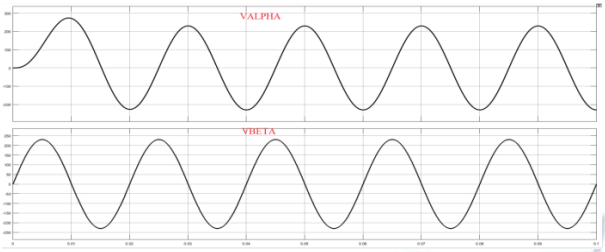


Figure 18 αβ transformation

4.5 REAL AND REACTIVE CURRENT CONTROL

The output current of inverter is controlled by current controller. The real power is controlled by coswt signal and reactive power is controlled by sinwt signal. Both signals are decided by PLL. The output of the two control signals are shown in Figure 19.

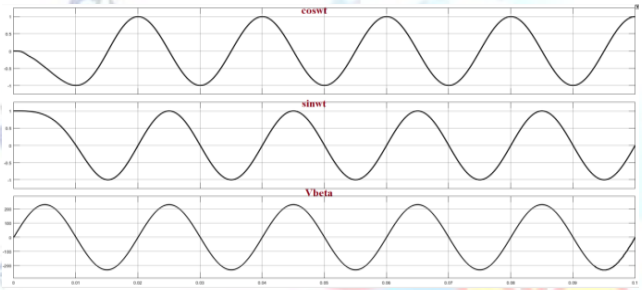


Figure 19 Real and Reactive power control

4.6 OUTPUT CURRENT OF INVERTER

The output current of inverter is shown in Figure 20. The output current is controlled by current controller used in the PLL. The preset value of current in the current controller is 10A. It generates reference voltage for PWM generation to achieve the required output current. The FFT analysis of output current is carried out to find THD of output current shown in Figure 21. From the analysis, THD of inverter output current is finding as 3.68%.

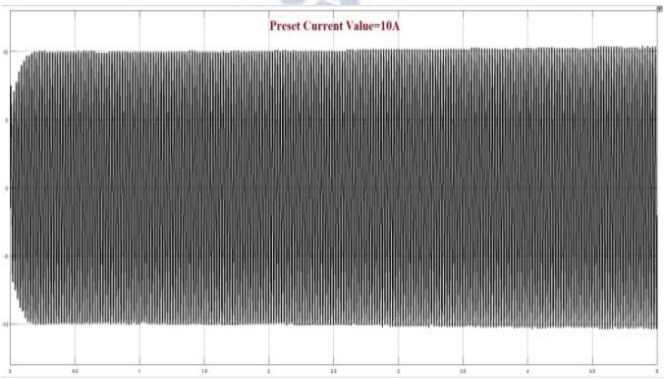


Figure 20 Output current of inverter after filter

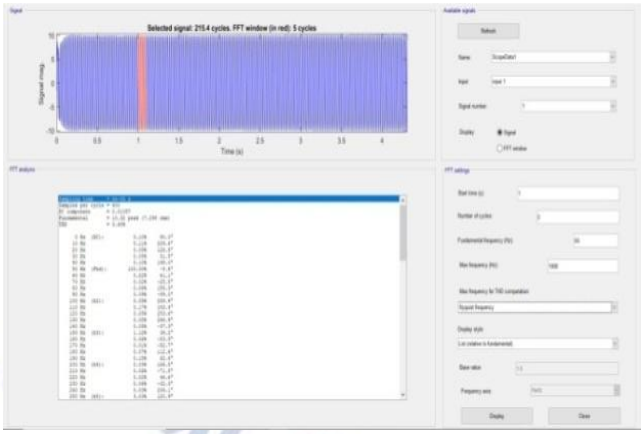


Figure 21 FFT analysis of output current

Table 2 Performance of proposed inverter

S.NO	DC INPUT VOLTAGE (V)	INPUT CURRENT (A)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	THD (%)
1	300	7.5	229	7.954	3.68
2	270	6.75	230	7.540	4.2
3	260	6.49	228	7.289	5.4
4	250	6.249	229	6.201	10.8
5	240	5.99	230	5.230	13

The Table 2 shows performance of inverter with different input voltage conditions. When the input voltage is changed, the output voltage of inverter is 230V. However the output current is changed slightly to maintain an output voltage of inverter. By using FFT analysis, the performance of THD is monitored for output current. From the results, It is observed that the THD of output current changes for different input voltages. As the LCL filter is designed for 300V voltage rating, so by reducing the input voltage it increases the harmonics in the output current.

V.CONCLUSION

The Proposed seven levels inverter has been designed and simulated with reduced no of switches and one isolated dc source. The self voltage balancing of DC link capacitor is achieved by using Y matrix PWM technique.

The inverter is connected to the grid through LCL filter and the performance of the inverter is analyzed. The PLL is used to achieve interconnection of grid and inverter. Because of current controller used in the PLL inverter injects the current into the grid. The PR controller is designed in the current controller to achieve zero steady state error quickly. The result of FFT analysis shows improvement in the performance of THD.

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