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Non Isolated High Voltage Gain DC-DC Interleaved Boost Converter

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ABSTRACT

In this paper presents the high voltage gain achieve with two phase interleaved boost converter with voltage multiplier whereas to increase the voltage gain and the mathematical expression for the voltage gain was derived and the procedure for components selection was presented. The proposed converter is simulated to convert 14 V to 430 V. The main principle of this paper is the non-isolated converter consisting of interleaved boost converters implemented by using inductors to gain high voltage.

KEYWORDS: *High voltage gain (HVG) dc-dc converter, a two- phase interleaved boost converter,and discontinuous conduction mode(DCM)*

INTRODUCTION

In now recent years increasing the usage of renewable energy sources (RES) such as solar PV, and fuel cells, has opened the field for researchers to find the best ways of applying these technologies in existing grids and other applications with more efficient ways. High-voltage-gain (HVG) dc–dc converters used to convert the low voltage levels to increased $V_{dc} = 430V$, are used in many applications. Recently, non-isolated HVG dc–dc converters have used a lot of attention due to their simplicity and have ability to provide high voltage gain with duty cycle and high efficiency. However, using classical non-isolated dc-dc converters such as boost and buck-boost converters for renewable energy applications and is not beneficial because a high voltage gain cannot be achieved in real applications. Although, efficiency reduces dramatically as duty cycle increases due to the high losses as well as high voltage stress in switches [1]-[3].

For isolated dc-dc converters, they are also not beneficial due to their discontinuous input currents, unless a filter or a large capacitor is used in the input side, which will increase cost, size, and weight [1] and [4]. Authors in [2] have explained the classification of step-up dc-dc converter topologies with a high voltage gain into cascaded boost converters, coupled-inductor type of boost converters, switched- capacitor-based boost converters, interleaved boost converters, and three-state-switching-cell-based converters. The most suitable step-up dc-dc converters for RES applications can be classified into non-isolated and isolated HVG dc–dc converters, which has been explained in [1]–[12]. While authors in [3] have focused on two-phase interleaved boost converters and they have grouped them into non-isolated converters implemented by using either inductors or coupled-inductors. coupled inductors or transformers.

The main interest of this paper is the non-isolated converter consisting of two phase interleaved boost converters implemented by using of inductors. Additionally, this paper focuses on the DCM operation and analysis of a topology of dc–dc converter with high voltage gain consisting of two input boost stages presented in [1], which has not been discussed or analyzed in the literature. This topology can be used in the DCM as a two- phase interleaved boost dc–dc converter with a single input source to draw a continuous input current, and then diode- capacitor voltage multiplier (VM) stage is used to boost the voltage to 400 *Vdc*. Moreover, reducing the overall size and weight will make this topology in the DCM more suitable for many applications, especially those that require smaller size and lower weight and some applications prefer a converter to operate in the DCM due to the advantages of the DCM presented in [12]. Eventually, the same topology in the DCM with two input sources can be used in applications that do not require a continuous input current.

This paper is organized as follows: section II presents converter operating modes and topology. Section III analyzes and derives the voltage gain based on the volt–second balance of the inductors. Section IV concludes the paper.

CONVERTER TOPOLOGY

The high voltage gain (HVG) dc-dc converter topology is composed in two phase boost stages with single input source and voltage multiplier is used to improve the voltage gain as depicted in Fig. 1, where V_{in} is the input voltage, L_1 and L_2 are the power inductors, S_1 and S_2 are the power *MOSFETs* with reverse-paralleled diodes, D_1 to D_4 are the power diodes, C_1 to C_4 are the power capacitors, and R is the output resistor.

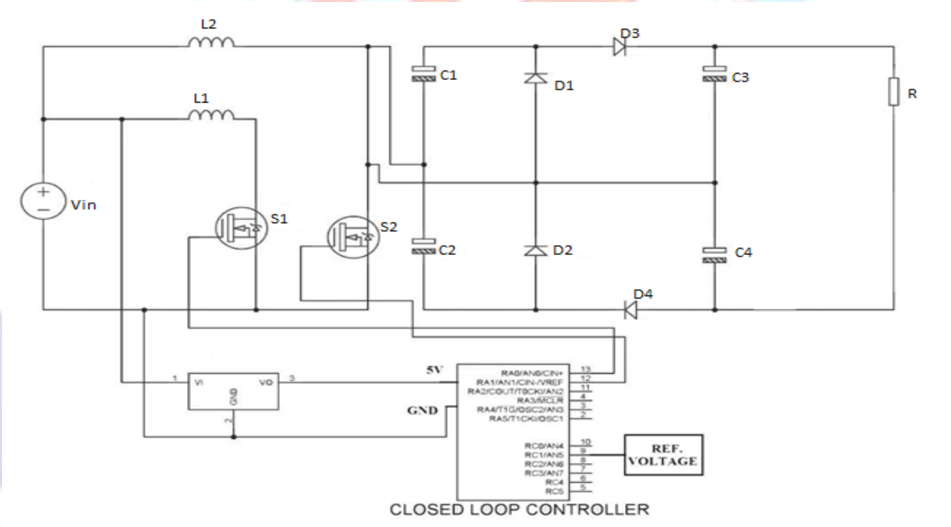

Fig. 1. High voltage gain dc-dc converter with single input source and VM stage.

A. MODE 1

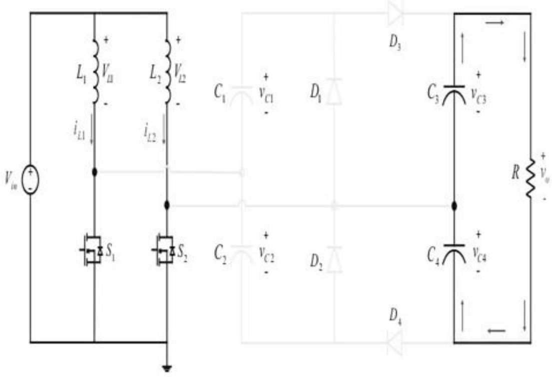

Fig. 2. Equivalent circuit of Mode 1

In this interval, both switches (S_1 and S_2) are ON; the two inductors are charging and voltage across these two inductors are equal to V_{in}. Moreover, all VM diodes are reverse-biased (OFF) and there is no change in the capacitor C_1 and C_2, as shown in Fig. 2. Therefore, the load is supplied by both capacitor C_3 and C_4.

B. MODE 2

In this mode, switch S_1 is OFF and S_2 is ON; subsequently, the inductor L_1 is discharging all of its energy in this mode, while the inductor L_2 is still in the charging mode and the voltage across L_2 is equal to V_{in}. Moreover, both diodes D_1 and D_4 are reverse-biased (OFF), while the diodes D_2 and D_3 are forward-biased (ON). Hence, the capacitor C_1 is discharging, while capacitor C_2 is charging, as shown in Fig. 4. Lastly, the load is supplied by a part of the diode D_3 current (i_{D3}) and the remaining of this current (i_{D3}) is charging the capacitor C_3, while the capacitor C_4 is still in the discharging mode.

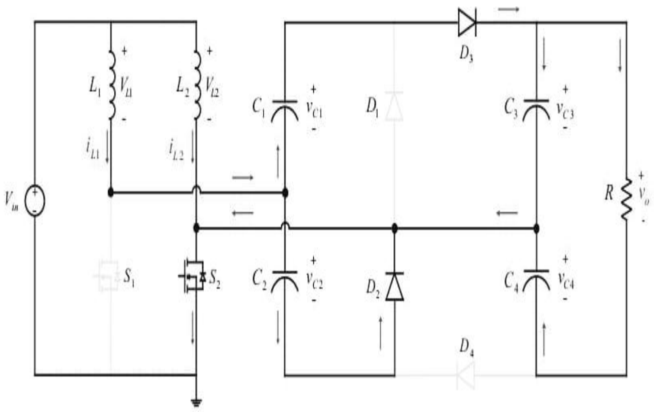

Fig. 3. Equivalent circuit of Mode 2

C. MODE 3

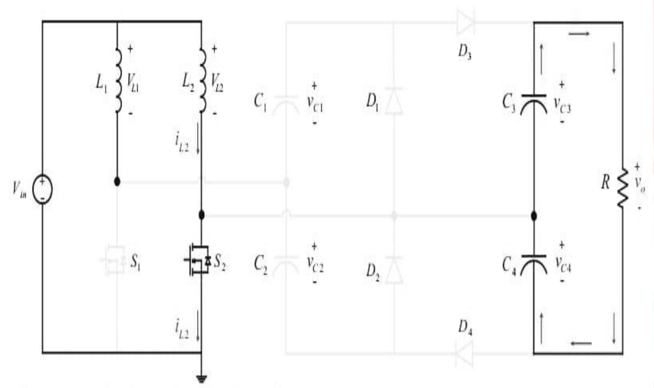

Fig. 4. Equivalent circuit of Mode 3

In this mode, the switching signals are the same as in Mode 2 (S_1: OFF and S_2: ON). For L_1, no energy is released in this mode; thus, current and voltage of the L_1 is zero. The inductor L_2 is still in the charging mode as in Mode 2 and the voltage across it is equal to V_{in}. Moreover, all diodes are reverse-biased (OFF), and there is no change in capacitor C_1 or C_2, as shown in Fig. 4. Therefore, the load is supplied by both capacitor C_3 and C_4 as in Mode 1.

D. MODE 4

This mode is same as in mode1, Both switches (S_1 and S_2) are ON; and the two inductors are charging and voltage across these two inductors are equal to $V_{in.}$ VM diodes are reverse-biased (OFF) and there is no change in the capacitor C_1 and C_2 as shown in fig 2, and the load is supplied by both capacitor C_3 and C_4.

E. MODE 5

In this subinterval, the switch S_1 is ON and S_2 is OFF; thus, the inductor L_1 is charging and the voltage across it is equal to V_{in}, while the inductor L_2 is discharging all of its energy in this mode. Additionally, both diodes D_2 and D_3 are reverse biased (OFF), as described fig 5. As a result of this capacitor C_1 is charging while capacitor C_2 is discharging, the capacitor C_4 is charging and the load is supplied by the capacitor $C_{3.}$

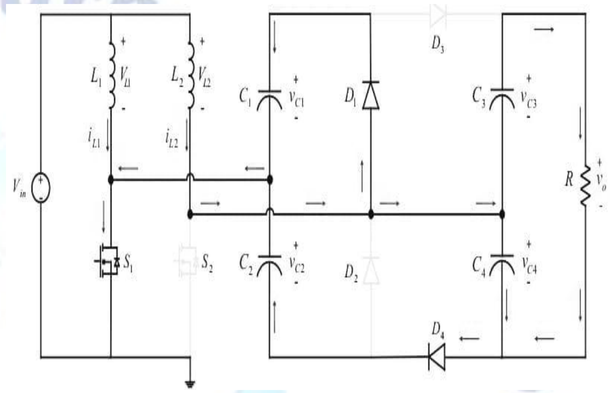

Fig. 5. Equivalent circuit of Mode 5

F. MODE 6

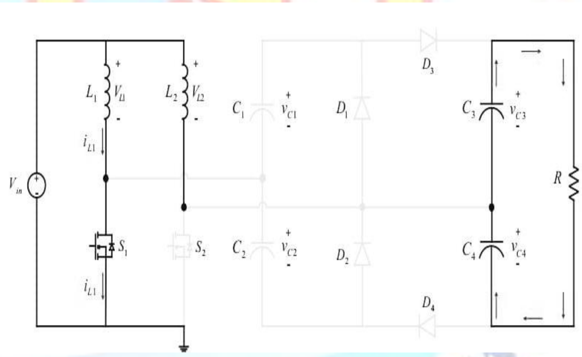

Fig. 6. Equivalent circuit of Mode 6

In this mode the switching signals are same as in mode 5 (S1: ON and S2: OFF). Thus, the inductor L1 is still in the charging mode as in Mode 5 and the voltage across it is equal to Vin while no energy is released by L2; subsequently, current and voltage of L1 is zero. Moreover, all diodes are reverse- biased (OFF), and there is no change in capacitor C1 or C2, as shown in Fig. 7. Therefore, the load is supplied by both capacitor C3 and C4 as in Mode 1, 3 and 4.

VOLTAGE GAIN OF THE CONVERTER

The volt-sec balance of the both inductors can be used to derive the voltage gain of the topology.

Therefore the average voltage across the inductor L_1 is,

$$V_{C2} = V_{C3} - V_{C1} = V_O - V_{C4} - V_{C1} = V_{in}\left(\frac{d_1+d_3}{d_3}\right) \qquad (1)$$

The average voltage across the inductor L_2 is,

$$V_{C1} = V_{C4} - V_{C2} = V_O - V_{C2} - V_{C3} = V_{in}\left(\frac{d_2+d_4}{d_4}\right) \qquad (2)$$

From (1) and (2), the capacitor voltages for the proposed converter are given as follows:

$$V_{c1} = V_{in}\left(\frac{d_2+d_4}{d_4}\right) \text{ and } V_{C2} = V_{in}\left(\frac{d_1+d_3}{d_3}\right), \qquad (3)$$

$$V_{C3} = V_{in}\left(\frac{d_1+d_3}{d_3}\right) + V_{in}\left(\frac{d_2+d_4}{d_4}\right), \qquad (4)$$

$$V_{C4} = V_{in}\left(\frac{d_1+d_3}{d_3}\right) + V_{in}\left(\frac{d_2+d_4}{d_4}\right) \qquad (5)$$

Accordingly, the voltage gain in terms of d_3 andd_4 can be found as

$$V_o = 2V_{in}\left(\frac{d_1+d_3}{d_3}\right) + 2V_{in}\left(\frac{d_2+d_4}{d_4}\right). \qquad (6)$$

Also, d_3 and d_4 can be computed as

$$d_3 = \left(\frac{4L_1 f}{V_{in} d_1}\right) I_o \text{ and } d_4 = \left(\frac{4L_2 f}{V_{in} d_2}\right) I_o. \qquad (7)$$

Substituting the previous expressions for d_3 and d_4 into equation 6 and solving for $\frac{V_o}{V_{in}}$ results in the general equation of the voltage gain:

$$\frac{V_o}{V_{in}} = \sqrt{\left(\left(\frac{d_1^2 R}{2fL_1}\right) + \left(\frac{d_2^2 R}{2fL_2}\right) + 4\right)} + 2 \qquad (8)$$

By assuming $L_1 = L_2 = L$, and $d_1 = d_2 = d$, then

$$\frac{V_o}{V_{in}} = \sqrt{\left(\frac{d^2 R}{fL} + 4\right)} + 2 \qquad (9)$$

SIMULATION EXPERIMENTAL PARAMETERS

In the simulation, MATLAB is used to validate the operation of this topology in the converter. Simulation modeling is the process to create and analyzing a digital prototype of physical model to predict its performance in the real time, The simulation modeling used to help designing methods and helps to find which ways a part could fail and what loads it can withstand. The input voltage, 22 µH for both inductors, 50 kHz for switching frequency has been chosen to achieve 430V output voltage. After executing the simulation, the average current and voltage are 1.2 A and 430V respectively. The simulation parameters used in the proposed system with its specifications, input range output range are represented in the following table. 1.

Table 1

PARAMETERS	VALUE
Input voltage	14v
Switching frequency	50kHz
Inductor L_1, L_2	22µH
Capacitor C_1, C_2	47µF
Capacitor C_3, C_4	150µF

SIMULATED INTERLEAVED BOOST CONVERTER

The simulink model for interleaved boost converter with voltage multiplier cells is shown figure. 7. The input voltage s given to the switches with two phase interleaved boost converter and the voltage multiplier is increased the voltage level to high. Voltage multiplier circuit implemented with the quadrupler method to used to gain high voltage with capacitors and diodes with two phase interleaved converter

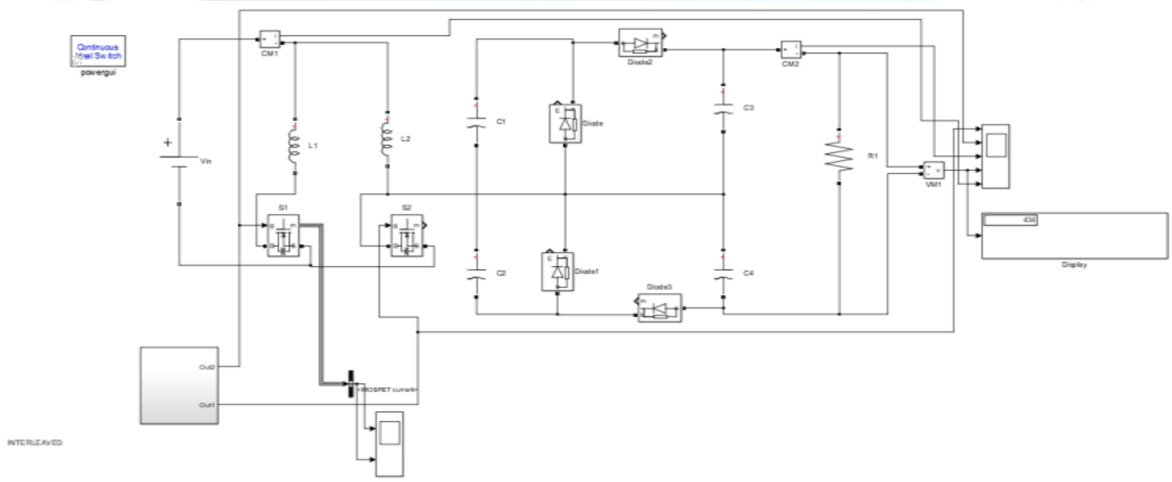

Fig. 7. Simulation of interleaved boost converter with Voltage multiplier cell

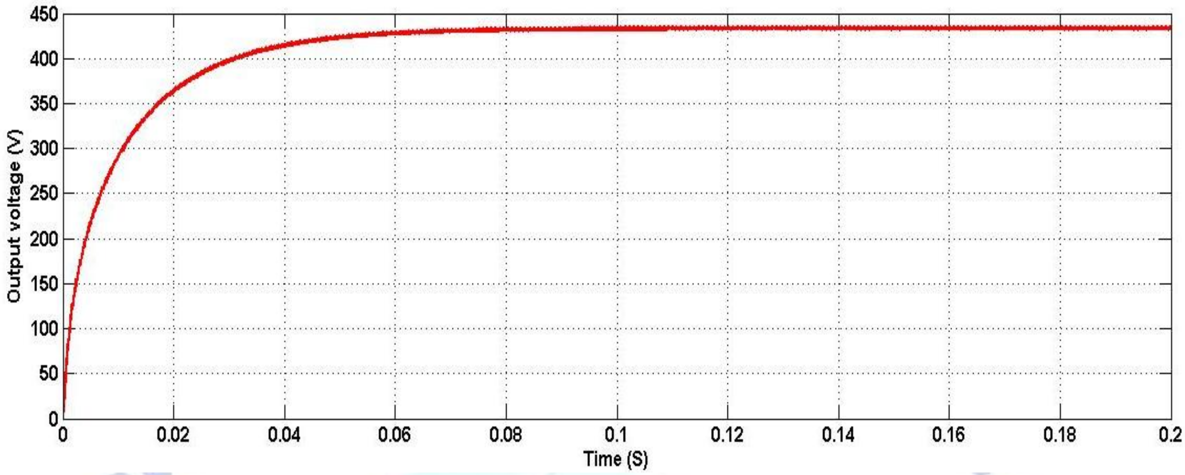

Fig. 8. Simulation results for output voltage

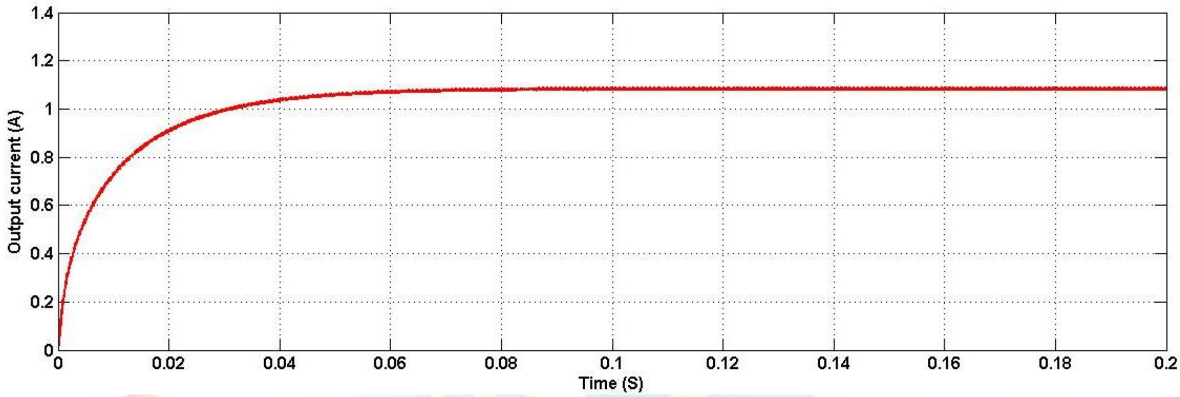

Fig. 9. Simulation waveform for current

In fig.7 The simulation Results are shown for two phase interleaved boost converter with increased voltage gain.

Output voltage

The simulated output voltage is represented in the fig.8, The input DC source voltage fed, after simulating it will provide the output value which will be boosted while comparing the input value of voltage. Here we applied to 14V input voltage, the resulted output value is obtained as 430V.

CONCLUSION

The interleaved boost converter is presented in this paper with highly improved voltage with simulated output results. The voltage gain mathematical derivations are derived and the simulation results are shown. The analysis and the design were verified by the simulation results. The salient features such as the high voltage gain, continuity of input current, and low voltage stress on the components, it can be concluded that this topology in the DCM is used to many applications such as solar PV and fuel cell applications.

REFERENCES

[1] Alzahrani, Ahmad, Pourya Shamsi, and Mehdi Ferdowsi, "A novel interleaved Non-isolated High-gain DC-DC Boost Converter with Greinacher Voltage Multiplier Cells," Renewable Energy Research and Applications (ICRERA), 2017 IEEE 6th International Conference, pp. 222-227. IEEE, 2017.

[2] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter," IET Power Electronics, vol. 8, no. 10, pp. 2044-2057, 10 2015.

[3] M. Nguyen, T. Duong and Y. Lim, "Switched-Capacitor-Based DualSwitch High-Boost DC–DC Converter," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 4181-4189, May 2018.

[4] B. P. R. Baddipadiga, V. A. K. Prabhala, and M. Ferdowsi, "A Family of High-Voltage-Gain DC-DC Converters Based on a Generalized Structure," IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8399– 8411, 2018.
[5] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC-DC Converter with High Voltage Gain and Two Input Boost Stages," IEEE Trans. Power Electron., vol. 31, no. 6, pp. 4206–4215, 2016.
[6] Alzahrani, Ahmad, Pourya Shamsi, and Mehdi Ferdowsi, "A novel Non-isolated High-gain DC-DC Boost Converter," Power Symposium (NAPS), 2017 North American, pp. 1-6. IEEE, 2017.
[7] F. Yang, X. Ruan, G. Wu, and Z. Ye, "Discontinuous-Current Mode Operation of a Two-phase Interleaved Boost DC-DC Converter with Coupled Inductor," IEEE Trans. Power Electron., vol. 33, no. 1, pp. 188–198, 2018
[8] B. C. Barry, J. G. Hayes, M. S. Ryłko and J. W. Masłoń, "Discontinuous Conduction Mode Operation of the Two-phase Integrated-magnetic Boost Converter," IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5782-5789, 2014.
[9] B. C. Barry et al., "Small-signal Model of the Two-phase Interleaved Coupled-onductor Boost Converter," IEEE Trans. Power Electron., vol. 33, no. 9, pp. 8052–8064, 2018.
[10] F. Yang, X. Ruan, G. Wu, and Z. Ye, "Discontinuous-Current Mode Operation of a Two-phase Interleaved Boost DC-DC Converter with Coupled Inductor," IEEE Trans. Power Electron., vol. 33, no. 1, pp. 188–198, 2018.
[11] B. P. Baddipadiga and M. Ferdowsi, "A High-Voltage-Gain DC-DC Converter Based on Modified Dickson Charge Pump Voltage Multiplier," IEEE Trans. Power Electron., vol. 32, no. 10, pp. 7707– 7715, 2017
[12] M. Ferdowsi and A. Emadi, "A New Estimative Current Mode Control Technique for DC-DC Converters Operating in Discontinuous Conduction Mode," IEEE Power Electron. Lett., vol. 2, no. 1, pp. 20–23, 2014.