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Design and Implementation of FSM Based MBIST using March Algorithm

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ABSTRACT

The research article aims at identifying memory testing in static random access memory which is significant in deep sub micron era. Built in self test provides a best solution replacing the external Automatic test equipment. Built in Self Test is a technique of designing additional hardware and software feature into Integrated circuits to allow them to perform testing. BIST works in the background checking memories for faults without interfering with actual functionality of the memory. The objective of the proposed work is to identify faults associated with the memory, perform test algorithms to detect the faults in memory BIST architecture.The implementation of Memory BIST is done using Finite state machine model. The design of memory BIST is accomplished using Xilinx Vivado IDE for 32X8 memory.

KEYWORDS: *BIST, ATE, memory testing, March Algorithms.*

I. INTRODUCTION

The memory architecture is usually 2D array. The regular structure of the memory structure makes testing process quite easy compared to combinational logic circuit and sequential circuit. The memory testing is slightly different yet interesting process. The defect associated with memory is developed during the process of manufacturing. The defects thus developed are very large in number, varient and need to test the memories before marketing the memories inside the system to ensure correct functioning of memories. Memories SRAM, DRAM,ROM are regular structure with testing strategies slightly different but the approach is same using classical algorithms and non classical algorithms like march algorithms[1]. In VLSI the integrated chips reduce in size drastically. Testing in the VLSI field involves both the design stage, verificationstage,in order to ascertain test and design issues at the early stage in the design and testing engineer in production test stage. It would be appropriate to develop test strategy at the early stage in the product development process that may include the addition of any additional test circuitry. The production test stage implements the test during the high volume production of the product and is to make cost effective to reduce the overall device cost. DFT is used to reduce the test generation cost, generation costs, enhance the quality and hence reduce defect level(physical faults) and for memories it is a necessity as the yield in memories after manufacture is least 1 to 5%[6].For testing the comparison is carried out on the tester. Although the Automatic Test Equipment(ATE) based test methodology has been dominant in the past, as transistor to pin ratio and circuit operating frequencies continue to increase, there is a growing gap between the ATE capabilities and circuit test. Conventional DFT methods do not provide a

complete solution to the requirement of testing memory faults and its self-repair capabilities. The challenge is to test memories from the system level as it requires test logic to multiplex and route memory pins to external pins[2]. To test the memories functionally through ATPG (Automatic Test Pattern Generation) requires very large external pattern sets for acceptable test coverage due to the size and density of the cell array and its associated faults[3].ATE limitations make BIST technology an attractive alternative to external test for complex chips. BIST is a design-for-test (DFT) method where part of the circuit is used to test the circuit itself (i.e., test vectors are generated and test responses are analyzed on-chip at the chip level.The growing gap between the ATE capabilities and circuit test requirements especially in terms of speed, pin count and volume of test data. Only prohibitive amount of test vectors can be stored in ATE memory, the degree of controllability and observability of the the circuit depends on the tests generated randomly or deterministically which involves lot of test vector calculation efforts. The pin count availability is always a problem[4] . BIST needs only an inexpensive tester to initialize BIST circuitry and inspect the final results (pass/fail and status bits). However, BIST introduces extra logic, which may induce excessive power in the test mode, in addition to potential performance penalty and area overhead.

II. DESIGN OF MBIST USING XILINX VIVADO

Test pattern generation for memories should definitely be deterministic or pseudo random.The behavioral model is totally based on the system specification and is highest level of abstraction. The behavioral model is realized by algorithmic approach which ensures the intended test Pattern for a fault model[7] .The SRAM cell with defect considered is shown in Fig.1.

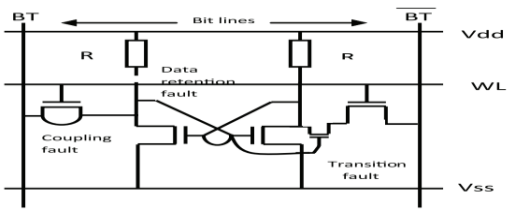

Fig. 1 SRAM with defect

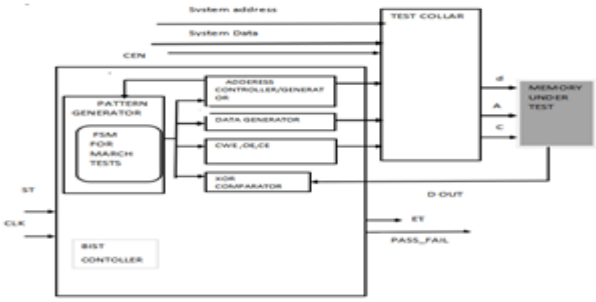

Fig. 2 Memory BIST architecture

As shown in Fig.2 Test pattern generation [TPG] is a method used to find an input (or test) sequence that , when applied to a digital circuit, enables automatic test equipment to distinguish between the correct and the and the faulty circuit behavior caused by defects.So, TPG process of generating patterns are deterministic by algorithm or pseudo-random by LFSR which generated all the test but in random order. The generated patterns are used to test semiconductor devices after Manufacture, or to assist with determining the cause of the failure. The effectiveness of TPG is measured in the number of fault models, detectable and by the number of generated patterns.The TPG should generally include fault coverage and test application time.A fault model is the mathematical description of how the defect alters design behaviour. The logic values observed at design primary outputs, while applying test patterns to some device under test (DUT), are called the output of the test patterns. The output of the testing pattern when testing with a fault -free device that works exactly as designed, is called the expected output of the test pattern. A fault is said to be detected by the test pattern, if the output of the test pattern, when testing has one fault, is different than the expected output. The TPG process for a targeted fault consists of two phases: fault activation and fault propagation. Fault activation establishes a signal value at the fault model. Fault propagation moves the resulting signal value, or fault effect, forward by sensitizing a path from the fault site to a primary output.TPG can fail to find a test for particular fault in at least two cases. First the fault may be undetectable, such that no pattern exist that can detect the particular fault.

III. IMPLEMENTATION DETAILS OF THE MEMORY BIST

The TPG methodology in the proposed model is algorithmic test sequence that is each address is accessed only four times write 0,write 1, read 0, and read 1. unlike any methodology

psuedo-random testing, exhaustive testing (all 2*n possibilities of n bit address)where number of tests are 2*n and memory is accessed 2*n times. This algorithmic sequence is the march sequence. March algorithm is a simple combination of March elements (r0, w1).A read operation infers the same Memory back ground data used in the last operation. Similarly, a write operation infers the reversed background data used in the last operation. For implementing March C, four March elements are needed(w), (r, w), (r). The total number of March elements for the most practical March algorithms is less than ten.

Isolation circuit is the interface between the BIST controller and the memory under test. It separates the two inputs to the memory; the two inputs test inputs and the normal inputs. Based on the BIST controller test enable isolation circuit works if the BIST test enable input is 0 , the normal inputs are given to the memory ,it is in normal mode, and if the BIST test enable input is 1 , the BIST inputs are given to the memory, it denotes that memory is in the test mode. A multiplexer is used for isolation circuit. BIST is an automated testing that enables high speed testing and high fault coverage. BIST controller top module is used to coordinate operations of the different blocks of the BIST. The multiplexer block is shown in Fig.3.Based on the test mode input test-enable pin to the controller and the isolator, the system either operates in the normal mode or test mode.

Steps followed for implementation

- The RTL of the BIST controller allows us to suspend the data sequence generation at any desired point according to the march test algorithm in the test sequence.
- The BIST controller coordinatestheaddress generation also.
- The Output response analyzer(ORA) ORA is preferably placed inside the BIST controller block so that testing of an external memory happens with the inbuilt ORA avoiding generation of other ORA for the testing of faults. This controls the signal between all the blocks and is the heart of the MBIST. This gives the control signals to the memory which is under the test and controls the ORA and other blocks in the circuit. The module implemented is shown in Fig.4.

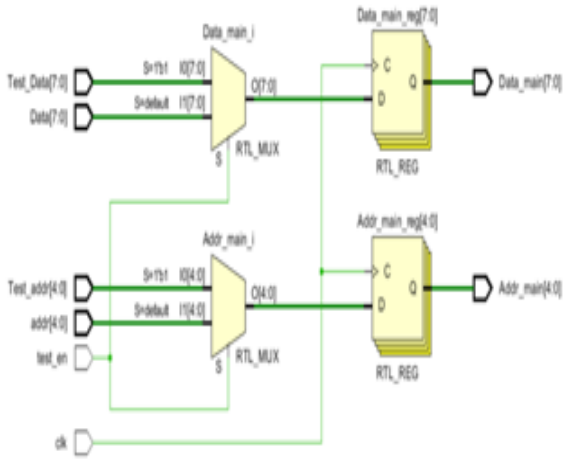

Fig. 3 Multiplexer block in the BIST architecture

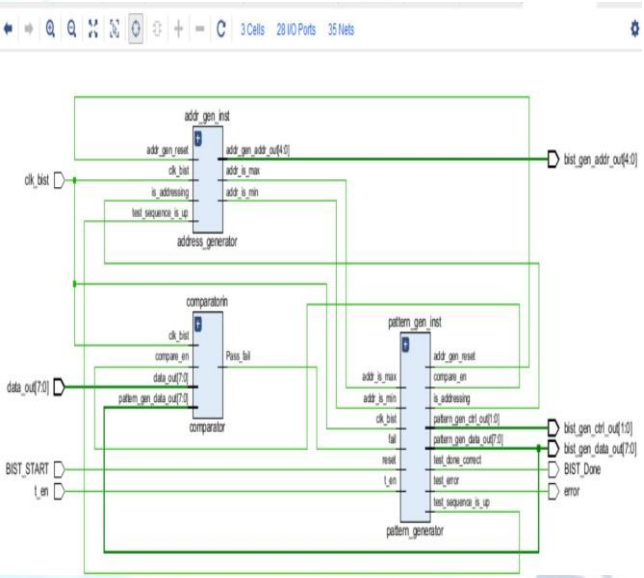

Fig. 4 The implemented BIST structure

IV. RESULTS

The address controller/generator is designed and the simulated. The inputs to the address generator are a addr_reset, addressing direction, addressing mode.

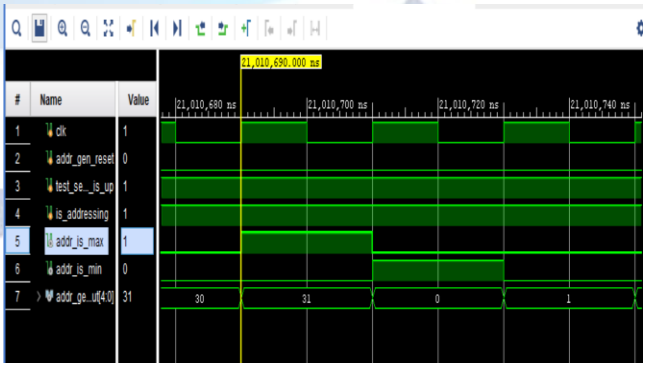

Fig.5. The input signals for Proposed BIST

The MARCH C- implementation using the BIST block is shown in Fig.5.The bist address ,bist data,bist control write enable and read enable are

obtained. The test_en is the trigger for testing the memory for fault temporarily stopping normal system functioning of storing data in the memory.

The Wire_fail shows the faulty behaviour and also gives fault location simultaneously but test_error is used to detect that fault is present in the memory.The output generated is shown in Fig.6.

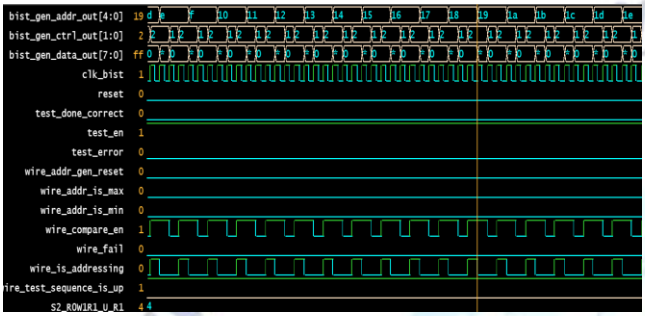

Fig.6 Output generated

The Output response analyzer is one of the main component of BIST to determine a fault has occurred.The response of the ORA analyzer block is shown in Fig.7.

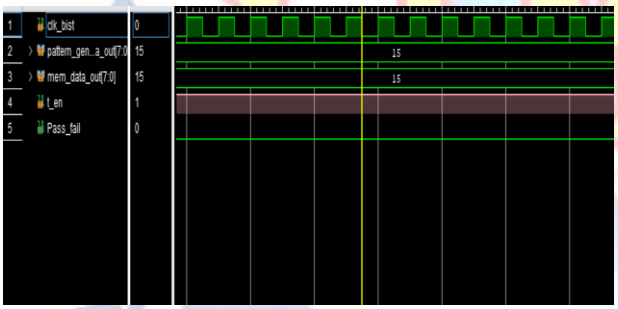

Fig.6. Response of the ORA analyzer

The final implementation is shown in Fig.7. of the BIST operation is checked on memory with varied stimulus like a psuedo-random LFSR for data and address both to check the correctness of the whole hardware

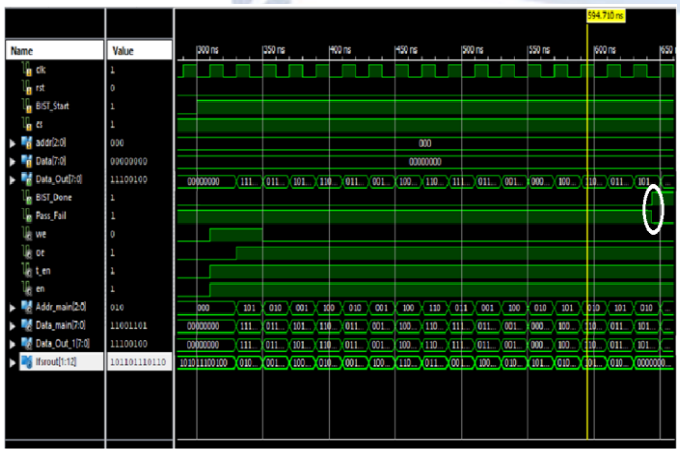

Fig.7. Testing of March-C Algorithm

IV. CONCLUSION

Proposed Memory BIST (MBIST) is implemented for testing static random access memories (RAM). March C- algorithm is compared with other March algorithms MATS+ and proved it has advantages over other March algorithms in terms of fault coverage and it also tests all possible faults associated with memories. The utilization of MBIST is shown in the Xilinx Vivado design suite which is comparably less compared to the memory utilization.

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