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Design of Low Power & Area Efficient of 8-Bit Comparator using GDI Technique

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ABSTRACT

In this paper we are design a circuit based on data selector and distributor networks in which we will not realize the circuit based upon the expressions but off course the circuit which have designed will have internally some expression. In the recent trends the need for low power and less on-chip area is on high note for the portable devices. In this project we want to focus on the design constraints of VLSI. Innovative design of 8-Bit GDI based Comparator will be proposed and implemented. Optimization depends on selection of GDI Cell as well as selection of primary inputs to the terminals of GDI cell. 8-Bit GDI based Comparator will be designed and simulated using Tanner EDATool. Comparator has three main outputs where it can compare the weight of two words and generates three functions. GDI has the advantage of low power consumption because the total number of logic devices needed willbe less and it can also operate with high speed due to affective realization of logic using minimal hardware. Comparator circuits is designed using tanner tools and also observe the simulation results in H-SPICE attaining low power and less delay.

KEYWORDS: *GDI-Gate Diffusion Input, H-SPICE, Data selector, Tanner EDA*

I. INTRODUCTION

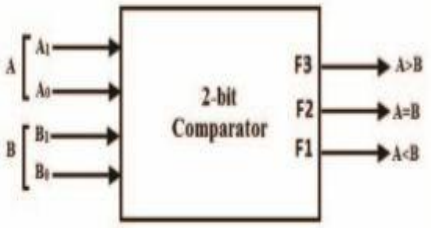
In today's world innovative technology turns out to be more exceptional and available across the globe.Various Semiconductor engineers and VLSI designers have been exploring and executing Modified GDI Technique for different technical applications. In our project, we have presented the concept of a comparator using Modified GDI technique which can be used for various digital applications. It will not only end up on this application but also can be applied to many digital circuits for optimized VLSI constraints.

The main objective of this project is to provide better optimization of an 8bit comparator Designing a high speed and low cost circuit given, a low area and low power consuming circuit. Through the implementation of a 2bit and 8bit comparator designs, the area constraint and power consumption are largelyoptimized circuit design using the Modified GDI technique, so it can have suitable VLSI constraints.

II. LITERATURE SURVEY

Data comparison is needed in digital systems while performing arithmetic or logical operations. This comparison determines whether one number is greater than, equal, or less than the other number. A digital comparator is widely used in combinational system and is specially designed to compare the relative magnitudes of binary numbers. Whenever we want to compare the two

binary numbers, first we have to compare the most significant bits. A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers (consider A andB) and determines their relative magnitudes in order to find out whether one number isequal, less than or greater than the other digital number. Three binary variables are usedto indicate the outcome of the comparison as A>B, A<B, or A=B. These comparators can compare 2-bit, 4-bit and 8-bit numbers depending on the applicationrequirement.



F1 = A1' B1+ A0' B0 (A1 B1 + AB1)

F2 = (A1'B1' + A1 B1) (A0' B0' + A0 B0)

F3 = A1 B1' + A0 B0' (A1' B1'+ A1 B1)

Modified GDI technique is a very power efficient method compared to theCMOS and normal GDI technologies. Using the modified GDI technique, the number of transistors widely reduced which eventually helps in low power consumption. The power delay product is calculated and reduced.

III. EXISTING METHOD

The project takes on the designing of 2bit comparator and 8bit comparator. The existing designs for 2bit design. TheLogic Function of the Magnitude Comparator can be acknowledged customarily utilizing 66 Transistors as appeared in Fig below.

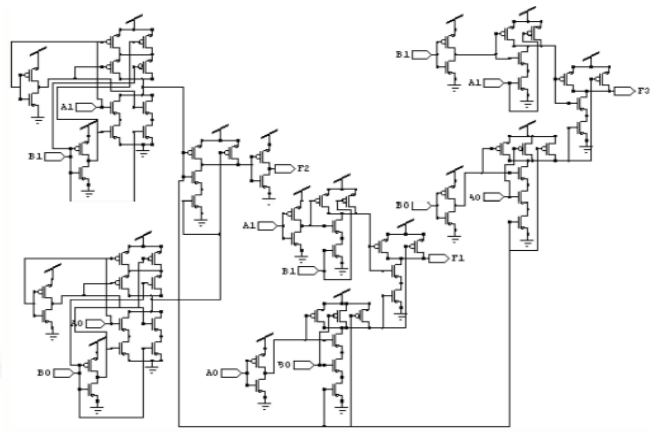


Figure 1: CMOS 2-bit Magnitude Comparator

As itutilizes more number of transistors it involves more territory and more will be the PowerDissemination.

Existing 2 bit GDI magnitude comparator using 30 transistors is based on full adder. When compared with other logic styles implemented using CMOS, transmission gates and NMOS pass transistor GDI is found to be advantageous with high performance or speed, low power consumption and low silicon chip area.

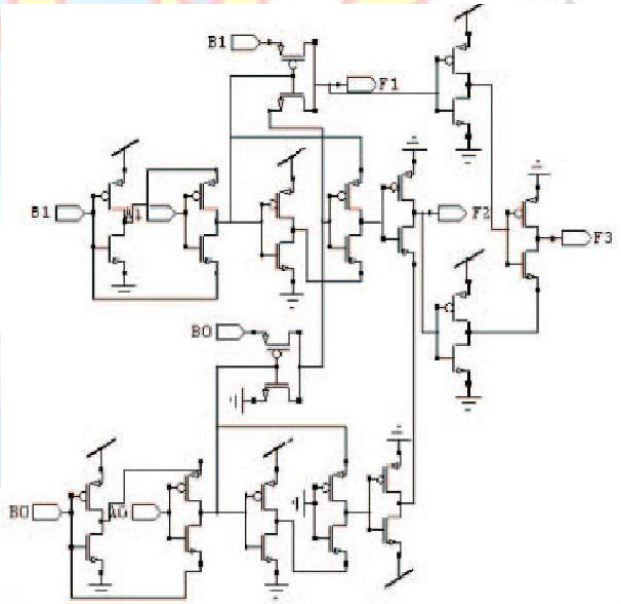


Figure 2: GDI 2-bit Magnitude Comparator

IV. PROPOSED DESIGN

We have designed a modified circuit compared to the existing circuit. The proposed design is based on modified GDItechnique, which is an extension of the normal GDI technology. In the modified GDI technique, the PMOS gate terminal is connected to the sourceand NMOS gate is connected to ground. The design of modified GDI cell enables the

connection ofany input to the G, P, N terminals without any restrictions..The 2bit design is based on multiplexer whichis similar to a GDI cell. The 8bit design is done in blocks. Every block is designed using GDI technique. The design is done as branches for A>B &A<B. The outputs of A>B and A<B logics are gives to a GDI based NOR gate which gives the A=Blogic.

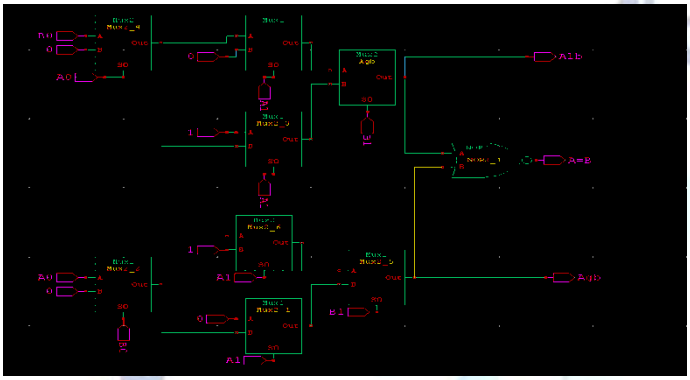


Figure 3: 2-Bit Design of Proposed Model

The design schematic of proposed 8bit comparator is as below:

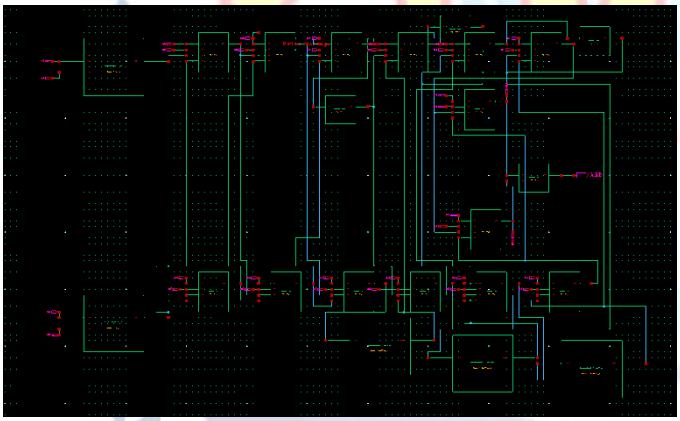


Figure 4: 8-Bit Design of Proposed Model

The 8bit design uses 116 transistors. In the 8bitdesign, the branching is similar to 2 bit design. In this, there are blocks that are divided into stages where in the each block is supplied with previous stage output and gives a carry forward logic. Each block is designed inGDI model and the theNOR gate is also designed in GDItechnique.

V. SIMULATION RESULTS

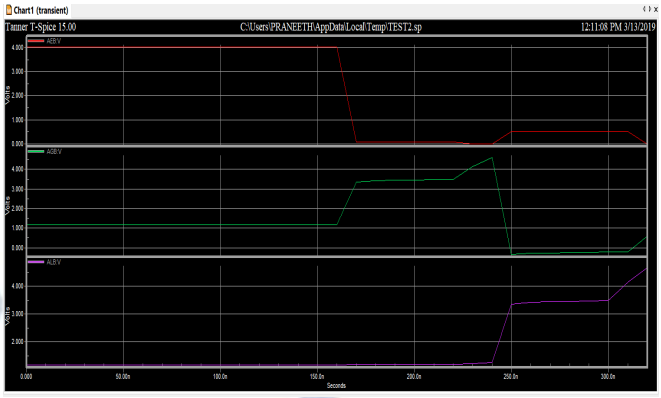


Figure 5: Output waveform for Comparator

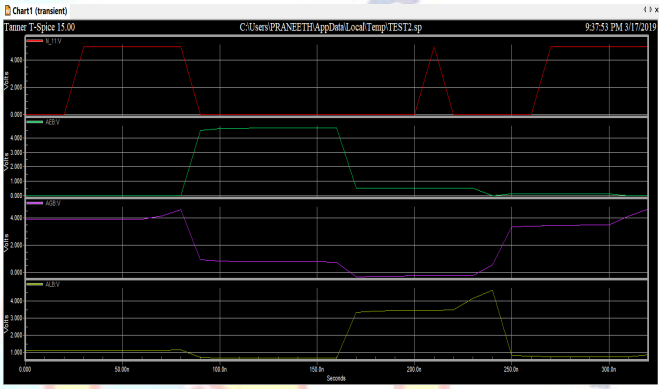


Figure 6: Output waveform for Delay

VI. CONCLUSION AND FUTURE DEVELOPMENT

Proposed design has been optimized with respect to the design constraints of VLSI.Theexecution of the proposed Modified GDI size comparator circuit with help of full viper rationale has appeared great execution in contrast with existing regular CMOS based outline. The near execution of regular CMOS and proposed Modified GDI greatness comparator with deference to control utilization at various scope of info voltage, temperature and recurrence has been talked about in above area. The littler territory of proposed GDI extent comparator comes about into shorter interconnects and therefore less crosstalk. Empower more proficient arrangement and steering. Along these lines, it is inferred that proposed extent comparator in view of Modified GDIstrategy require less power and littler region in correlation with CMOS greatness comparator. Subsequently, this new configuration isgreat choice for low powerproficient framework outline. There is a reduction ofnumberof transistors in the proposed design taking the count to 116 transistors.

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