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Reduced Switch Multilevel Inverter based STATCOM

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ABSTRACT

This paper presents an application of reduced switch multilevel inverter topology to STACOM. This topology consists of basic unit in which two switches are connected in series and one H-bridge unit. Multilevel inverter is beneficial in terms of reliability and improved output quality. Multilevel inverter have only drawback of higher number of switches. This reduced switch topology has less number of switches as compared to conventional Cascaded H Bridge Inverter. Compared to direct control method, indirect control method is simple but due to fast response and precise control, direct current control method is quite effective. In this work STACOM is implemented to improve the Power factor of the power system. An extensive digital simulation of the recommended STATCOM and its controller is carried out using MATLAB/SIMULINK software to study system performance. Simulation results prove that using Direct current control technique overall power factor is improved.

KEYWORDS: *Multilevel inverter; Reduction of switches; STATCOM; PWM Technique*

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I. Introduction

Depending on the output voltage levels inverters are generally classified as two level inverter and multilevel inverter. Multilevel inverter has an ability to produce high voltage, better harmonic performance, lower semiconductor voltage stress, low electromagnetic interference and lower switching losses hence multilevel inverter gaining more popularity in many high power applications [1-2]. Regardless of these advantages, multilevel inverters output voltage amplitude is limited to DC sources voltage summation. An intermediate DC to DC converter is required for the boost or buck operation of inverter output voltage [3].

The primary difficulty in multilevel inverter is in terms of increased switches which are requiring for practical application to reduce cost and losses across the switches [4-5]. In this work the primary objective is to investigate the multilevel inverter topology with reduced number of switches.

Power quality is the main concern now a day due to recent development in the industrial load. To deal with the power quality issues there is an evolution of FACTS devices. STATCOM is one of central device among the various FACTS devices which are used for harmonic mitigation and reactive power compensation of the system. [7-8] explains the basic operating principle of Static Synchronous Compensator (STATCOM).

There are number of control strategies introduced by researchers in order to detect the harmonic content and reactive power of the power system. [9] Investigates the direct current control method applied to distribution STATCOM. In general there are two methods, Direct current control method and indirect current control method for the operation of STATCOM which is discussed in [10]. Out of these two, direct current control method is fast and precise. Control system for PWM based STATCOM is explored in [11], where author explains the necessity of capacitor voltage control.

This paper presents application of reduced switch inverter for power factor improvement of overall system using STATCOM and its control based on direct current control method. The results are verified by simulating the system using MATLAB/SIMULINK software.

II. PROPOSED SYSTEM

STATCOM is a device which absorbs or generates reactive power from the system to provide voltage support without using large reactor or capacitor bank. This paper presents reduced switch inverter based STATCOM for power factor Improvement.

A. *Reduced switch cascaded Inverter*

Reduced switch inverter cascaded basic unit comprises of 6 switches as shown in Fig. 1 (a). Output voltage waveform are shown in Fig. 1 (b) V_0 has different levels such as 0, Vin, 2Vin,…., nVin. It is clear that V_0 is just positive or zero, to generate waveform which approaches a nearly sinusoidal, final configuration is introduced in Fig. 2(a) that H bridge is connected to the cascaded basic unit which reverse alternate waveform to get positive, zero and negative levels.

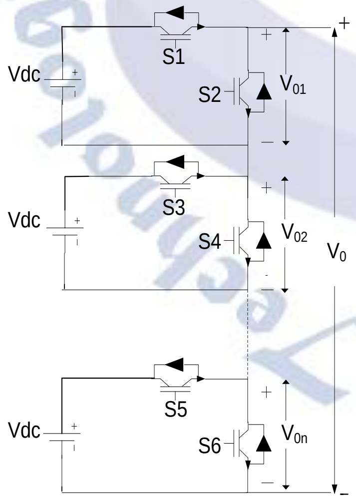


Fig.1 (a) Cascaded basic unit configuration

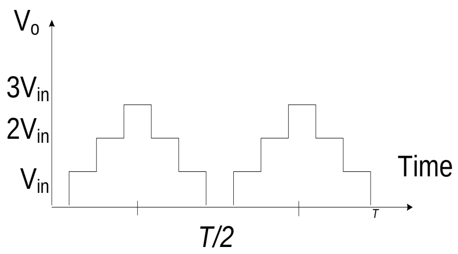


Fig.1 (b) Output voltage of basic unit configuration

For 0 < t < (T/2), Sa, S_b are fired together and positive half of V_{out} is generated, for (T/2) < t < T, S_c, S_d are on and negative half of output waveform is produced. It is obvious that period time of V_o is half of period time of V_{out}..

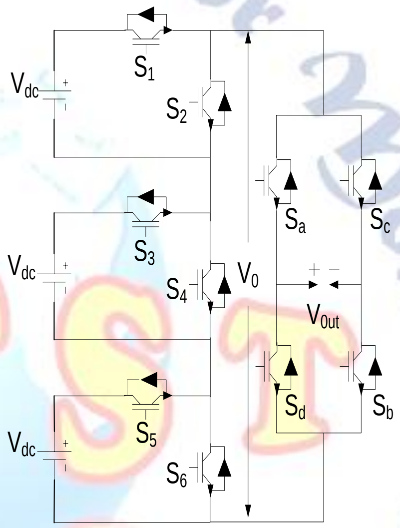


Fig.2 (a) Seven-level multilevel inverter

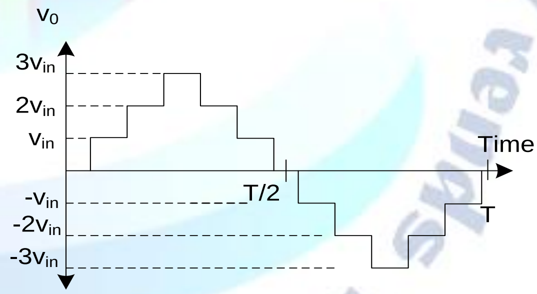


Fig. 2(b) Output voltage waveform of seven level inverter

In suggested topology, the maximum number of output phase voltage is given by

$$m = 2n + 1 \qquad (1)$$

n, m are the number of DC voltage sources and the maximum number of levels of phase voltage, respectively. In the conventional cascaded multilevel inverter, the relation between the number of DC voltage source and the maximum number of levels of output phase voltage is similar to suggested topology. As a result, for the same number of output phase voltage, the number of DC voltage source is the same.

The number of power electronic switches (IGBTs and gate drives) in the single phase of suggested topology is given by

$$k = m + 3 \qquad (2)$$

Where k is the number of switches,

In the conventional cascaded multilevel inverter the number of power switches is given by

$$k = 2(m - 1) \qquad (3)$$

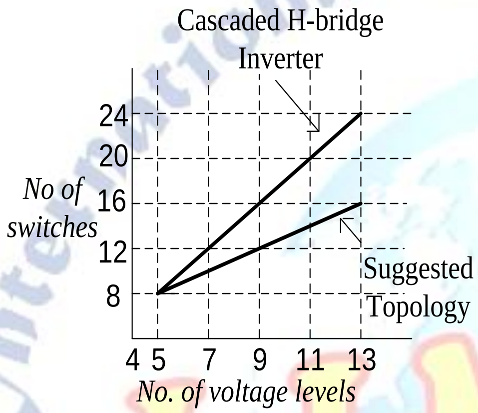


Fig.3 Comparison of switches to output voltage levels

Fig. 3 compares the number of switches with the conventional cascaded multilevel inverter. As shown in this figure, the suggested topology needs fewer switches for realizing m level voltages for output. This point reduces the installation area and the number of the gate driver. For example, to generate seven levels of output voltage (m=7), proposed topology needs 10 switches and conventional cascaded H-bridge multilevel inverter requires 12 switches.

B. STATCOM

STATCOM is a device which absorbs or generates reactive power from the system to provide voltage support without using large reactor or capacitor bank. Fig. 1 shows equivalent circuit of STATCOM, where Vc is fundamental component, Vs is system voltage. The voltage of reactance is V_l and the impedance is $R+jX_l$.

a. When STATCOM voltage is greater than supply voltage it injects reactive power.
b. When STATCOM voltage is less than supply voltage it absorbs reactive power.

When both voltages are equal, there will be no interaction between STATCOM and the system.

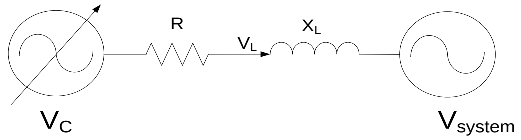


Fig.4. Equivalent circuit of STATCOM

Fig. 5 shows a single line diagram of STATCOM circuitry in which voltage source converter is coupled to power system through reactor. Here, VSC is fed by DC energy source. Voltage source converter used in STATCOM may be two-level or three-level type. Depending on the required output power and voltage, main function of VSC is to produce reactive power required for compensation. In normal condition VSC operate with fundamental frequency to minimize converter losses. Fig.5 shows the block diagram of direct current control method, it is divided into two parts: 1. Estimation of instantaneous reactive power and harmonic current. 2. Generation of gate pulse for voltage source converter.

For estimation of reactive power and harmonic current, initially Ia, Ib and Ic three phase load currents are transformed into α-β phase coordinates using abc-dq transformation (Park's transformation). Values of sine and cosine angle are obtained using virtual phase lock loop (PLL). In such a manner, ip (direct axis component) and iq (quadrature axis component) can be calculated. Here, only active channel ip is considered by terminating the reactive channel iq. Thereafter, ip is compared with the error signal obtained by the comparison of V_{dc} and V_{ref}. Furthermore, dq axis components are converter back to abc coordinates to calculate the fundamental active current signal.

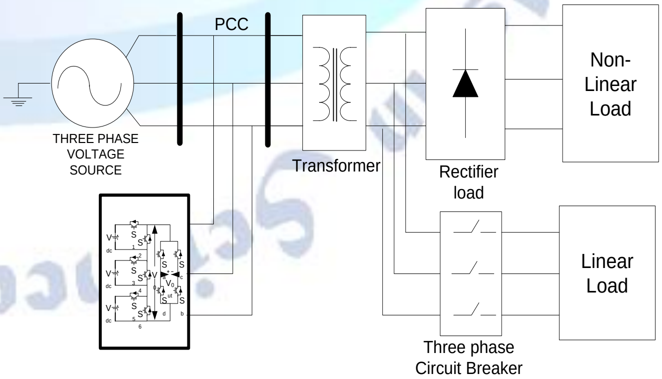


Fig.5. Schematic diagram of STATCOM connected power system using reduced switch Inverter.

III. Simulation Result

Configuration shown in Fig. 3(a) has been simulated using MATLAB/SIMULINK to verify the capabilities of mentioned inverter. Suggested multilevel inverter parameters are listed in Table 2.

Table 1 Simulated inverter parameters

Parameters	Values
V_{dc}	50V
T_{ca}	0.0002sec
V_{ca}	1
T	0.02Sec

Fig. No 6 shows output voltage of circuit shown in Fig 1 (a), Fig. No 7 shows output voltage of seven levels inverter.

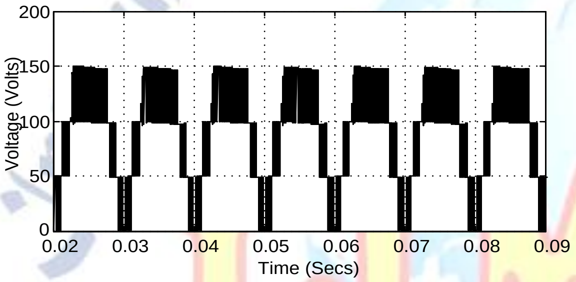


Fig.6 Output Voltage of Basic Unit Multilevel Inverter.

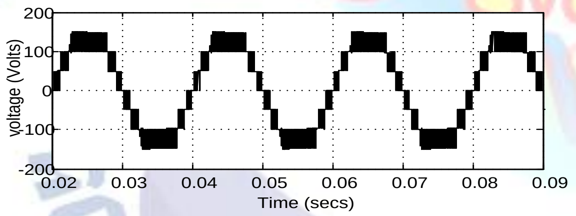


Fig.7 Output Voltage across Multilevel Inverter.

Table 3 Inverter voltage levels and THD%

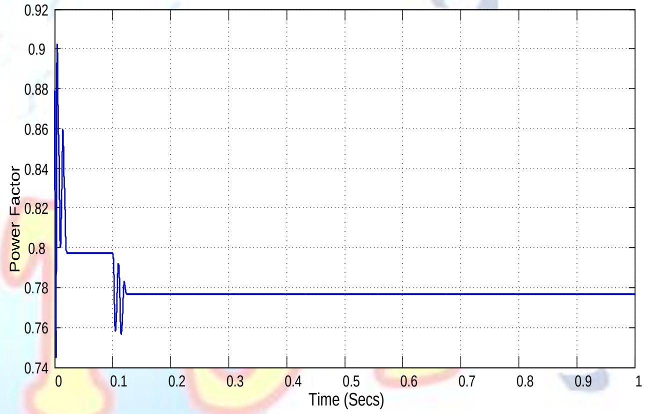
Sr. No	No. of voltage level	Total Harmonic Distortion	
		VSI	SRI
1	3	60.10%	60.17%
2	5	34.33%	32.54%
3	7	24.00 %	20.96 %
4	9	15.11%	15.73%

Table 4 Component count

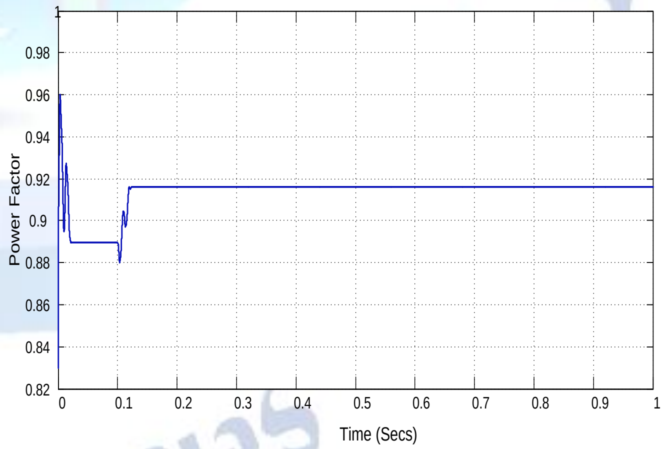
Number of Level (m)	Number of Switch (k)		Number of DC source (n)	
SRI and VSI	VSI	SRI	VSI	SRI
3	6	6	1	1
5	8	8	2	2
7	12	10	3	3
9	16	12	4	4
11	20	14	5	5

In table 2 and 3 VSI stands for conventional voltage source inverter and SRI stands for switch reduced inverter.

Also, fig.8 (a) and (b) shows that the power factor of considered system, before and after compensation, is improved from 0.77 to 0.916. This indicates the robustness of direct current control method. Hence, good reactive power compensation is achieved.



(Before Compensation)
Fig.8 A Phase B power factor



(Before Compensation)
Fig.8 B Phase B power factor

IV. Conclusion

In this study, the simulation of a reduced switch based multilevel inverter has been presented. The preferred inverter has fewer switches as compared to a traditional cascaded multilevel inverter. Reduced switch multilevel inverter based STATCOM proposed to improve the power factor of power system. Simulation and experimental results show the ability of the reduced switch multilevel inverter.

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