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Design of Low Power and Delay of Booth Multiplier using GDI Technique

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ABSTRACT

In digital signal processing the speed of the processor is dependent on the processing speed of a multiplier used in it, which affects total processing of a circuit. Hence, when a normal multipliers are used they consumes most of the power also gives rise to a delay. So to overcome these problems the high speed digital multiplier used nowadays. This paper introduced a low power booth multiplier, which work on a partial product, shifted approximately and addition. For the design of low power circuit the Gate Diffusion Input technique used. This technique plays a key role in the low power reduction technique. The speed booth multiplier is depending upon the partial product. As the booth multiplier cuts the required partial product into half so the speed of partial product increase's. The booth multiplier consists of a three section encoder, partial product generation unit and adder circuit. Implementation of a booth multiplier takes place using a cadence virtuoso. The result obtained is in term of average power and is compared with the performance of GDI to static CMOS technique at 45nm technology. The voltage used for the circuit varies from 0.1 to 0.7 volts.

KEYWORDS: *GDI-Gate diffusion input, Booth multiplier*

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. VLSI lets IC designers add all of these into one chip.In electronics, logic synthesis is a process by which an abstract form of desired circuit behaviour, typically at register transfer level (RTL), is turned into a design implementation in terms of logic gates, typically by a computer program called a synthesis tool.All the system consists of a basic block such as addition, shifting and multiplication. From the all above operations the multiplication is the main phenomenon which affects the speed of the system.

Digital signal processing (DSP) the important operations are filtering, inner product and spectral analysis. Here many of the operations such as filtering and product performed with the help of multiplication hence it plays a very curtail role for any DSP system [1]. Multiplication is a phenomenon of repeated addition. Various techniques applied internally and externally in the multiplier to reduce its power consumption [5]. The advantage of GDI technique over the

static CMOS is the use of less number of transistors, hence the reduction in the area and interconnects.

II. GDI INTRODUCTION

The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS is grounded. But in a GDI cell this might not necessarily occur. There are some important differences between the two. The three inputs in GDI are namely

1) G- common inputs to the gate of NMOS and PMOS.
2) N- input to the source/drain of NMOS.
3) P- input to the source/drain of PMOS Bulks of both NMOS and PMOS are connected to N or P (respectively) that is it can be arbitrarily biased unlike in CMOS inverter.

The advantages of GDI technique is that it uses the less number of transistors as compared to CMOS hence reduction in power and noise with the reduction in area take place. The circuits below consist of a basic GDI inverter, NAND and XOR gate in figure 1.

Various logic functions of GDI cell for different input configurations bulks to Out are directly polarized and there is a short between N and P, resulting in static power dissipation and this causes a drawback for OR, AND, and MUXimplementations in regular CMOS with configuration. The effect can be reduced if the design is performed in floating-bulk SOI technologies, where a full GDI library can be implemented.

III. GDI CELL

The GDI cell is displayed in figure which consists of one PMOS and one NMOS transistors, and Table shows the Truth Table of cell. It has two extra input pins which will used. The cell contains total three inputs P(input to source/drain of PMOS),G(combined gate input of PMOS and NMOS) and N(input to source/drain of NMOS).Both PMOS and NMOS bulks are linked to P or N, so it based on the CMOS inverter. In order to implement GDI it uses less number of transistors as compared to CMOS and pass transistor logic designs. The following figure shows symbol of GDI cell.

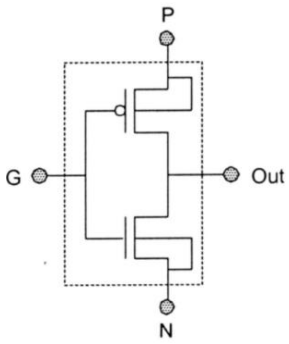

Fig 3.1: Basic GDI Cell

GDI logic cell simplified functional block diagram, which uses two transistors for implementing the logic functions. Basic GDI Logic cell contains P logic block, N logic block, first & second logic inputs, and three logic terminals: first & second dedicated logic terminals, and common diffusion logic terminal. The first &second dedicated logic terminals and the common diffusion logic terminal are capable of every work as either a logic signal input terminal or a logic signal output terminal, depending upon the precise logic circuit implementation.

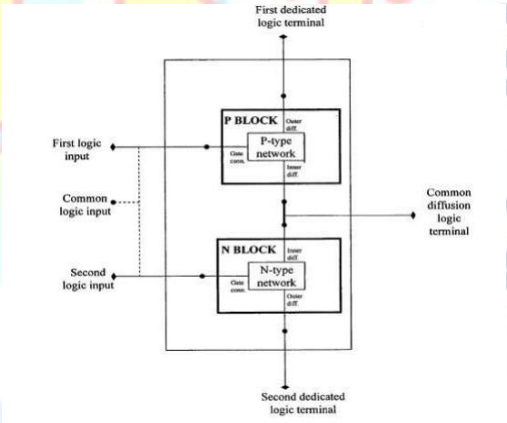

Fig 3.2: Logic Diagram of GDI cell

The following table shows the GDI cell based various logic functions using different input configuration and corresponding transistors count.

Table 3.1: Truth table for GDI cell

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'.B	F1	2
B	1	A	A'+B	F2	2
1	B	A	A + B	OR	2
B	0	A	A . B	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4

IV. PROPOSED GDI TECHNIQUE BOOTH MULTIPLIER

The main objectives of booth multiplier is to perform high speed operation and low power consumption. The booth multiplier is combination of repeated addition and shifting athematic which mainly take place by the help of encoder and partial product generating unit. As the speed and the power consumption of a multiplier depends upon the partial product so in booth multiplier the partial unit is reduced to half which result in an increase in speed and reduction in power consumption reduces. The maximum delay can be determined by the help of a sum of a total delay occur due to the partial product unit. There are mainly three sections in booth multiplier those are booth encoder, partial product generating unit and adder circuit.

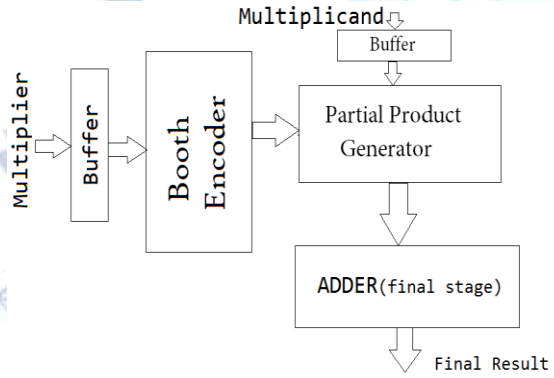

Fig 4.1: Block diagram of Booth multiplier

The working of booth encoder is to contained more number of zero's by converting input bits to equivalents bit. This can done by changing the 2's complement value to the single digit representation. The booth encoder is a combination of XOR and NAND gates. The input taken is in the form of input multiplicand value. This result obtained is according to this table given below. The encoder consist of a XOR gate, NAND gate and INVERTER circuit.

V. CMOS BASED BOOTH MULTIPLIER

A one-bit Booth Multiplier adds three one-bit numbers, often written as A,B and C_{in}; A and B are the operands, andC_{in} is a bit carried in from the previous less-significant stage It is possible to create a logical circuit using multiple full adders to add N-bit numbers The circuit produces a two-bit output. Those are carry and sum. The conventional Booth Multiplier consists of 28 transistors 16 for sum and 12 for carry.it occupies more chip area, increases power consumption and increases time delay when compared to GDI full adder. The schematic diagrams of conventional 28-T are shown in figure given below.

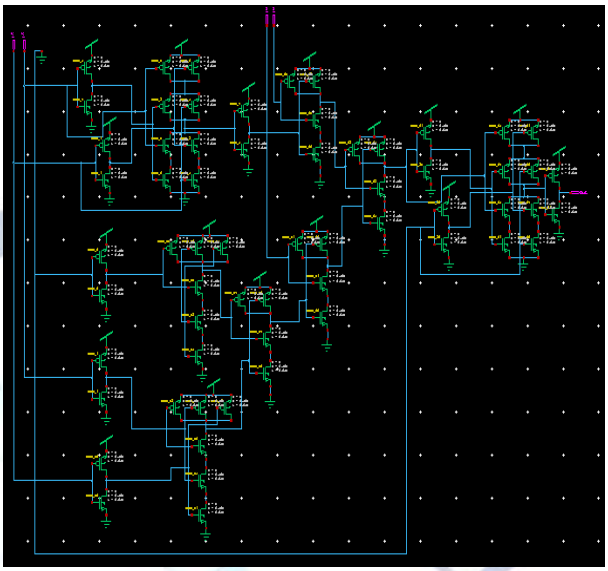

Fig 5.1: CMOS based Booth Multiplier Schematic

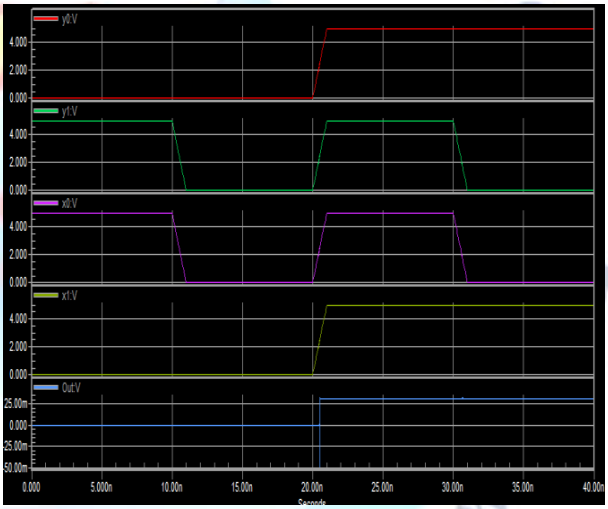

Fig 5.2: Simulation Result for CMOS based Booth Multiplier

GDI based Booth Multiplier

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in notation. Now we are implementing the low power Booth Multiplier circuit with the help of 2T MUX, made by GDI technique. It requires total 6 numbers of 2T MUX having same characteristics to design a 12T Booth Multiplier and connected as below figure.

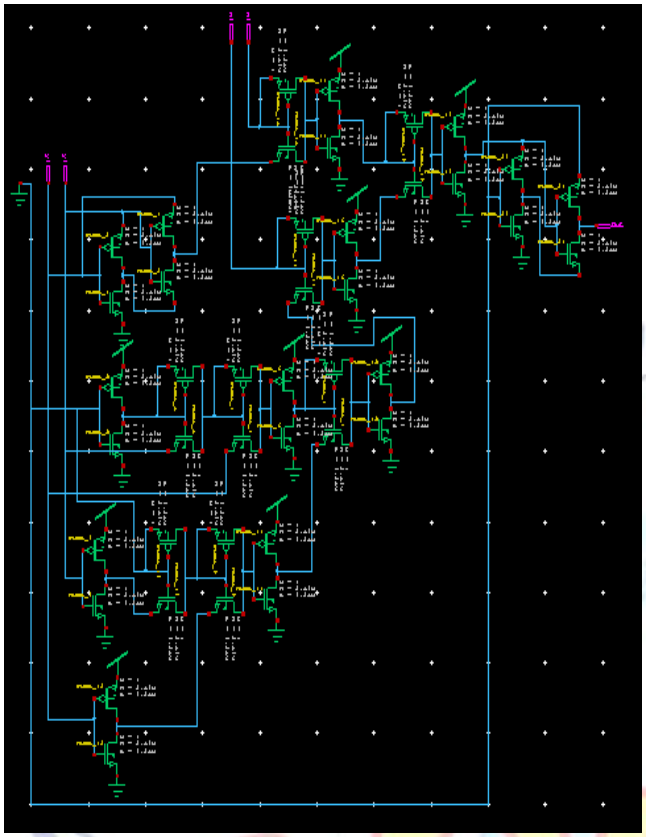

Fig 5.3: GDI based Booth Multiplier Schematic

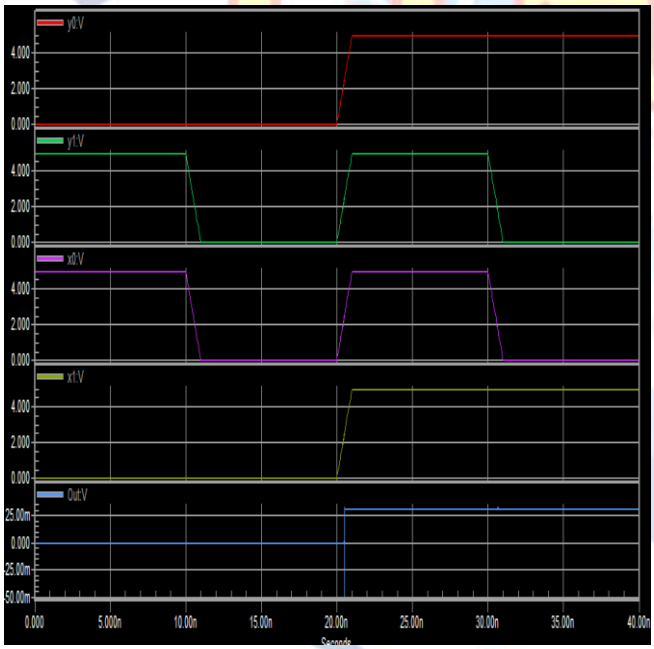

Fig 5.4: Simulation result for GDI based Booth Multiplier

Table 5.1: Average power and noise values of GDI based Booth multiplier

Input Value	Average Power	Noise
0.1 V	2.108 n	6.111 p
0.4 V	15.25 n	3.892 p
0.7 V	21.42 n	3.892 p

VI. CONCLUSION

In this paper a modified booth multiplier implemented using CMOS and GDI technique in 45 nm using a tool Tanner EDA 15.1 version. With the help of output value we conclude that the GDI technique is better than the CMOS technique in terms of power consumption and noise, as it reduces the switching of output value with the sudden change in inputs value also the area reduce with the reduction in transistor used in a circuit.Same work can be extend continue further investigation to achieve all the parameters require to more extension, like less power consumption, some more delay reduction, and the reduction the size of transistors to form gates used in this project, this the scope of the project further.

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