Available online at: http://www.ijmtst.com/vol5issue08.html

International Journal for Modern Trends in Science and Technology

ISSN: 2455-3778 :: Volume: 05, Issue No: 08, August 2019

Design of Low Power High Speed Double Tail Comparator using Power Gating Techniques

D Ramarao[1] | K Rajasekhar[2]

[1]PG Scholar, Dept of ECE, BABA Institute of Technology & Sciences, Visakhapatnam, Andhra Pradesh, India.

[2]Assistant Professor, Dept of ECE, BABA Institute of Technology & Sciences, Visakhapatnam, Andhra Pradesh, India.

To Cite this Article

D Ramarao and K Rajasekhar, "Design of Low Power High Speed Double Tail Comparator using Power Gating Techniques", *International Journal for Modern Trends in Science and Technology*, Vol. 05, Issue 08, August 2019, pp.-06-10.

Article Info

Received on 05-July-2019, Revised on 21-July-2019, Accepted on 25-July-2019, Published on 28-July-2019.

ABSTRACT

In the high speed analog to digital converters, comparator plays a vital role for reducing power consumption and performs high speed of operation. A double tail comparator is designed for improving the switching speed by using power gating techniques. These comparators are important in the modern mixed signal systems. Fine grain double tail comparator having low power consumption, delay and more switching speed.The proposed fine grain double tail comparator,which showslow power consumption and low propagation time. The minimal propagation time delay of 80 ns,and power consumption of 4.19 uw is achieved by the proposed fine grain double tail comparator.These results show that power has been reduced.Thus proposed comparator are optimized in such a way that it shows low power and low input propagation time, which is suitable for high speed ADCs.

KEYWORDS: *Double tail comparator, mixed signal*

I. INTRODUCTION

It is thus desirable to push the analog/digital boundary closer to the real world, where the system can take better advantage of the high-speed digital circuit. This trend puts high pressure on analog circuit designers to develop very high-speed interface circuits, namely, analog to digital and digital to analog converters (ADCs and DACs) that can keep up with the digital world yet still maintains other desirable attributes like low power consumption and small chip area. With shrinking of available power supply voltage and a number of new issues brought about by greatly reduced transistor size, this task seems to be more daunting than ever.Comparator is widely used in the process of converting analog signals to digital signals. In the A/D conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison. Low power and high-speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems.

In this paper, we developed a double tail latched comparator with power gating techniques and compare the results with the single tail latched comparator. To simulate the developed comparator in Tanner EDA Tools.

Power gating Techniques:

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. Inaddition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

By using power gating techniques to implement a model to control the parameters like power gate size, gate control slew rate, simultaneous switching capacitance and power gate leakage.

CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current.

II. DOUBLE TAIL COMPARATOR

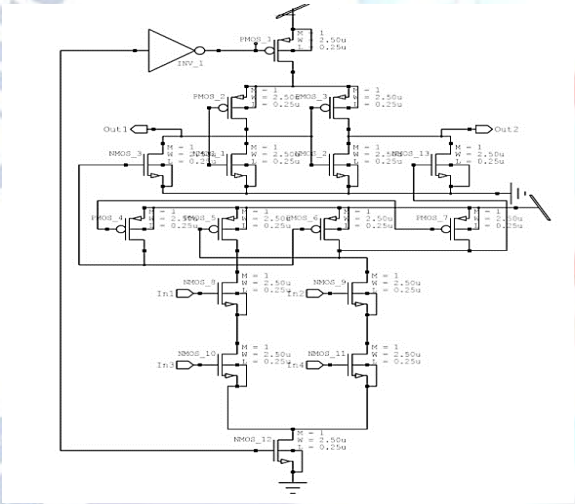

Figure 2.1: Schematic of Coarse Grain Double Tail Comparator

As long as fn continuously falling, the corresponding PMOS control transistors (Mc1 in this case) starts to turn on, pulling fp nodes back to the VDD; so another control transistors (Mc2) remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharging faster,a PMOS transistors (Mc1) turns on, pulling the other nodes fp back to the VDD.Therefore, the time passing, the difference between the fn and fp (Vfn/fp) increases in a exponential manner, leading to the reductions of latch regeneration times.

In this evident that the double tail comparator technologies can operates faster and be used in lower supply voltages, while consuming nearly the same powers as the conventional dynamics comparator. In case of even much better for the proposed comparator when compared to the conventional doubletail topology.

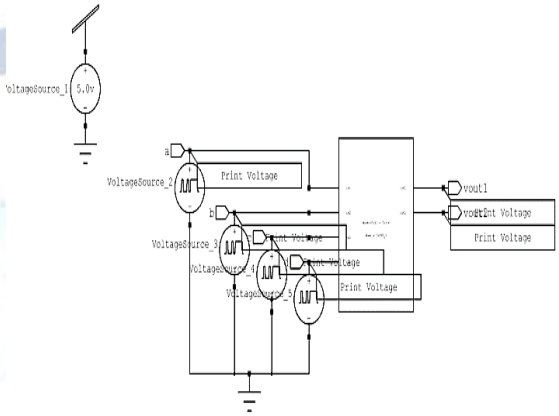

Figure 2.2: Schematic of Coarse Grain Double Tail Comparator

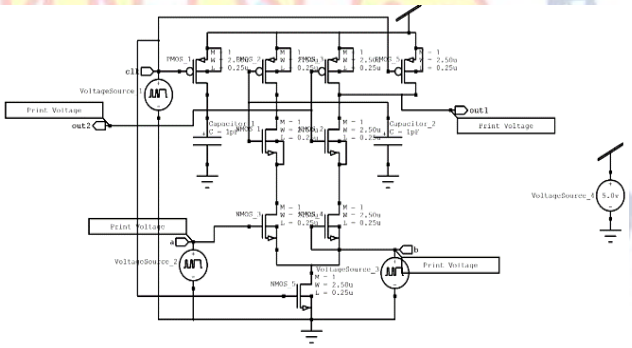

Figure 2.3: Schematic of Fine Grain Single Tail Comparator

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directlyaffect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistorsM3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5orM6 to start complete regeneration. At a low supplyvoltage, this voltage drop only contributes a

small gate-source voltage for transistorsM3andM4, where the gate source voltage ofM5andM6 is also small; thus, the delay time of the latch becomes large due to lower transconductance.

III. PROPOSED FINE GRAIN DOUBLE TAIL COMPARATOR:

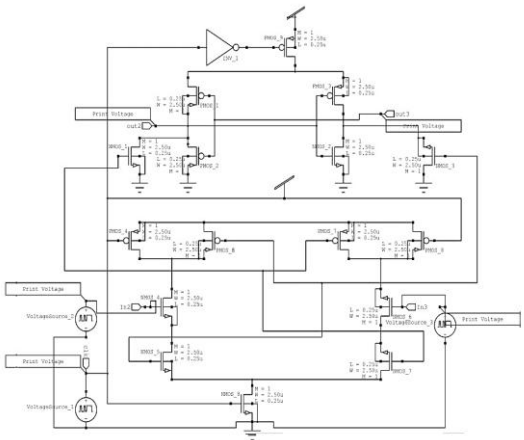

Figure 3.1 : Schematic of Fine Grain Double Tail Comparator

During reset phase (CLK=0, Mtail1 andMtail2 are off, avoiding static power),M3andM4pulls both fnand fp nodes to VDD, hence transistor Mc1andMc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs toground. During decision-making phase (CLK=VDD, Mtail1 and Mtail2 are on), transistorsM3andM4turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP >VINN, thus fn drops faster than fp, (since M2provides more current thanM1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1in this case) startsto turn on, pulling fp node back to the VDD; soanother control transistor (Mc2) remains off,allowing fnto be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOStransistor (Mc1) turns on, pulling the other nodefp back to the VDD. Therefore by the time passing, the difference between fn and fp (Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time . Despite the effectiveness of the proposed idea, one of the points whichshould be considered is that in this circuit, when one of the control transistors (e.g.,Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, andMtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors.

At the beginning of the decision-makingphase, due to the fact that both fn and fp nodeshave been pre-charged to VDD (during the reset phase), both switches are closed and fn and fptart to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch

IV. SIMULATION RESULTS

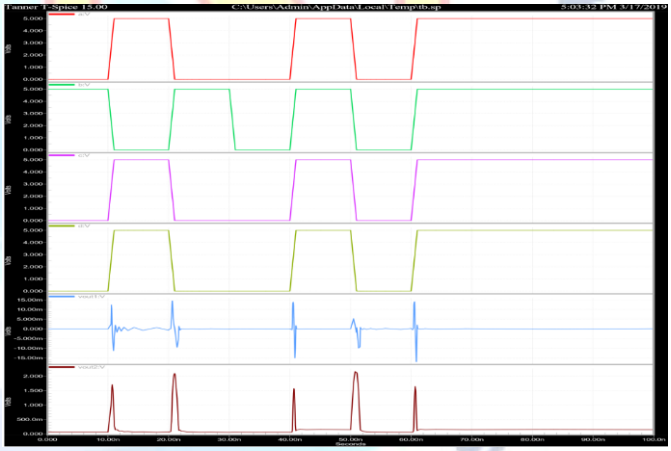

Figure 4.1: Simulated Waveforms for Coarse Grain Double Tail Comparator

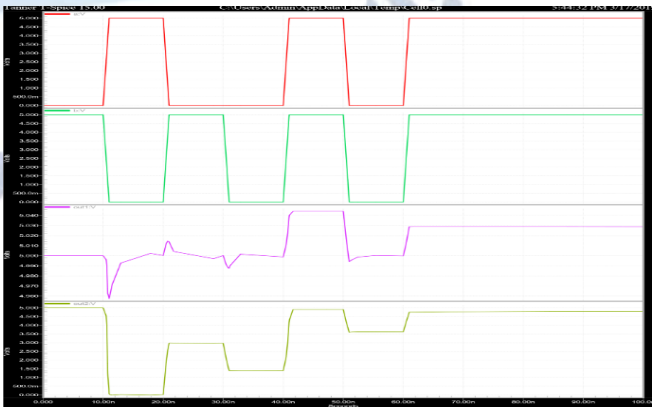

Figure 4.2: Simulated Waveforms for Fine Grain Single Tail Comparator

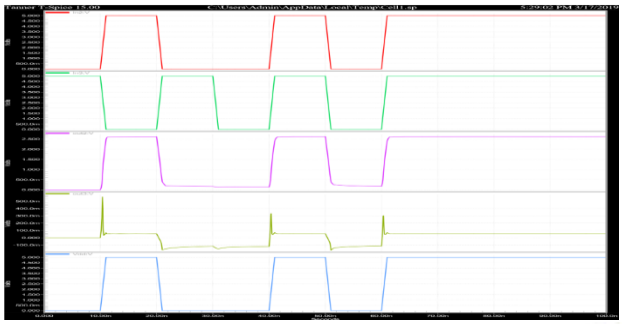

Figure 4.3: Simulated Waveforms for Fine Grain Double Tail Comparator

Parameters Comparison:

Table illustrates the all the performance parameters of different comparators.

Table: 4.1 Performance parameters for various comparators

Parameter	Coarse Grain Double Tail	Fine Grain	
		Single Tail	Double Tail
No of Transistors	18	9	19
Delay	80.9000ns	80.9000ns	50.9000ns
Power	9.10836uw	8.909175uw	4.1955uw

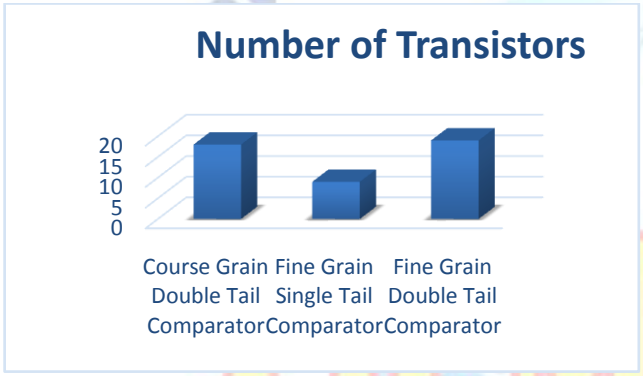

Figure 4.4: Comparison in Number of Transistors

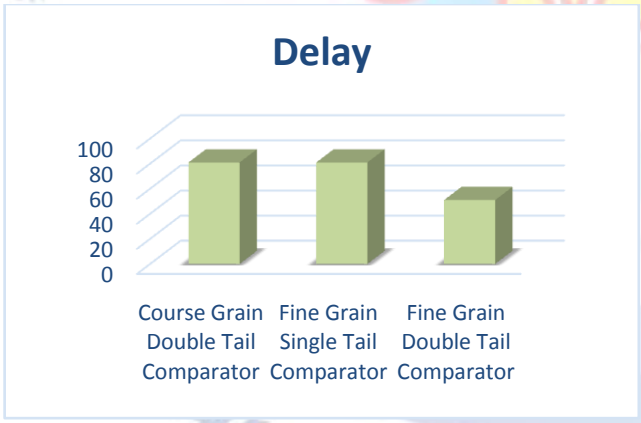

Figure 4.5: Comparison of Delay

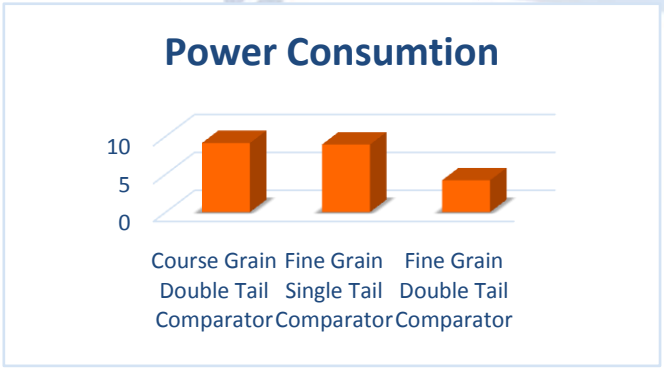

Figure 5.6: Power Comparison

V. CONCLUSION

In this thesis, the comparator circuits for high-speed ADCs have been investigated. The comparator circuits are mainly optimized for the low propagation time, minimal input referred offset voltage, low power consumption and minimal circuit area.The proposed fine grain double tail comparator,which showslow power consumption and low propagation time.The minimal propagation time delay of 80 ns,and power consumption of 4.19 uw is achieved by the proposed fine grain double tail comparator.These results show that power has been reduced.Thus proposed comparator are optimized in such a way that it shows low power and low input propagation time, which is suitable for high speed ADCs.

REFERENCES

[1] Samaneh Babayan-mashhadi, And Reza Lotfi, "Analysis And Design Of A Lowvoltage Low-power Double-tail Comparator", IEEE Trans. on Very Large Scale Integration (Vlsi) Systems, 2013.

[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65nm CMOS for supply voltages down to 0.65," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," Int. J. Analog Integr. Circuits Signal Process., vol. 66, no. 2, pp. 213–221, Feb. 2011

[4] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," inProc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.

[5] B. J. Blalock, "Body-driving as a LowVoltage Analog Design Technique for CMOS technology," in Proc. IEEE Southwest Symp. Mixed-Signal Design, Feb. 2000, pp. 113–118.

[6] M. Maymandi-Nejad and M. Sachdev, "1bit quantiser with rail to railinput range for sub1V Δ modulators," IEEE Electron. Lett., vol. 39, no. 12, pp. 894–895, Jan. 2003.

[7] Y. Okaniwa, H. Tamura, M. Kibune, D. Yamazaki, T.-S. Cheung, J. Ogawa, N. Tzartzanis, W. W. Walker, and T. Kuroda, "A 40Gb/s CMOS clocked comparator with bandwidth modulation technique," IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1680–1687, Aug. 2005.

[8] B. Goll and H. Zimmermann, "A 0.12 µm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, Feb. 2007, pp. 316–317.

[9] B. Goll and H. Zimmermann, "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3mW at 1.2V and 700MHz/47µW at 0.6V," in Proc. IEEE Int. Solid-State Circuits Conf. Papers, Feb. 2009, pp. 328–329.

[10] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12 µm CMOS," IEEE Electron. Lett., vol. 43, no. 7, pp. 388–390, Mar. 2007.

[11] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latchtype voltage sense amplifier with 18ps Setup+Hold time," in Proc. IEEE Int. SolidState Circuits Conf., Dig. Tech. Papers, Feb. 2007, pp. 314–315.

[12] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.