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Low Power and Area Efficient GDI Based Modified Booth Multiplier

S. Aruna Kumari[1] | Ravi Naga Srinivas[2] | B. Siva Prasad[3]

[1]Assistant Professor, Department of ECE, Baba Institute of Technology and Sciences, Visakhapatnam, Andhra Pradesh, India.

[2]PG Scholar, Department of ECE, Baba Institute of Technology and Sciences, Visakhapatnam, Andhra Pradesh, India.

[3]Associate Professor and Head, Department of ECE, Baba Institute of Technology and Sciences, Visakhapatnam, Andhra Pradesh, India.

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ABSTRACT

In digital signal processing the speed of the processor is dependent on the processing speed of a multiplier used in it, which affects total processing of a circuit. Hence, when a normal multipliers are used they consumes most of the power also gives rise to a delay. So to overcome this problems the high speed digital multiplier used nowadays. This paper introduced a low power modified booth multiplier, which work on a partial product, shifted approximately and addition. For the design of low power circuit the Gate Diffusion Input technique used. This technique plays a key role in the low power reduction technique. The speed modified booth multiplier is depending upon the partial product. As the modified booth multiplier cuts the required partial product into half so the speed of partial product increase's. The booth multiplier consists of a three section encoder, partial product generation unit and adder circuit. Implementation of a booth multiplier takes place using a Tanner EDA 15.0 version. The result obtained is in term of average power and is compared with the performance of GDI to static CMOS technique at 45nm technology. The voltage used for the circuit varies from 0.1 to 0.7 volts.

Keywords— *Modified Booth Multiplier, Tanner tools, Gate Diffusion Input (GDI), Multipliers.*

I. INTRODUCTION

All the system consists of a basic block such as addition, shifting and multiplication. From the all above operations the multiplication is the main phenomenon which affects the speed of the system. Often many problems arise due to the speed of a multiplication operation. Digital signal processing (DSP) the important operations are filtering, inner product and spectral analysis. Here many of the operations such as filtering and product performed with the help of multiplication hence it plays a very curtail role for any DSP system [1]. Multiplication is a phenomenon of repeated addition. There are various types of low power digital multiplier is present with high clock frequency. They play a wide role in today digital image processing, hence is the heart for today mobile communication system [2]. Recently because of increase in demand of battery - powered and of high speed electronic devices, power consumption became a very serious and important factor in VLSI chips because of the increase in the non-linear effect. The power consumption also affects the battery life of a device [3]. Because the output current of the MOS source coupled multiplier in a differential pair is depends upon the non linearity of the biased current (Iss)

and input signal. Various techniques applied internally and externally in the multiplier to reduce its power consumption [5]. The advantage of GDI technique over the static CMOS is the use of less number of transistors, hence the reduction in the area and interconnects

II. GDI INTRODUCTION

Arkadiy Morgenshtein was the first to introduce a basic GDI cell in 2002. There are several other power reduction techniques were present in which GDI provide lowest power dissipation as it reduces the logic switching hence the power loss in charging and discharging of capacitance is reduced and static power dissipation also reduces. The basic GDI cell consists of PMOS and NMOS having of four terminals each (gate, drain, body and source). Here the body of PMOS connected to Vdd and NMOS to the ground to provide better output. The advantages of GDI technique is that it uses the less number of transistors as compared to CMOS hence reduction in power and noise with the reduction in area take place. The circuits below consist of a basic GDI inverter, NAND and XOR gate in figure 1.

Various logic functions of GDI cell for different input configurations bulks to Out are directly polarized and there is a short between N and P, resulting in static power dissipation and this causes a drawback for OR, AND, and MUX implementations in regular CMOS with configuration. The effect can be reduced if the design is performed in floating-bulk SOI technologies, where a full GDI library can be implemented.

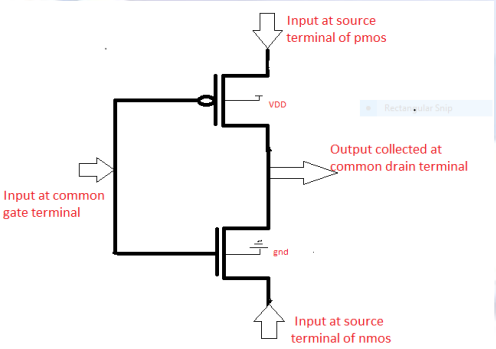


Figure 1 Basic GDI cell

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table 1 Function table of GDI Logic

III. MODIFIED BOOTH MULTIPLIER

The main objectives of modified booth multiplier is to perform a high speed operation and low power consumption. The modified booth multiplier is combination of repeated addition and shifting arithmetic which mainly take place by the help of encoder and partial product generator unit. As the speed and the power consumption of a multiplier depends upon the partial product so in modified booth multiplier the partial unit is reduced to half which result in an increase in speed and reduction in power consumption reduces. The maximum delay can be determined by the help of a sum of a total delay occur due to the partial product unit. There are mainly three sections in modified booth multiplier those are booth encoder, partial product generator unit and adder.

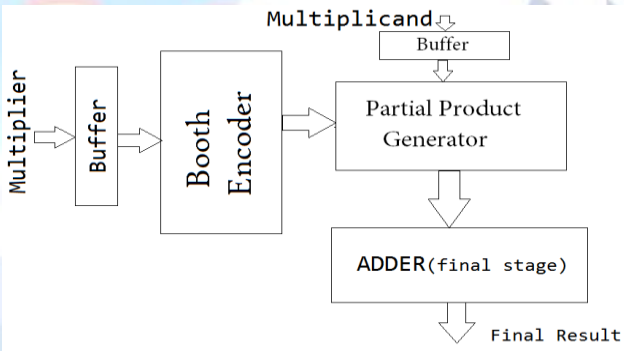


Figure 2 Modified Booth Multiplier block diagram

A. Booth Encoder:

The encoder is the main section to take the multiplier inputs from it. The booth encoder section consists of combination of XOR and NAND gates. The result obtained is according to this table given below. The encoder consist of a XOR gate, NAND gate and INVERTER circuit, In this encoder the MUX operation is also perform. This result obtained is according to this table given below

Multiplicand		Output
Bit i	Bit i-1	Selected by bit i
0	0	0*M
0	1	+1*M
1	0	-1*M
1	1	0*M

Table 2 Booth Encoder Table

The encoder consist of a XOR gate, NAND gate and INVERTER circuit. The figure below is a modified booth encoder circuit.

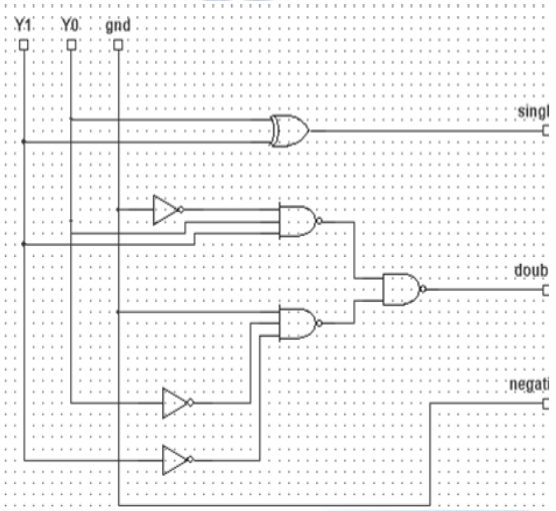


Figure 3 Modified Booth Encoder circuit diagram

B. Partial Product Generator Unit:

In this block the multiplicand bit is multiplied with the output of encoder unit with the help of NAND gate as NAND gate multiplies the two inputs value to each other to form a partial product output. Here the equivalent value is converted to the single bit partial product which is later provided to the adder circuit to generate the output of modified booth multiplier.

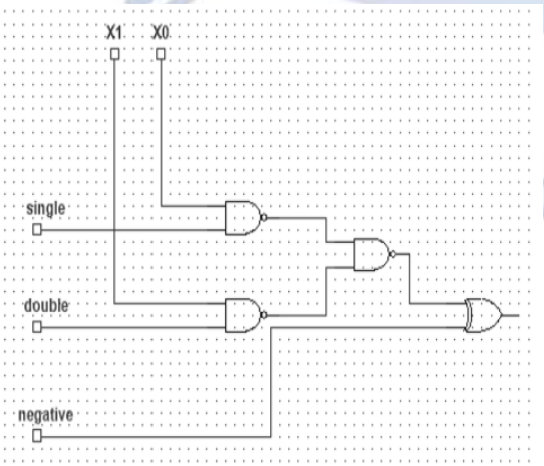


Figure 4 Partial Product Generator Unit Circuit Diagram

IV. RESULT AND SIMULATION

The simulation of a modified booth multiplier using the GDI technique and CMOS technique is carried out and compares them. The simulation performed done using a software Tanner EDA 15.0 version at 45 nm. The result obtained in terms of average power and noise. The input value of a voltage taken is 0.7 volt. Here the simulated waveform show that the switching activity in CMOS technique is more as compared to GDI technique which give rise to the static and dynamic power dissipation in the circuit.

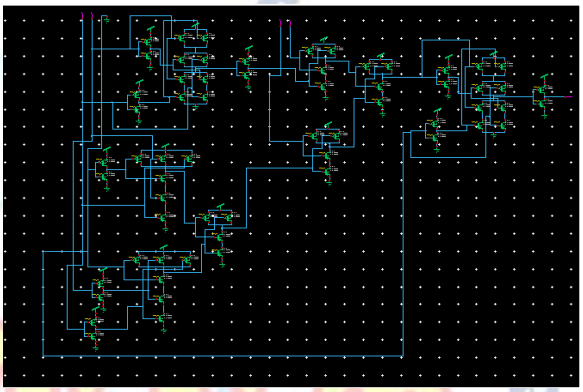


Figure 5 Cmos implementation of modified booth multiplier

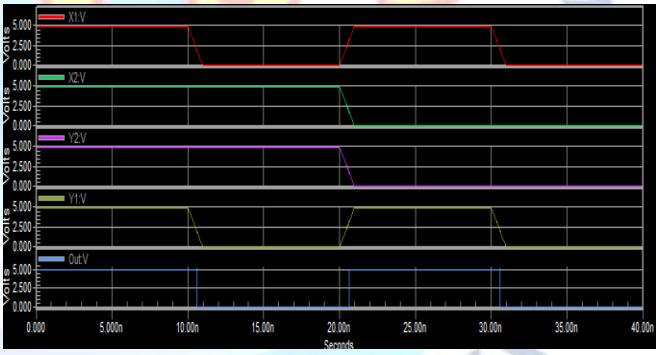


Figure 6 Simulated CMOS modified booth multiplier waveform

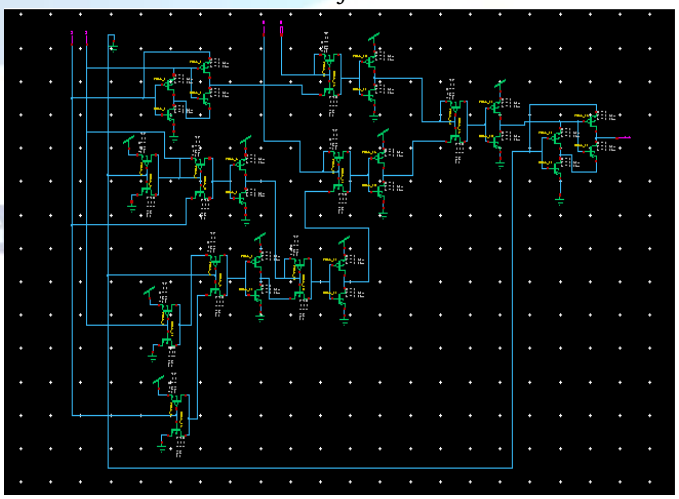


Figure 7 GDI implementation of modified booth multiplier

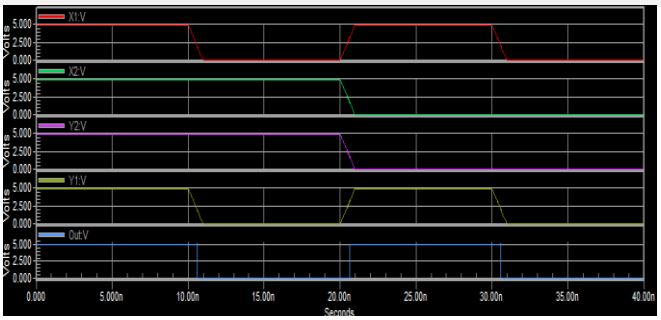
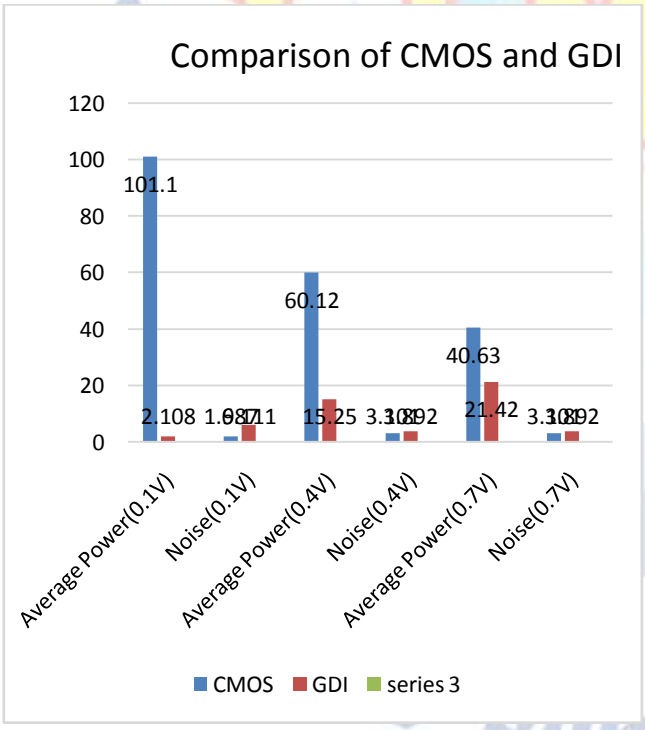


Figure 8 Simulated GDI modified booth multiplier waveform

Input Value	Average Power		Noise	
	CMOS	GDI	CMOS	GDI
0.1 V	101.1n	2.108n	1.987 f	6.111f
0.4 V	60.12n	15.25n	3.101 f	3.892f
0.7 V	40.63n	21.42n	3.101f	3.892f

Table 3 Comparison Table Of CMOS Technique And GDI Technique



V. CONCLUSION

In this paper a modified booth multiplier implemented using CMOS and GDI technique in 45 nm using a Tanner EDA 15.0 Version. With the help of output value we conclude that the GDI technique is better than the CMOS technique in terms of power consumption and noise, as it reduces the switching of output value with the sudden change in inputs value also the area reduce with the reduction in transistor used in a circuit.

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