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# Design and Optimization of a High-Speed CMOS Carry Look-Ahead Decimal Adder (CLDA)

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***KEYWORDS***

*BCD adders, CLDA, CMOS technology, decimal arithmetic, decimal hardware, LT-SPICE, PDP*

**ABSTRACT**

*Decimal arithmetic has gained significant attention due to its importance in financial, commercial, and other human-centric applications where decimal precision is essential. Hardware implementations of decimal arithmetic outperform software-based solutions in real-time systems. Among decimal operations, addition is fundamental as most arithmetic functions rely on it. Traditional Ripple Carry Adders (RCA) suffer from large propagation delays due to sequential carry propagation. This work proposes two CMOS-based Carry Look-Ahead Decimal Adders (CLDAs) designed to improve speed while maintaining acceptable power consumption. The Boolean logic for the proposed CLDAs is derived and implemented using CMOS circuits. The designs are simulated using a 45 nm technology library in LT-SPICE. Simulation results demonstrate improved performance in terms of speed, power efficiency, and Power Delay Product (PDP), making the proposed CLDAs suitable for integration into decimal arithmetic units.*

## I. INTRODUCTION

The Binary number is the standard number system for electronic computers in the modern computing world. However, decimal arithmetic is essential for many applications, including commerce, banking, and Internet-based business. The updated IEEE 754-2008 standard has included decimal arithmetic to reflect its importance. Thus, there is a rising demand for high-performance decimal computer arithmetic designs.

Human beings have preferred decimal as their number base for all calculations done by hand, since the time when the man learned to count on his ten fingers. This fact has never changed, although binary has been selected as the default base for almost all computers due to the storage and the speed efficiency of binary hardware. The designers have preferred binary computers due to the speed and simplicity of binary arithmetic, but nowadays, there is an increasing demand

for the hardware support to decimal arithmetic in financial and commercial applications. This is due to the following reasons: Most of the fractional decimal numbers, such as 0.1, cannot be exactly represented in binary format and therefore, their approximate representations are used in binary arithmetic operations. This is not tolerable for most financial and commercial applications, which require exact representation of decimal numbers.

The commercial databases contain more decimal data than binary data. Therefore, when the binary hardware is used, the decimal data is converted from decimal to binary and after it is processed, the binary data is converted back to decimal in order to store the result in decimal format. However, the conversion between decimal and binary formats causes too much delay. In all arithmetic units, whether binary or decimal, an adder is used. Therefore, adders play a vital role in the performance of the system. Here we have proposed a reduced delay BCD adder in which delay is much reduced compared to that of conventional BCD adder.

Classical computing devices process large amount of digital data using logical (Boolean) operations. A single bit of information is erased after every logical operation.Landauer proposed that KT ln(2) joules of energy are lost for erasing a single bit of data, where K is the Boltzmann's constant and T is the absolute temperatureat which computation is performed. Energy dissipation is one of the major issues in present day technology. Improvement in technology leads to compactness in size of system and increase in execution speed. Due to this energy dissipation is increased by the system.

The logical circuits used in these systems are called irreversible systems. Charles Bennet proposed a theoretical background which proved that reversible general purpose computing devices can be built [1, 2]. This gave rise to reversible logic circuits. Logical reversibility means that after finishing a computation, it is possible to retrace every step and reconstruct data which was used in every step. Thus, reversible logic circuits offer an alternative that allows computation with very small energy dissipation.

The main objective of this work is to perform both BCD addition in a single circuit with minimum number of garbage gate count and constant input. To achieve the operation of qca BCD addition in a single circuit two new gates are proposed which are optimized such that it doesn't possess any restrictions of qca gates as mentioned above. It has been proved that the proposed reversible BCD arithmetic circuit is better than the existing logics in the literature; in terms of number of garbage outputs, constants inputs and the gate count.

## 2.LITERATURE REVIEW

**Cost-efficient decimal adder design in quantum-dot cellular automata by W. Liu, L. Lu, E. E. Swartzlander, and M. OŠNeill:**

Applications that cannot tolerate the loss of accuracy that results from binary arithmetic demand hardware decimal arithmetic designs. Binary arithmetic in Quantum-dot cellular automata (QCA) technology has been extensively investigated in recent years. However, only limited attention has been paid to QCA decimal arithmetic. In this paper, two cost-efficient binary-coded decimal (BCD) adders are presented. One is based on the carry flow adder (CFA) using a conventional correction method. The other uses the carry look ahead (CLA) algorithm which is the first QCA CLA decimal adder proposed to date. Compared with previous designs, both decimal adders achieve better performance in terms of latency and overall cost. The proposed CFA-based BCD adder has the smallest area with the least number of cells. The proposed CLA-based BCD adder is the fastest with an increase in speed of over 60% when compared with the previous fastest decimal QCA adder. It also has the lowest overall cost with a reduction of over 90% when compared with the previous most cost-efficient design.

**Decimal floating-point: Algorism for computers by M. F. Cowlishaw:**

Decimal arithmetic is the norm in human calculations, and human centric applications must use a decimal floating point arithmetic to achieve the same results. Initial benchmarks indicate that some applications spend 50% to 90% of their time in decimal processing, because software decimal arithmetic suffers a 100/spl times/ to 1000/spl times/ performance penalty over hardware. The need for decimal floating point in hardware is urgent. Existing designs, however, either fail to conform to modern standards or are incompatible with the established rules of decimal arithmetic. We introduce a new approach to decimal floating point which not only provides the strict results which are necessary for

commercial applications but also meets the constraints and requirements of the IEEE 854 standard. A hardware implementation of this arithmetic is in development, and it is expected that this will significantly accelerate a wide variety of applications.

**Conditional speculative decimal addition by A. Vázquez and E. Antelo:**

Decimal arithmetic circuits compliant with the IEEE-754-2008 floating-point standard typically employ 10-bit Densely Packed Decimal (DPD) encoding to represent three Binary-Coded Decimal (BCD) digits efficiently. While DPD reduces storage requirements compared to straightforward BCD representation, arithmetic operations usually require unpacking DPD data into BCD format, performing the operation, and then repacking the result back into DPD. This repeated conversion process introduces additional delay, hardware overhead, and power consumption.

To address these limitations, the proposed approach adopts Binary-Coded-Chiliad (BCC) encoding as an alternative internal arithmetic format. BCC encoding packs three BCD digits into 10 bits, similar to DPD in storage efficiency, but it allows direct arithmetic manipulation without the need for unpacking and repacking during each operation. In this methodology, decimal data retrieved from memory (in DPD format) are converted once into BCC form. All intermediate arithmetic computations—such as addition and accumulation—are performed entirely in BCC format. The results are stored in a BCC register file throughout multi-operation sequences and converted back to DPD format only when final results must be written back to memory or displayed.The design and synthesis of improved mixed BCC/binary adders aim to enhance performance efficiency. By optimizing internal carry handling and decimal correction logic in BCC format, the proposed arithmetic units demonstrate improvements in area utilization and power consumption when compared with traditional BCD and earlier BCC adders.

**Device architecture for computing with quantum dots by C. S. Lent and P. D. Tougaw:**

We describe a paradigm for computing with interacting quantum dots, quantum-dot cellular automata (QCA). We show how arrays of quantum-dot cells could be used to perform useful computations. A new adiabatic switching paradigm is developed which permits clocked control, eliminates metastability problems, and enables a pipelined architecture.

**A novel XOR/XNOR structure for modular design of QCA circuit by L. Wang and G. Xie:**

Quantum dot cellular automata (QCA) is considered one of the most promising technologies to replace the current CMOS technology. Compared with the traditional transistor technology, the computation relies on a new paradigm based on the interaction between nearby QCA cells. It has significant advantages, such as operating frequency (THz), high device density, and low power consumption. In this brief, a novel XOR/XNOR-function logic gate with two inputs, two enable inputs and one output is proposed and designed in Quantum-dot Cellular Automata (QCA) nanotechnology. In order to demonstrate the functionality and capabilities of the proposed QCA-based XOR/XNOR architecture, performance is evaluated and analyzed. The proposed XOR/XNOR logic gate has a superb performance in terms of area, complexity, power consumption and cost function in comparison to some existing QCA-based XOR architectures. Moreover, some efficient circuits based on the proposed XOR/XNOR gate are designed in QCA.

Design of efficient

**BCD adders in quantum-dot cellular automata by G. Cocorullo, P. Corsonello, F. Frustaci, and S. Perri:**

Among the emerging technologies recently proposed as alternatives to the classic CMOS, quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultralow-power and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. This brief proposes a new approach to design QCA-based BCD adders. Exploiting innovative logic formulations and purpose-designed QCA modules, computational speed significantly higher than existing counterparts is achieved without sacrificing either the occupied area or the cell count.

**3.EXISTING SYSTEM**

A BCD adder is a circuit that adds two BCD digits and produces a sum digit also in BCD. BCD numbers use 10 digits, 0 to 9 which are represented in

the binary form 0 0 0 0 to 1 0 0 1, i.e. each BCD digit is represented as a 4-bit binary number. When we write BCD number say 5 2 6, it can be represented as 0101 0010 0110. Here, we should note that BCD cannot be greater than 9. The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added. By examining the three cases of BCD addition we can summarise the BCD addition procedure as follows:

1.Add two BCD numbers using ordinary binary addition.

2. If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.

3. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.

4. To correct the invalid sum, add 0110 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Thus to implement BCD adder we require:

- 4-bit binary adder for initial addition
- Logic circuit to detect sum greater than 9 and
- One more 4-bit adder to add 0110 in the sum if sum is greater than 9 or carry is 1.

The logic circuit to detect sum greater than 9 can be determined by simplifying the Boolean expression of given truth table.

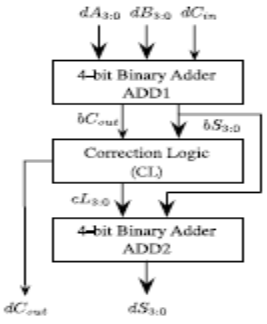


**Figure 1:Conventional Design**

As shown in the Figure 2, the two BCD numbers, together with input carry, are first added in the top 4-bit binary adder to produce a binary sum. When the output carry is equal to zero (i.e. when Sum <= 9 and Cout=0) nothing (zero) is added to the binary sum. When it is equal to one (i.e. when Sum >9 or Cout = 1), binary 0110 is added to the binary sum through the bottom 4-bit binary adder. The output carry generated from the bottom binary adder can be ignored, since it supplies information already available at the output-carry terminal.

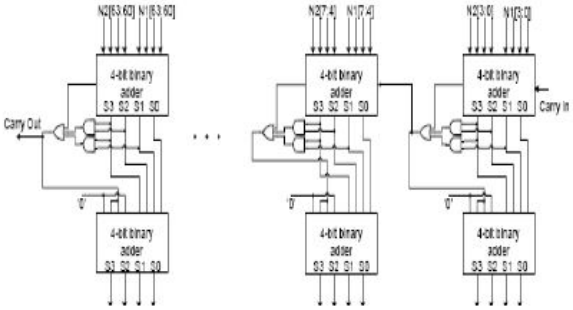


**Figure 2: Conventional BCD Adder**

**4.PROPOSED SYSTEM**

The proposed system is a hierarchical, high-performance **16-bit Binary Coded Decimal (BCD) adder** designed using modular and structured Verilog HDL. The system is built by cascading four 4-bit BCD adder blocks to enable multi-digit decimal arithmetic suitable for digital systems requiring precise decimal computations. The architecture emphasizes modularity, scalability, fast carry propagation, and logical clarity, making it appropriate for FPGA and ASIC implementations.

At the core of the proposed system is the **4-bit BCD adder module**, which performs decimal addition on two BCD digits along with an input carry. Unlike conventional binary adders, a BCD adder must detect invalid decimal results (greater than 9) and apply decimal correction. The proposed design incorporates propagate–generate logic to improve carry computation efficiency. Instead of relying solely on ripple carry propagation, the system utilizes structured intermediate modules such as pre, gray, and post blocks to compute propagate and generate signals. This approach reduces carry delay and enhances overall performance.

The first stage of the 4-bit BCD adder is the **pre-processing stage**, where propagate (p) and generate (g) signals are computed for each bit of the two 4-bit inputs. The propagate signal represents whether a carry will propagate through the bit position, while the generate signal indicates whether a carry is produced at that bit. These signals form the foundation for fast carry computation. By pre-computing propagate and generate

conditions, the system ensures structured carry evaluation rather than purely sequential carry passing.

The second stage consists of the **carry computation network**, implemented using gray blocks. These blocks compute intermediate carries using the propagate and generate signals along with the incoming carry. This method resembles a simplified prefix-style carry structure, enabling faster carry determination compared to traditional ripple architectures. The carries generated at each stage (c1, c2, c3, c4) are used both for sum computation and for determining decimal correction requirements.

Following carry computation, the **post-processing stage** determines intermediate sum bits. However, since BCD arithmetic must produce valid decimal digits (0–9), additional correction logic is required. In decimal arithmetic, whenever the binary sum exceeds 1001 (decimal 9) or a carry is generated from the most significant bit, a correction factor of 6 (0110) must be added to the intermediate result. The proposed system detects this condition using combinational logic expressions derived from intermediate sum outputs and carry signals. Specifically, logical combinations such as z2 & z4, z3 & z4, and the most significant carry are used to determine whether correction is necessary.

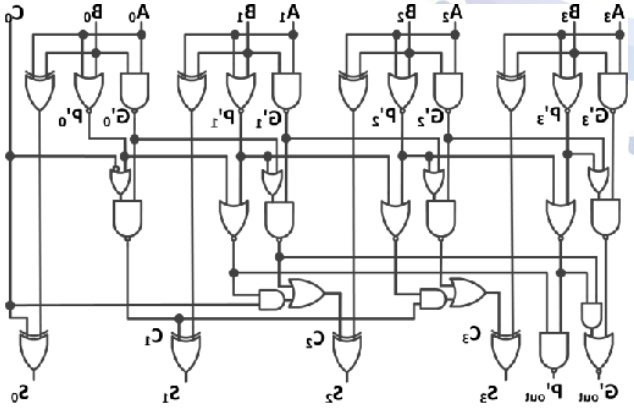

**Figure 3: Proposed 1-bit BCD adder**

Once the correction condition is detected, additional adders (such as fulladder1) perform the required correction by adding the value 6 to the intermediate binary sum. This guarantees that the final output digit is a valid BCD number. The corrected outputs are assigned to the final sum vector, while the correction carry becomes the output carry (co) of the module. Thus, each 4-bit module performs complete decimal addition with correction in a self-contained manner.

To support multi-digit decimal arithmetic, the proposed system integrates four such 4-bit BCD adders into a **16-bit BCD adder module**. Each 4-bit block represents one decimal digit. The carry output from a lower significant digit becomes the carry input of the next higher significant digit. This cascading structure enables addition of four-digit decimal numbers. The final carry output from the most significant digit represents overflow, indicating that the result exceeds the 4-digit decimal range.

One of the major strengths of the proposed system is its **modular design approach**. Each functional unit—pre-processing, carry computation, correction logic, and sum generation—is implemented as a separate module. This enhances readability, simplifies debugging, and allows reuse in larger arithmetic systems. Furthermore, the hierarchical construction ensures that the 16-bit system can easily be extended to 32-bit or higher digit lengths by adding more 4-bit BCD blocks.

Performance optimization is another important feature of the proposed architecture. By incorporating propagate and generate concepts in carry evaluation, the design reduces critical path delay compared to basic ripple-based BCD adders. The structured carry path shortens propagation time, which improves operational speed. This makes the system suitable for high-frequency digital applications such as calculators, financial processors, digital clocks, and embedded control systems that require accurate decimal operations.

From a hardware perspective, the design is fully synthesizable using standard Verilog HDL constructs. It avoids behavioral arithmetic operators and instead uses structural modeling. Structural modeling provides better hardware transparency and allows designers to optimize gate-level performance. The design can be synthesized onto FPGA platforms for prototyping and later migrated to ASIC implementation for production environments.

Reliability and correctness are also central to the proposed system. The decimal correction mechanism ensures that invalid BCD states are never produced at the output. Since financial and commercial systems depend on accurate decimal arithmetic, maintaining BCD integrity is critical. The explicit correction logic

guarantees that all output digits remain within the valid range of 0000 to 1001.

Scalability is another important advantage. Because the design uses a clear hierarchical framework, additional digits can be supported simply by cascading more BCD adder blocks. This modular scalability reduces redesign effort and supports future system expansion without altering the fundamental architecture.

In summary, the proposed system presents a structured, modular, and efficient approach to multi-digit BCD addition. It combines propagate-generate based carry computation with dedicated decimal correction logic to achieve accurate and high-speed decimal arithmetic. The hierarchical composition from 4-bit BCD units to a 16-bit multi-digit adder ensures scalability, maintainability, and hardware efficiency. The design is well suited for FPGA and ASIC realization, offering a reliable solution for digital systems that require precise decimal computations.

## 4. RESULTS& DISCUSSION

### Simulation Results

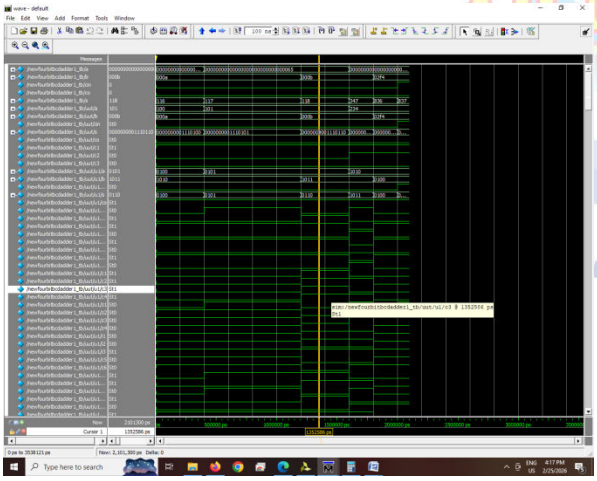

**Figure 4: Simulation Result**

### RTL Schematic

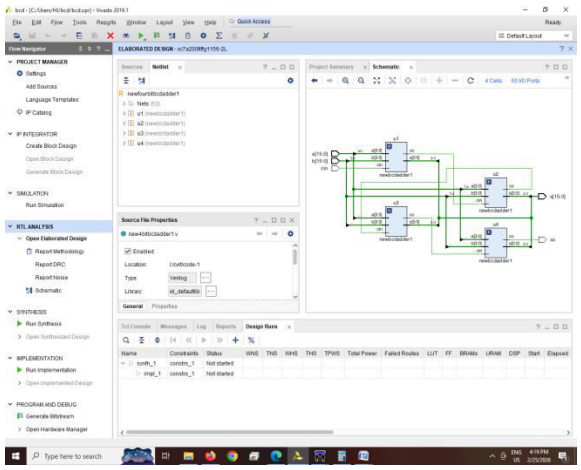

**Figure 5: RTL schematic of adder**

Figure 5 shows the RTL schematic of adder using preprocessing, carry computation and final summation .

### Power Report

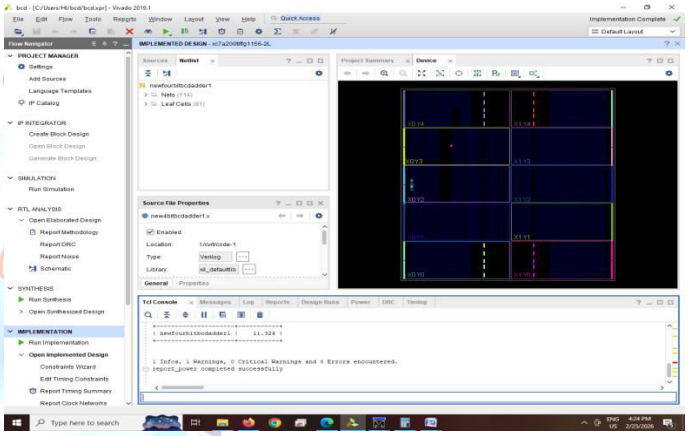

**Figure 6: Power Report**

According to the power report, the adder circuit exhibits a power consumption of 11.324 mW.

### Device Utilization summary:

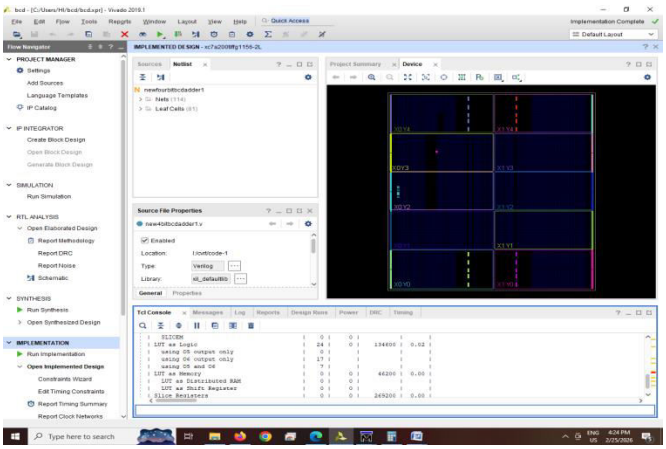

**Figure 7: Area Report**

Figure 7 shows the area report of the adder, where 24 lookup tables are required to perform the operation.

### Timing Summary:

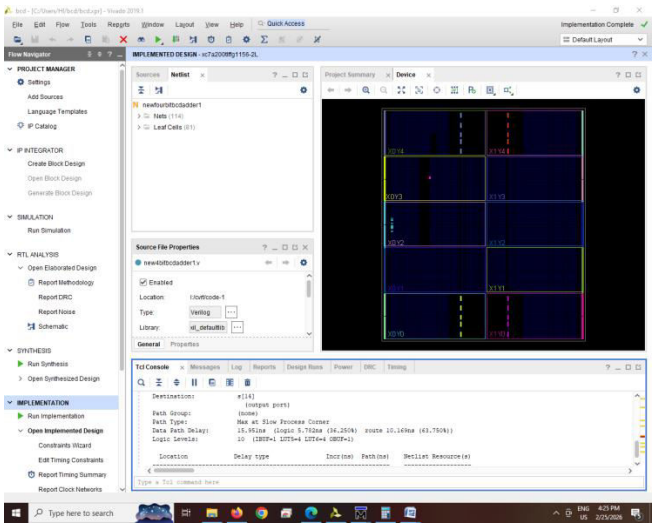

**Figure 8: Delay Report**

Figure 8 shows the delay report of the adder, where the circuit delay is 15.951 ns.

**Table 1: Compression table**

| | EXISTING SYSTEM | PROPOSED SYSTEM |
|---|---|---|
| DELAY | 21.144ns | 11.951ns |
| POWER | 12.879mw | 11.324mw |
| AREA | 23 | 24 |
| SPEED | 47.29mz | 83.67mz |
| PDP | 272.31 | 135.33 |

## 5. CONCLUSIONS

The proposed 4-bit BCD adder system demonstrates significant structural and performance improvements compared to a conventional Ripple Carry Adder (RCA). In an RCA, each bit must wait for the carry from its previous stage before producing a valid output, resulting in linear carry propagation delay proportional to the number of bits. This makes RCA-based BCD addition slower, especially for multi-digit decimal operations. In contrast, the proposed system incorporates propagate–generate logic and structured carry computation blocks to accelerate carry evaluation. By partially optimizing carry propagation within each 4-bit BCD module and applying efficient decimal correction logic, the overall delay is reduced compared to a pure ripple-based design. This makes the proposed architecture more suitable for high-speed arithmetic applications.

Furthermore, while an RCA offers simplicity and lower hardware complexity, it does not inherently address decimal correction requirements efficiently in BCD arithmetic. The proposed system integrates correction detection and adjustment within each modular block, ensuring valid BCD outputs without relying solely on sequential carry rippling. Although the hardware complexity is slightly higher than a basic RCA due to additional logic components, the trade-off results in improved speed, modular scalability, and better suitability for large multi-digit decimal systems. Therefore, compared to a conventional Ripple Carry Adder, the proposed BCD adder architecture provides a more optimized and reliable solution for precise decimal arithmetic in modern digital systems.

### Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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