



# Design and Performance Analysis of Master–Slave D Flip-Flop Using Pass Transistor Logic

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## KEYWORDS

Master-Slave D Flip flop, Pass Transistors, TGFF, PTDF, dual stage DVS

## ABSTRACT

This project presents a novel positive-edge triggered D flip-flop design using pass transistors, aimed at achieving high-speed operation with low power consumption. The proposed architecture employs 12 transistors to implement a compact and efficient flip-flop, reducing propagation delay and energy dissipation compared to conventional designs. A detailed design methodology is presented, covering transistor-level schematics, layout considerations, and timing analysis. The impact of process variations and parasitic capacitances on performance is also evaluated, demonstrating the robustness of the design. The results indicate that the proposed pass-transistor-based flip-flop is highly suitable for low-power, high-performance digital circuits.

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## I. INTRODUCTION

Digital systems increasingly demand storage elements that achieve both high speed and low power consumption, especially as technology continues to scale and operating frequencies rise. Among these storage elements, the D flip-flop (DFF) plays a crucial role in defining the overall timing performance and energy efficiency of synchronous circuits. Conventional DFF designs often suffer from relatively large transistor counts, higher propagation delays, and increased power dissipation, all of which limit their effectiveness in modern low-power applications. As integrated circuits

evolve toward tighter performance and energy constraints, developing more compact and efficient flip-flop architectures has become an essential research focus.

A flip-flop is a fundamental sequential digital logic circuit capable of storing a single bit of binary data (0 or 1). Often referred to as a bistable multivibrator, it possesses two stable states and is used extensively in digital electronics to store state information. Unlike combinational logic, where the output depends solely on current inputs, a flip-flop's output depends on both its current inputs and its prior state. This memory-retaining

ability makes them the essential building block for memory devices, registers, and counters in computers, processors, and various communication systems.

A key characteristic distinguishing a flip-flop from a simpler, level-triggered latch is its "edge-triggered" operation, which means the output changes state only at specific points the rising or falling edge of a clock signal. Common types include the Set-Reset (SR) flip-flop, Data (D) flip-flop, JK flip-flop, and Toggle (T) flip-flop. They are constructed using cross-coupled NAND or NOR gates, allowing them to maintain a specific output state even after the input signals are removed, acting as a crucial element in creating stable and synchronized digital systems.

A Master-Slave flip-flop is a specialized sequential logic circuit designed to store one bit of data, formed by connecting two gated latches (or flip-flops) in series: a "master" and a "slave". Its primary purpose is to eliminate the "race-around condition" found in level-triggered JK flip-flops, where the output toggles multiple times during a single, long clock pulse. In this configuration, the master stage captures the input data during the high phase of the clock, while the slave stage remains inactive. The slave then copies the master's stored data during the low phase of the clock, ensuring that the final output changes only once per clock cycle.

Structurally, the circuit utilizes an inverter on the clock line to ensure that the master and slave are triggered by opposite phases, with the master commonly positive-level triggered and the slave negative-level triggered. When the clock is high, the master reads the input; when the clock goes low, the slave captures that value, creating an edge-triggered behavior. This setup, while more complex, provides highly reliable, synchronized, and predictable operation in sequential circuits, making it crucial for robust data storage.

A D flip-flop, or "Data" or "Delay" flip-flop, is a fundamental sequential logic circuit in digital electronics designed to store a single bit of binary data ((0) or (1)). Unlike simple latches, it is edge-triggered, meaning it only captures the value of the input '(D)' at a specific moment-typically the rising or falling edge of a clock pulse-and holds that value at the output '(Q)' until the next active clock edge. This behavior makes it highly predictable and reliable for storing data and ensuring synchronization within digital systems like registers and counters.

Constructed frequently from a modified SR flip-flop, the D flip-flop eliminates the invalid "Set=1/Reset=1" condition of SR types by connecting the set and reset inputs with an inverter, thus requiring only one "Data" input. It is widely used for temporary data storage, memory, and in complex processors because it ensures the output follows the input directly on the clock edge, while ignoring input changes between clock pulses.

A master-slave positive-edge-triggered D flip-flop is a fundamental digital circuit used in digital electronics and sequential logic design. It plays a crucial role in storing and synchronizing binary information in digital systems. This type of flip-flop is designed to operate on the rising edge of a clock signal, capturing the input data and transferring it to the output on this edge. The master-slave D flip-flop consists of two main stages: the master stage and the slave stage. These stages work together to ensure that the data at the input (D) is captured and stored only when the clock signal transitions from a low (0) to a high (1) level, commonly referred to as a positive-edge transition.

The master stage is responsible for capturing the input data and holding it temporarily until the rising edge of the clock signal. It uses pass transistors to perform this operation efficiently. These pass transistors are activated or deactivated based on the clock signal, allowing or blocking the transfer of data from the input to the internal node of the flip-flop. The slave stage, on the other hand, takes the data captured by the master stage and latches it onto the flip-flop's output, making it available for further processing or as an output signal for other parts of the digital circuit. The slave stage also employs pass transistors to achieve this data transfer.

Pass-transistor logic has emerged as a promising design technique for reducing transistor count and minimizing switching energy in digital circuits. Unlike traditional CMOS logic styles, pass-transistor circuits rely on the direct transfer of logic signals through transistors, which helps lower parasitic capacitances and reduce dynamic power. These characteristics make pass transistors particularly appealing for applications that prioritize speed and energy efficiency. However, careful design is required to address issues such as voltage degradation and signal integrity, which can impact correct functionality.

In this context, the present work introduces a novel positive-edge triggered D flip-flop that employs pass-transistor logic to achieve a compact and power-efficient design. The proposed architecture utilizes only 12 transistors, significantly fewer than conventional DFF structures, without compromising the key performance metrics required for high-speed digital systems. By minimizing the number of transistors involved in data storage and signal transfer, the design reduces propagation delay, switching energy, and overall dynamic power consumption.

A detailed design methodology is presented, covering key aspects such as transistor-level schematics, device sizing considerations, and physical layout strategies. The work also incorporates comprehensive timing analysis to evaluate setup time, hold time, and propagation delay characteristics of the proposed flip-flop. These analyses help demonstrate how the use of pass-transistor logic contributes to speed improvements while maintaining reliable timing behavior. Additionally, the impact of parasitic capacitances—introduced by interconnects and device layouts on performance is assessed to provide insights into practical implementation constraints.

To ensure robustness in real-world conditions, the proposed design is further evaluated under process variations commonly encountered in advanced CMOS technologies. Simulation results show that the flip-flop maintains stable performance across varying device parameters, supply fluctuations, and parasitic effects. Overall, the findings confirm that the pass-transistor-based DFF is a strong candidate for next-generation low-power and high-performance digital circuits, offering an optimal balance between compactness, speed, and energy efficiency.

## 2. LITERATURE REVIEW

In this section, A Master-Slave D Flip-Flop is a fundamental building block in digital integrated circuits, widely used for sequential logic operations. Over the years, extensive research has been conducted to improve performance, reduce power consumption, and enhance the reliability of this key component. Several notable studies and advancements in the field of Master-Slave D Flip-Flops are highlighted here as follows: A NAND based Master-Slave D flip-flop is complex because it requires multiple NAND gates, and careful wiring to ensure proper operation. This complexity can lead to

more significant chances of errors during design and higher manufacturing costs. [1]-[4]. NOR implementation of Master-Slave D Flip-Flop typically consumes less static power compared to NAND-MSDFF. NOR-MSDFF often have limited noise margins, making them more susceptible to signal integrity issues and noise interference, potentially leading to signal glitches and incorrect operation [4]. Static CMOS master-slave D flip-flop are chosen for simplicity and reliability but may not be suitable for power-sensitive or highspeed applications. [5]-[6]. The conventional Transmission Gate Flip-Flop (TGFF) comprises sixteen transistors [9]. To enhance TGFF performance, a Push Pull Flip-Flop (PPFF) design was introduced, inserting Transmission Gates (TG) and inverters between the master and slave sections. Dynamic master-slave D flip-flops rely on charge storage, which can leak overtime due to leakage currents, potentially resulting in data loss if not refreshed, making the design more intricate, and special circuitry may be needed for reliable operation. Adaptive clock gating techniques incorporated in MSDFF [10]. The fine-tuning of these techniques to balance power efficiency and performance can be challenging [8]. Improper configuration of clock gating or power gating control signals might lead to timing issues, reduced reliability in the flip-flop operation. Master-Slave D Flip-Flop using two cascaded JK flip-flops [9] is the increased complexity and resource utilization compared to using D flip-flop implementations. In a Master-Slave D flip-flop with dual-stage dynamic voltage scaling, is the complexity involved due to the dual-stage architecture requires careful synchronization and control logic, which can increase the design complexity and the chances of errors during the design and fabrication process. Additionally, the transition between different voltage levels in the dual-stage DVS[10] can cause glitches and timing issues, especially during the handover between the master and slave stages[11]-[12]. In the High Performance Flip Flop (HPFF), feedback was provided by connecting a PMOS transistor between the output of the slave latch and a specific node in the master latch, resulting in a lower transistor count [13]. Lastly, the static C2MOS Flip-Flop featured C2MOS feedback at the outputs of the master and slave latches, incorporating a total of twenty transistors, making it the largest in terms of area [14]. The proposed design leverages transistors as key elements to achieve a compact and robust flip-flop

architecture of Masterslave D flip-flop and analyses various performance metrics using different CMOS technologies.

### 3. EXISTING SYSTEM

#### Master slave D flip-flop using NAND Gate logic

A master-slave D flip-flop using NAND logic consists of two cascaded D-latches (master and slave), requiring a total of 9 to 11 NAND gates (including an inverter for the clock). The master latch is enabled when the clock is high, while the slave is enabled when the clock is low, creating a negative edge-triggered device where the output (Q) updates only on the falling edge of the clock pulse.

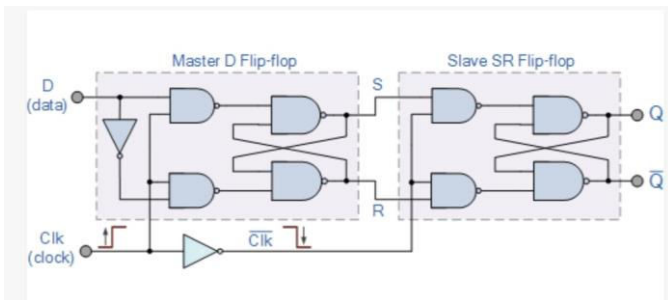


Figure 1: Flipflop using NAND logic

**Key Features and Design Structure:** Two series-connected gated D-latches. The output of the master ( $Q_{\{m\}}$ ) feeds the input of the slave.

**Clocking:** The clock input is applied directly to the master, while an inverted clock signal (via a NAND inverter) is applied to the slave.

**Operation:** Clock = 1 (High): Master is active (transparent), following input (D). Slave is inactive (latched). Clock = 0 (Low): Master is inactive (latched). Slave is active, taking the value of ( $Q_{\{m\}}$ ) and passing it to the final output (Q).

**Logic:** Uses four NAND gates for each latch and additional gates for inverter/control logic.

#### Master slave D flip-flop using transistor gate logic

A Master-Slave D Flip-Flop using transmission gate logic consists of two cascaded D-latches (master and slave) driven by opposite clock phases ( $\text{Clk}$ ) and ( $\overline{\text{Clk}}$ ), typically requiring 16-20 CMOS transistors. When ( $\text{Clk}=0$ ), the master is active (sampling (D)) and the slave holds its previous state.

When ( $\text{Clk}=1$ ), the master holds and the slave passes the data to (Q).

**Transistor Level Implementation Details:** The circuit is implemented using CMOS technology, specifically transmission gates (TG) to minimize transistor count compared to NAND-only gate designs.

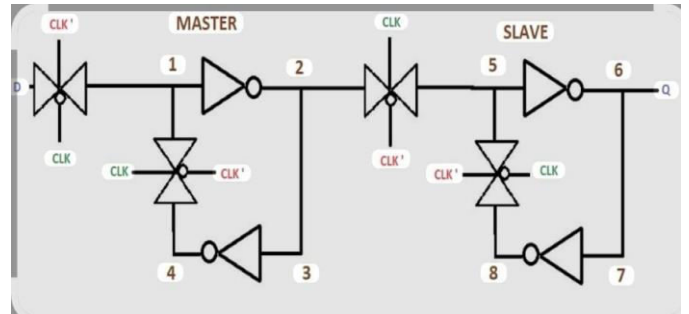


Figure 2: Flipflop using Transmission logic

**Master Latch:** Comprises a transmission gate ( $\text{TG}_{\{1\}}$ ) at the input, controlled by ( $\text{Clk}$ ) and ( $\overline{\text{Clk}}$ ), followed by two cross-coupled inverters to hold the value.

**Slave Latch:** Comprises a transmission gate ( $\text{TG}_{\{2\}}$ ) connected to the master's output, controlled by inverted clock phases, followed by its own set of cross-coupled inverters.

**Clock Inverter:** A simple inverter is used to create the ( $\overline{\text{Clk}}$ ) signal from the ( $\text{Clk}$ ) input.

**Operation Principles Positive Edge Triggering (Rising Edge):** When the clock transitions from (0  $\rightarrow$  1), the master stage ( $\text{TG}_{\{1\}}$ ) turns off, locking in the data ((D)) that was present at the instant of the edge, and the slave stage ( $\text{TG}_{\{2\}}$ ) turns on, transferring this stable data to the output (Q).

**Active High/Low Phases:** During the high phase ( $\text{Clk}=1$ ), the master is in hold mode, and the slave is transparent. During the low phase ( $\text{Clk}=0$ ), the master is transparent (samples input (D)), and the slave holds the previous (Q).

**Signal Flow:** The master-slave configuration ensures that the output (Q) only changes once per clock cycle, specifically on the rising edge, making it an edge-triggered device rather than a level-sensitive latch

### 4. PROPOSED SYSTEM

The Pass transistor logic (PTL) is a type of digital logic that uses transistors as switches to pass logic levels

between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Pass transistor logic has the following characteristics:

A. Reduced Transistor count

Pass transistor logic circuits can use fewer transistors than equivalent CMOS circuits, because transistors are used as switches rather than as inverters.

B. Increased Speed

Pass transistor logic circuits can be faster than CMOS circuits, because pass transistors have lower on-resistance and can switch faster than CMOS transistors.

C. Reduced Power Consumption

Pass transistor logic circuits can consume less power than CMOS circuits, because they have fewer transistors and lower on-resistance.

D. Reduced Noise Immunity

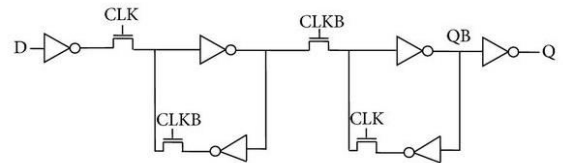
Pass transistor logic circuits have lower noise immunity than CMOS circuits, because the voltage difference between high and low logic levels decreases at each stage. Hence the Pass transistor logic is a versatile type of digital logic that can be used to implement a wide variety of digital circuits. It is well-suited for high-performance and low-power applications.

**4.1 Master-Slave Positive-Edge Trigger using Pass Transistors**

A master-slave positive-edge-triggered flip-flop is a sequential circuit composed of two latches connected in series: the master latch and the slave latch. The master latch captures the input data (D) when the clock signal is low, while the slave latch updates the output (Q) when the clock signal transitions high. This configuration ensures that data is transferred only on the positive edge of the clock, preventing unwanted changes during the clock cycle and providing stable, edge-triggered behavior essential for synchronous digital systems.

When implemented using pass-transistor logic, the flip-flop relies on NMOS or transmission-gate structures that pass signals directly through transistors rather than through full CMOS gates. This approach reduces the number of transistors required, lowers parasitic capacitances, and minimizes switching energy. In the master-slave structure, pass transistors act as controlled switches that open or close based on the clock and its complement, allowing data to move from the master to the slave latch only during specific clock phases. As a result, the circuit provides fast operation with reduced propagation delay.

However, using pass transistors requires careful attention to issues such as threshold voltage drop and signal degradation. Despite these concerns, the master-slave positive-edge-triggered flip-flop implemented with pass-transistor logic achieves a compact, power-efficient design that is well suited for high-speed, low-power digital applications. With proper transistor sizing and buffering, the architecture maintains signal integrity and delivers reliable edge-triggered performance while using fewer transistors than conventional CMOS flip-flops



**Figure 3: Master slave d flip flop using pass transistor**

**4.2 Implementation**

The implementation of the proposed positive-edge-triggered D flip-flop begins at the transistor level, where a 12-transistor pass-transistor-based architecture is designed to achieve compactness and low power consumption. The circuit is constructed using complementary pass transistors to efficiently transfer logic levels while minimizing the number of switching elements. Careful selection of transistor sizes ensures proper signal strength and reduces degradation typically associated with pass-transistor logic.

The next phase focuses on schematic capture and simulation using standard VLSI design tools. The circuitry is modeled to evaluate critical performance parameters such as propagation delay, setup and hold times, and power dissipation. Extensive transient and DC analyses are performed to verify correct functionality under different input conditions. The design is further optimized through iterative simulations to address issues related to threshold voltage drops and potential glitches during clock transitions.

Finally, the layout of the flip-flop is developed with attention to minimizing parasitic capacitances and ensuring symmetry for reliable clocked operation. Design rules are strictly followed to avoid fabrication errors, and post-layout simulations are conducted to assess the impact of interconnect parasitics on timing performance. The results demonstrate that the implemented flip-flop maintains its low-power, high-speed characteristics even when subjected to process variations, confirming its suitability for integration into advanced digital systems.

#### 4. RESULTS& DISCUSSION

Figure 4 shows the circuit diagram of the existing system used for comparison in the project. It represents the earlier design approach, including all components and connections involved in the circuit. The structure reflects a conventional implementation, which may have limitations in terms of power consumption and area efficiency. This diagram serves as a baseline for evaluating the improvements introduced in the proposed system

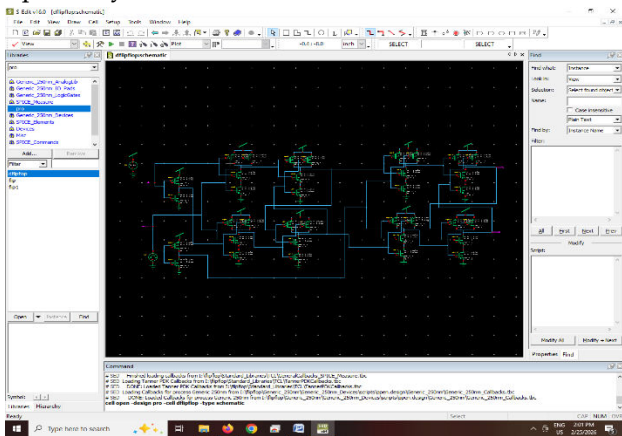


Figure 4: Circuit Diagram of Existing System

Figure 5 presents the simulation waveform of the existing system. It illustrates how the circuit responds to input signals over time. The waveform shows the behavior of input and output signals, highlighting the switching characteristics and operational performance. From the waveform, it can be observed that the existing system performs the required function, but may exhibit slower transitions or higher power usage compared to the improved design

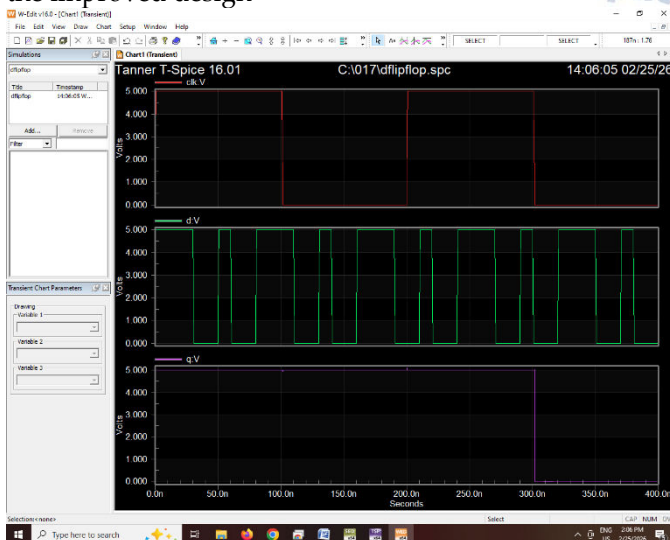


Figure 5: Simulation Waveform of Existing System

Figure 6 displays the power consumption report of the existing system. It provides detailed information about

the amount of power utilized during circuit operation. The results indicate that the existing design consumes relatively higher power, which can affect overall efficiency, especially in large-scale VLSI systems. This serves as an important metric for comparison with the proposed system.

Figure7shows the area report of the existing system, indicating the silicon area occupied by the circuit. A larger area implies increased cost and reduced efficiency in chip design. The existing system occupies more area due to its design complexity and component usage. This highlights the need for optimization in the proposed design.

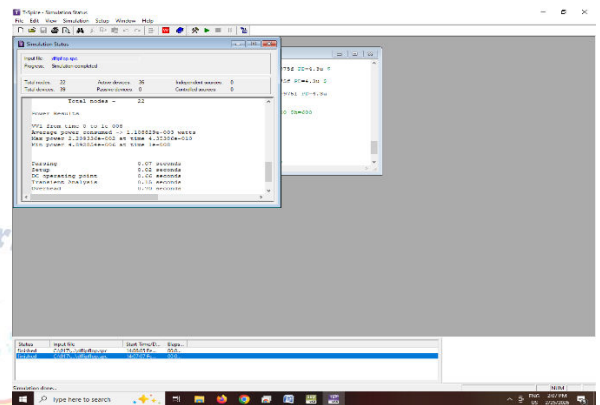


Figure 6: Power Report of Existing System

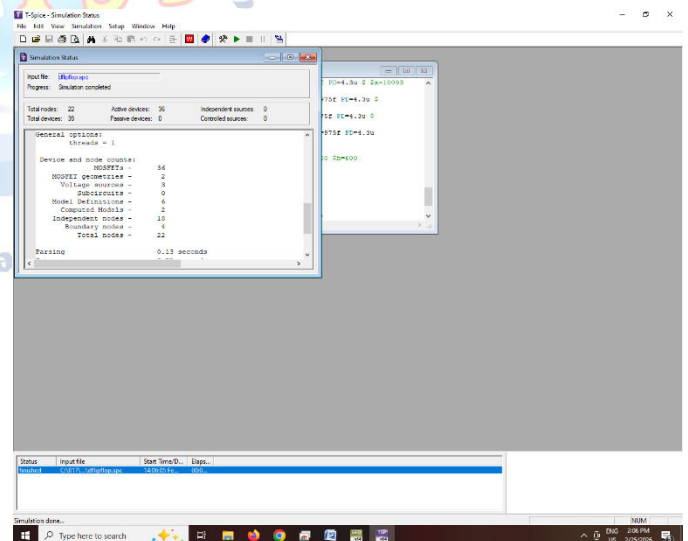


Figure 7: Area report of existing system

Figure 8 illustrates the circuit diagram of the proposed system. The design incorporates improvements over the existing system, aiming to reduce power consumption and area while maintaining or enhancing performance. The optimized arrangement of components and efficient architecture contribute to better overall functionality. This diagram represents the improved version of the circuit developed in the project.

Figure 9 presents the simulation waveform of the proposed system. It shows the response of the improved

circuit to input signals over time. Compared to the existing system, the waveform demonstrates faster switching, stable output levels, and improved performance. This confirms that the proposed design operates efficiently and meets the required specifications.

Figure 10 shows the power report of the proposed system. It indicates a significant reduction in power consumption compared to the existing system. The optimized design ensures energy-efficient operation, making it suitable for modern low-power VLSI applications. This improvement is a key advantage of the proposed system.

Figure 11 presents the area report of the proposed system. It demonstrates that the circuit occupies significantly less area compared to the existing system. The reduction in area leads to lower manufacturing cost and better scalability. This confirms that the proposed design is more compact and efficient.

Table 1 compares the performance of the existing and proposed systems in terms of area and power consumption. The results clearly show that the proposed system achieves substantial improvements. The area is reduced from 36 units to 12 units, and power consumption is decreased from  $1.103 \times 10^{-3}$  to  $5.620 \times 10^{-4}$ . This comparison validates that the proposed system is more efficient, compact, and suitable for high-performance VLSI applications.

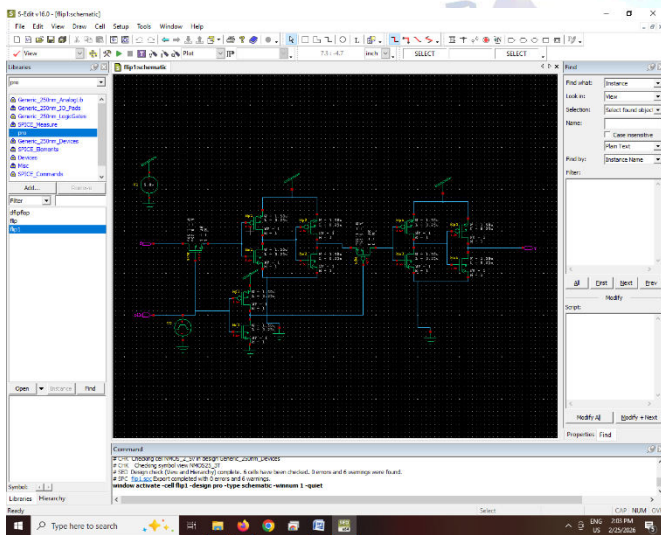


Figure 8: Circuit Diagram of proposed system

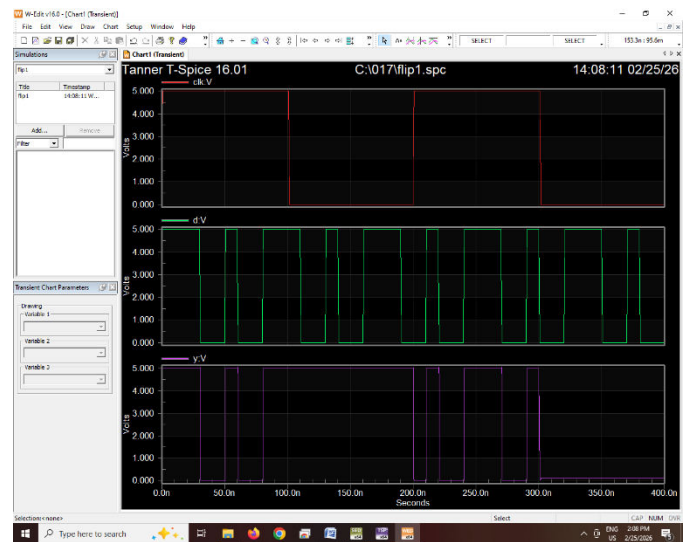


Figure 9: Simulation Waveform of Proposed System

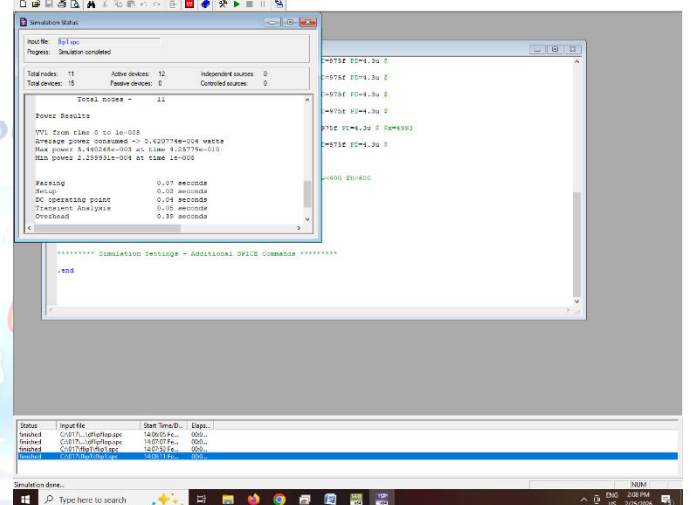


Figure 10: Power report of Proposed System

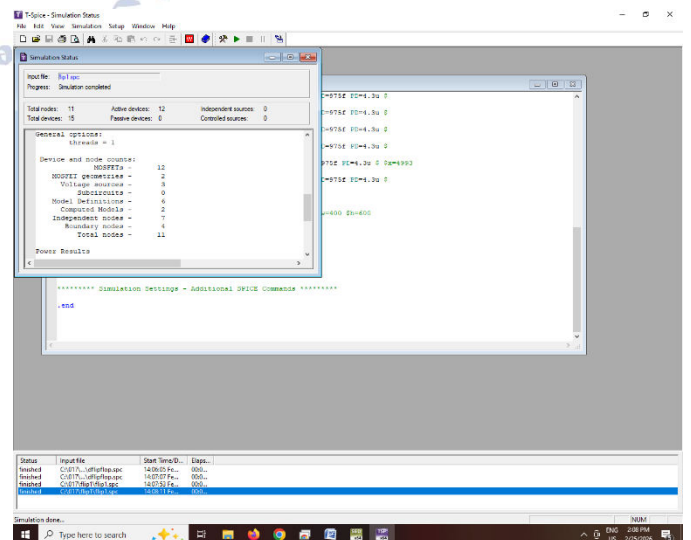


Figure 11: Area Report of Proposed System

Table 1: Compression Table

	Existing System	Proposed System
Area	36	12
Power	$1.103 \times 10^{-3}$	$5.620 \times 10^{-4}$

## 5. CONCLUSIONS

The proposed positive-edge-triggered D flip-flop design successfully demonstrates the advantages of using pass-transistor logic to achieve high-speed and low-power performance. By implementing the flip-flop with only 12 transistors, the design achieves significant reductions in propagation delay, energy dissipation, and overall circuit complexity compared to conventional CMOS-based implementations.

Comprehensive simulations and post-layout analyses confirm that the architecture maintains reliable operation across varying process parameters and parasitic conditions. The results highlight the robustness of the design, particularly in applications requiring efficient clocking and minimal power overhead. Overall, the proposed pass-transistor-based flip-flop presents an effective solution for modern VLSI systems, offering a compact, energy-efficient, and high-performance alternative that is well-suited for next-generation low-power digital circuits

### Future scope

The proposed pass-transistor-based D flip-flop can be further enhanced by exploring advanced transistor technologies such as FinFETs, GAA FETs, or other emerging device structures that offer lower leakage and improved switching characteristics. Implementing the design using these modern technologies could yield even greater speed and power benefits, making the flip-flop suitable for ultra-low-power and high-frequency applications. Future work can also focus on integrating the flip-flop into larger sequential circuits, such as counters, shift registers, and pipeline stages, to evaluate system-level performance improvements. Additionally, incorporating clock-gating techniques or adaptive body-biasing strategies may help further reduce dynamic and static power consumption, increasing efficiency in real-time digital systems

### Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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