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Reliability and Harmonic Performance Analysis of a Reduced Switch Count 15-Level Inverter under Different PWM Strategies

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Total Harmonic Distortion. 1, Phase opposition.2, Phase Disposition. 3, Alternate phase opposition disposition. 4, Pulse width modulation.5

ABSTRACT

Multilevel inverters (MLIs) acquired significant popularity in high-power and medium-voltage applications because of their ability to overcome harmonic distortion and switching voltages to produce high-quality output signals. The study addresses the design development and evaluation of a 15-level low-switch inverter topology employing only 10 active power switches. The proposed design aims to decrease circuit complexity and component count while maintaining good performance in terms of output voltage quality, efficiency, and reliability. The working principle of the suggested inverter is achieved utilizing pulse width modulation (PWM) approaches, particularly Phase Opposition PWM (PD-PWM), Phase Disposition PWM (PO-PWM), and Phase Opposition Phase Disposition PWM (POPD-PWM). A complete Total Harmonic Distortion (THD) analysis is performed for each modulation design to evaluate harmonic performance and waveform quality. The results indicate that the proposed inverter delivers significant reduction in harmonics, with performance comparable to or better than conventional multilevel inverter topologies. Additionally, the reliability assessment is performed considering the reduced number of switching devices, establishing that the proposed design offers a higher reliability through fewer components and reduced probability of failure. A comparative analysis with a typical 15-level inverter design is presented as well, with a focus on critical characteristics such as number of switching's, THD and reliability. Simulation findings support the performance of the suggested design and confirm that high-quality results may be provided with fewer components. The proposed 15-level reduced switching inverter provides a cost-effective, efficient, and robust solution for applications such as renewable energy systems, electric drives, and power quality upgrade, thus fostering the development of

I. INTRODUCTION

The demand for efficient conversion of power has increased in recent times owing to developments in areas like industries, renewable energy, and electric drives [1],[2]. The two-level inverters are mostly used; however, these have certain disadvantages including high THD, increased switching losses, and low quality of output voltages [1],[11]. To address these problems, much attention has been paid on the use of multi-level inverters (MLIs), which have the advantage of producing high-quality output voltage levels along with lower harmonic distortions [2],[13].

A multilevel inverter produces the necessary output voltage from various sources of DC voltage, thereby producing a staircase output which is almost similar to a sinusoidal wave output. The benefit of this approach is that it ensures minimal electromagnetic interference and minimizes dv/dt stress [3],[17]. There exist numerous MLI configurations such as NPC (neutral point clamped), flying capacitors, and cascaded H bridge inverters; however, obtaining more voltage levels with few switches remains an issue [4],[15].

PWM (Pulse Width Modulation) methods have become very important for the control of multilevel inverters because they affect their performance. Out of all these PWM methods, carrier-based PWM methods including Phase Disposition (PD - PWM), Phase Opposition Phase Disposition (POPD - PWM), and Phase Opposition (PO - PWM) have become more popular because of their simplicity [5],[12]. The ordering of carrier signals in these PWM methods affects their harmonic distortions and switching losses [6],[14].

Various research works have been carried out to reduce THD and increase efficiency using advanced modulation schemes and optimal inverter design. Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are some of the widely studied techniques used in multilevel inverters [7][16]. But as the voltage levels increase, the complexity of the circuit increases, and more components are required [8],[18].

The focus of recent studies has been on designing multilevel inverter configurations having fewer switches without compromising on performance [9],[15]. Moreover, the comparative analysis of various PWM techniques plays an important role in deciding the best PWM technique for minimizing THD and obtaining better voltage quality [10],[14].

The proposed study involves the design of a topology for 15 level Multilevel inverter, which makes use of fewer switching components than previous designs. The proposed scheme involves the application of three different PWM schemes; that is PD-PWM, POD-PWM, and POPD-PWM. These PWM schemes have been studied so that good output voltage can be obtained by minimizing harmonic distortions. Further, reliability assessment has been undertaken to ensure the effect of having fewer switches on the overall working of the circuit.[19],[20].

Literature Survey:

Over the past couple of years, there have been numerous studies conducted in the field of MLI due to their ability to produce high-quality voltage output while ensuring minimal distortion. In earlier studies conducted by Tolbert et al. [11], the application of multilevel converters for high power industry applications was emphasized, mainly because of their benefits in lowering switching stresses. In another paper written by Holmes and Lipo [12], an extensive study was made on the PWM technique.

In addition, Rodriguez et al. [13] proposed a wide variety of multilevel voltage source converter topologies suitable for use in industrial medium voltage applications. They showed that more voltage levels result in better outputs, but the circuit becomes complicated. Babaei [15] offered a cascaded multilevel inverter topology that used less switching components, which was the problem with using too many switching devices. Multilevel inverters' performance depends largely on the type of PWM used. Palanivel and Dash [14] evaluated the performance of THD in cascaded multilevel inverters under various types of PWM schemes based on carrier signals. They concluded that PD PWM gives relatively low THD than other PWM schemes. Sirisukprasert et al. [16] extended their research to harmonic minimization and showed that proper modulation can improve inverter performance at various values of modulation indexes.

In this regard, Wu [17] presented an analysis of high-power converters and stressed that it is very crucial to minimize the switching losses for efficient performance of the multilevel inverters. Moreover, Pontt

et al. [18] addressed the issue of elimination of non-characteristic harmonics from cascaded multilevel inverters.

The use of selective harmonic elimination methods has also been considered for improving the inverter system. El-Naggar et al. [19] have used genetic algorithm techniques for minimizing particular harmonic components and obtained better THD results. In addition, Calais et al. [20] have analyzed the use of multilevel converters in solar power generation systems.

From the literature review, it is clear that despite considerable advancement in the design of the multilevel inverters and their PWM controls, problems like the high number of switching devices, complexity, and reliability issues continue to exist. Although various designs with fewer switches have been introduced, finding the best trade-off between the minimal switch configuration, minimizing the total harmonic distortion, and maintaining the reliability of the circuit is one of the open research areas.

Therefore, in this work, an attempt is made to develop a 15-level inverter using fewer switches and using carrier-based PWM methods such as PD-PWM, PO-PWM, and POPD-PWM. This paper evaluates the performance of the developed system based on THD and reliability of the circuit.

II. CONFIGURATION OF THE PROPOSED SYSTEM

The asymmetrical single phase MLI architecture with minimum switches is demonstrated using the schematic representation in Fig. 1. This inverter structure is able to produce 15 output voltage levels utilizing minimum number of switches and DC voltage sources.

The suggested inverter topology comprises 10 switches, out of which 9 are unidirectional switches (S_1–S_3 and S_5–S_{10}), whereas one switch is a redundant bidirectional switch (S_4). The redundant bidirectional switch has been added to the inverter design in order to increase its operational flexibility by providing alternative paths for the current flow through the inverter circuits. In the presented topology, four DC sources with voltage values of 2Vdc, 2Vdc, Vdc, and Vdc have been used which are asymmetrical in nature. The employment of asymmetrical DC sources helps to obtain a larger number of voltage levels using fewer numbers of switches.

In this way, the proposed topology can generate 15 output voltage levels.

These voltages levels can be given as follows: +7Vdc, +6Vdc, +5Vdc, +4Vdc, +3Vdc, +2Vdc, +Vdc, 0, –Vdc, –2Vdc, –3Vdc, –4Vdc, –5Vdc, –6Vdc, and –7Vdc.

It has been seen that the inverter can be classified into two basic sections, level generation section and polarity generation section. The first one generates the needed voltage values using asymmetrical DC sources whereas the second one produces the positive and negative voltages at the load terminals. The load will be connected across the output of the inverter. Since most practical loads including residential and industrial loads are inductive in nature, it is suggested to use RL load for analysis purpose.

Advantages of the topology designed above include the reduction in number of switches, switching losses, fewer gate drivers required, and reliability due to reduced components. Therefore, the topology proposed for design of fifteen-level asymmetrical multilevel inverter is a compact one and also economical in nature.

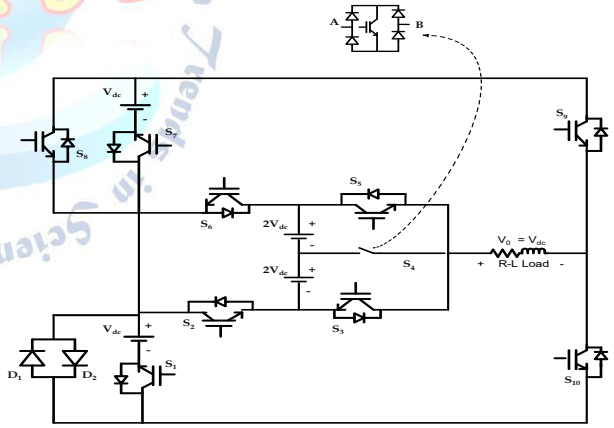


Figure 1 Circuit of a reduced switch Fifteen level inverter

III. OPERATION AND MODULATION TECHNIQUE

From the proposed network the generation of following mode of operations are generated 15 level inverter is discussed below,

Mode 1: S1, S2, S5, and S10 switches are ON, whereas other switches are OFF; then, the output voltage across the load is produced from switching action. Operating characteristics of the active circuit and direction of flow

of current are explained through Figure 2(a).

Mode 2: S2, S5, S8, and S9 switches are ON, whereas other switches are OFF; then, the output voltage across the load is produced from switching action. Operating characteristics of the active circuit and direction of flow of current are explained through Figure 2(b).

Mode 3: S2, S5, S7, and S9 switches are ON, whereas other switches are OFF; then, the output voltage across the load is produced from switching action. Operating characteristics of the active circuit and direction of flow of current are explained through Figure 2(c).

Mode 4: In this mode, switches S1, S2, S4, and S10 will be enabled and all other switches are disabled, and consequently, voltage load is generated by combination of switches actions. Operation of active circuit along with flow of current is shown in Figure 2(d).

Mode 5: Here, switches S2, S4, and S10 are enabled and remaining switches are disabled, and finally voltage load is generated by combination of switches action. Operation of active circuit along with flow of current is shown in Figure 2(e).

Mode 6: In this mode, switches S2, S4, S7, and S9 are enabled and rest of the switches are disabled, and finally voltage load is generated by switches actions. Operation of active circuit along with flow of current is shown in Figure 2(f).

Mode 7: In this mode, switches S1, S2, S3, and S10 are enabled and remaining switches are disabled, and finally voltage load is generated by switches actions. Operation of active circuit along with flow of current is shown in Figure 2(g).

Mode 8: Switches S2, S3, and S10 are made active to enable, and other switches are made inactive; hence, the combination of switches generates the load voltage. The working principle of an active circuit with current flow direction is shown in Figure 2(h).

Mode 9: Switches S5, S6, S7, and S9 are made active to enable, and other switches are made inactive; hence, the combination of switches generates the load voltage. The working principle of an active circuit with current flow direction is shown in Figure 2(i).

Mode 10: Switches S1, S4, S6, and S10 are made active to enable, and other switches are made inactive; hence, the combination of switches generates the load voltage. The working principle of an active circuit with current flow direction is shown in Figure 2(j).

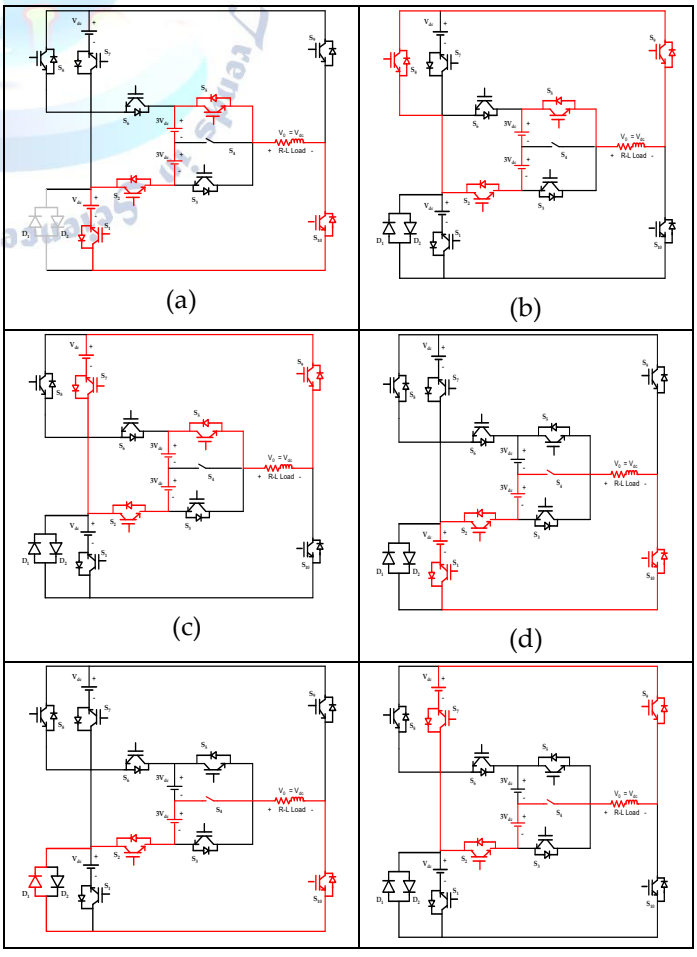
Mode 11: Switches S4, S6, S8, and S9 are made active to enable, and other switches are made inactive; hence, the combination of switches generates the load voltage. The working principle of an active circuit with current flow direction is shown in Figure 2(k).

Mode 12: Switches S4, S6, S7 and S9 are turned on to activate and the rest of the switches are turned off, resulting in the formation of load voltage using the switches' operation. The operation of the active circuit with current direction is shown in Fig. 2(l).

Mode 13: Switches S1, S3, S6 and S10 are activated and the rest of the switches are turned off, resulting in the formation of load voltage using the switches' operation. The operation of the active circuit with current direction is shown in Fig. 2(m).

Mode 14: Switches S3, S6, S8 and S9 are activated and the rest of the switches are turned off, resulting in the formation of load voltage using the switches' operation. The operation of the active circuit with current direction is shown in Fig. 2(n).

Mode 15: Switches S3, S6, S7 and S9 are activated and the rest of the switches are turned off, resulting in the formation of load voltage using the switches' operation. The operation of the active circuit with current direction is shown in Fig. 2(o).



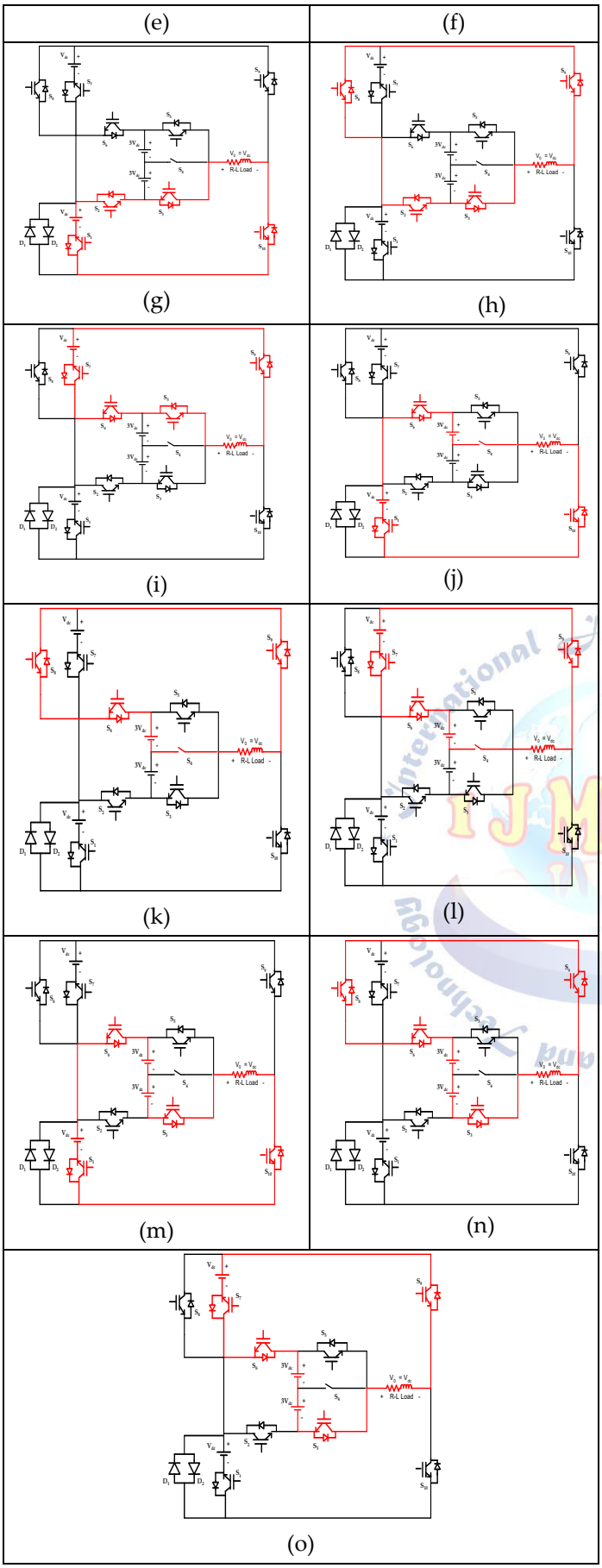
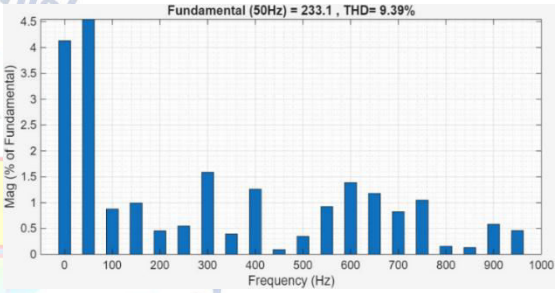


TABLE I: Switching Sequence Table for Multilevel Output

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
7-V_{dc}	H	H	L	L	H	L	L	L	L	H
6-V_{dc}	L	H	L	L	H	L	L	H	H	L
5-V_{dc}	L	H	L	L	H	L	H	L	H	L
4-V_{dc}	H	H	L	H	L	L	L	L	L	H
3-V_{dc}	L	H	L	H	L	L	L	L	L	H
2-V_{dc}	L	H	L	H	L	L	H	L	H	L
1-V_{dc}	H	H	H	L	L	L	L	L	L	H
0	L	H	H	L	L	L	L	L	L	H
-1-V_{dc}	L	L	L	L	H	H	H	L	H	L
-2-V_{dc}	H	L	L	H	L	H	L	L	L	H
-3-V_{dc}	L	L	L	H	L	H	L	H	H	L
-4-V_{dc}	L	L	L	H	L	H	H	L	H	L
-5-V_{dc}	H	L	H	L	L	H	L	L	L	H
-6-V_{dc}	L	L	H	L	L	H	L	H	H	L
-7-V_{dc}	L	L	H	L	L	H	H	L	H	L



The ON (high) state of the switch is denoted by H, and the OFF (low) state is represented by L.

IV. PWM STRATEGIES

A. Phase Opposition (PO – PWM)

The figure 4a shows the Phase Opposition (PO) PWM technique adopted in a 15-level multilevel inverter system. In this case, the carrier waveforms that are above the zero level are in phase with each other. The carrier waves below the zero level are in phase too, but they are 180° out of phase with respect to those above the zero level. Finally, the comparison between the sine waveform and the above mentioned carrier waveforms will result in generation of PWM signals.

With phase opposition between the carrier waveforms, the effective harmonics distribution becomes easy to achieve, which reduces the low-order harmonics content. This results in improved performance of the system and reduction of THD value.

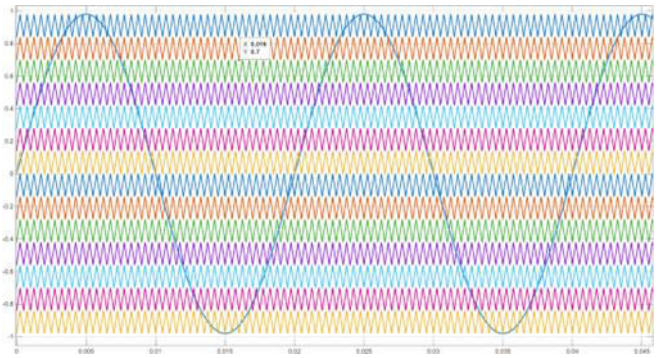


Figure 4a: Phase Opposition Pulse Width Modulation Technique for Carrier Signal Wave Form

Figure 4b shows the harmonic spectrum of the output voltage waveform achieved by applying the PO - PWM algorithm to the suggested multilevel inverter. As indicated by the FFT results, the fundamental frequency is seen to be 50 Hz and the corresponding voltage level is 233.1 V. With regard to the THD, it comes out to be 9.39%, which means that the performance of the inverter with phase opposition control method is satisfactory in terms of harmonic distortion without the requirement for any external filter system. Moreover, it can be said that the lower order harmonics tend to lie between 100 Hz and 400 Hz frequencies, whereas the high order harmonics are situated between 500 Hz and 1000 Hz; however, they have less magnitude compared with the fundamental frequency.

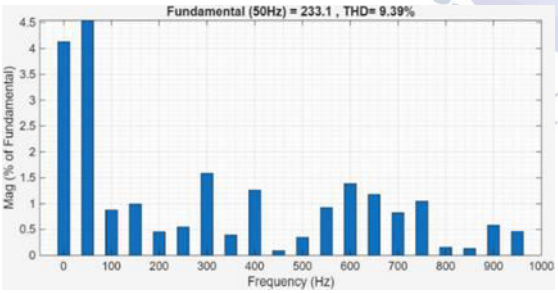


Figure 4b: THD performance of a 15-level inverter using the Phase Opposition PWM Technique.

B. Phase Disposition (PD-PWM)

The Figure 4c shows the operation of the Phase Disposition (PD) PWM scheme applied to a 15-level Multilevel Inverter (MLI). In this PWM scheme, several carrier signals with high frequency are used, which are aligned with each other and spread evenly along the vertical axis. Comparison between the reference sinusoidal signal of low frequency and all the above carrier signals results in the generation of output pulses. Since all the carriers have identical phases, symmetry in switching action is ensured by the PD-PWM technique, resulting in an output waveform of symmetrically stepped form. The use of PD-PWM technique helps in reducing the THD.

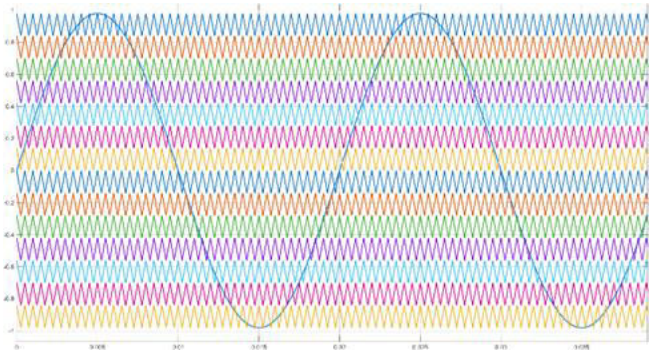


Figure 4c: Phase Disposition Pulse Width Modulation Technique for Carrier Signal Wave Form

Figure 4d shows the harmonic spectrum of the output voltage signal obtained from the PD - PWM. As seen from the analysis of FFT results, the fundamental frequency of this signal is 50 Hz, having an amplitude of 233 V. The value of THD for the output voltage signal is 9.68%, which clearly states the acceptable harmonic performance of the system without the need for any filter circuits. It may be noted that the lower order harmonics fall within the frequency range of 100-400 Hz whereas the high order harmonics fall within the frequency range of 500-1000 Hz. However, the amplitudes of these harmonic components are significantly less compared to that of the fundamental component.

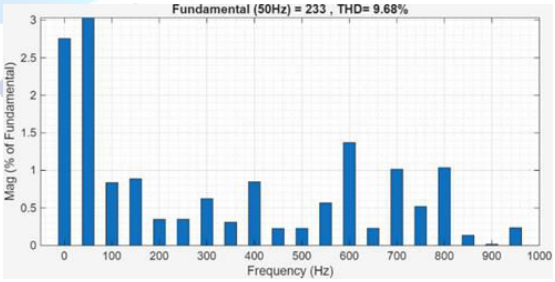


Figure 4d: Phase Disposition PWM Technique shows the THD performance of a 15-level inverter.

C. Phase Opposition Phase Disposition (POPD – PWM)

The figure 5a explains how the Phase Opposition Phase Disposition (POPD) PWM control algorithm operates for a multilevel 15 level inverter. According to the control algorithm, the carriers should be positioned in a way that makes carriers lying above the zeroaxis phase coincident while those lying below the zero axis should be 180o out of phase from the former ones. A

sinusoidal reference signal is then used to generate pulses by comparing itself with the carriers. Such an arrangement leads to phase opposition between the two sets of positive/negative carriers, hence better harmonics distribution.

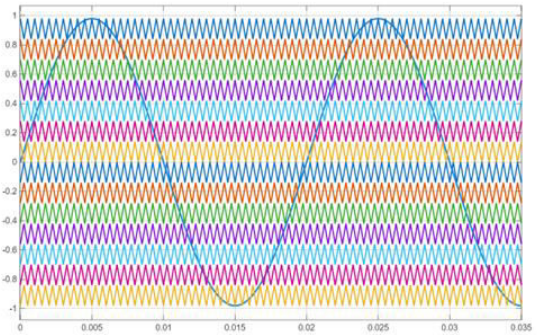


Figure 5a: Phase Opposition Disposition Pulse Width Modulation Technique for Carrier Signal Wave Form

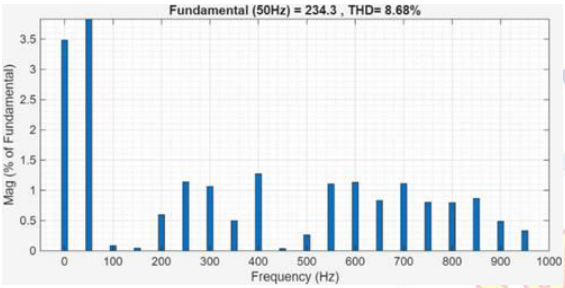


Figure 5b: THD performance of a 15-level inverter using the Phase Opposition disposition PWM Technique

Figure 5b displays the harmonic spectrum of the output voltage waveform that is generated using the proposed multilevel inverter system of POPD - PWM. Based on the results of FFT analysis, it has been determined that the fundamental sinusoid has a frequency of 50 Hz and an amplitude of 234.3 V. The THD ratio of the signal is calculated to be 8.68%. That's enough to eliminate harmonics from the multilevel inverter without filters. It is clear that the occurrence of low-frequency harmonics is in the range of 100-400 Hz, whereas that of high-frequency harmonics occurs beyond 1000 Hz. However, their amplitudes are significantly lower than those of the fundamental frequency.

V. ANALYSIS OF OBTAINED SIMULATION RESULTS

The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

A. 15 level output voltage waveforms

The waveforms of the developed 15-level multilevel inverter have been illustrated in Figure 5a. Due to several voltage levels, the waveform of the load voltage has been illustrated in the upper part of the figure. According to the graph, it is clear that the waveform consists of steps and is of sinusoidal shape. The development of 15 voltage levels reduces the value of the THD in the waveform.

The load current waveform, which also follows a sinusoidal shape, has been provided in the lower part. The reason for the provision of such a sinusoidal waveform of current is the presence of filtering due to the effect of the load inductance in the stepped load voltage.

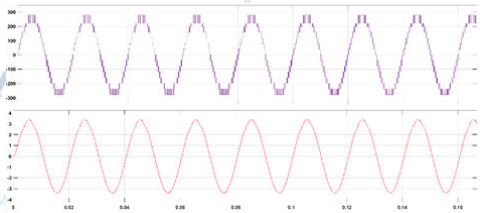
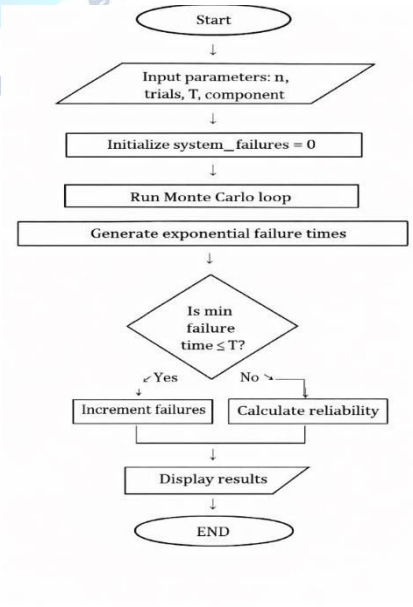


Figure 5a: Output Voltage and Reference Sinusoidal Waveforms of 15-Level Inverter

B. System Reliability Analysis

1. Monte Carlo Simulation for Reliability Assessment



Flow Chart

2. Mathematical Modeling for Theoretical Reliability Evaluation

RELIABILITY ANALYSIS:

Reliability is defined as the probability that a system performs its intended function without failure over a specified time interval, and it can be mathematically expressed as:

$$R(t)=e^{(-\lambda t)}$$

Where:

R(t) = Reliability

λ(t)= Failure rate (failures/hour)7

T = Time in hours

COMPONENT	COUNT(n)	FAILURE RATE (λ/HOUR)
SWITCHES	10	0.001
CAPACITORS	0	0.005
DIODES	2	0.003

a. **Capacitors Count**

Capacitors count is 0, so they do not affect reliability.

b. Reliability of an Exponential Component

For exponential failure distribution:

$R(t) = e^{(-\lambda t)}$

c. Reliability of Multiple Identical Components (Series)

For n identical components in series:

R(t) = e(−λt))n

or

R(t) = e(−nλt)

d. System Reliability

Rsystem = e(−((10*0.001)+(2*0.03))*10)

Rsystem = e^(−0.16)

Rsystem = 0.8520

% Rsystem = 0.852*100= 85.2%

e. Failure Probability

Pf = 1 − Rsystem

Pf = 1 – 0.8520

Pf = 0.1480

% Pf = 14.80%

TABLE 2: Reliability and Failure Probability Comparison

Topology	No. of Components			Reliability		Failure Probability	
	S	D	C	**Monte carlo**	**Mathematical modelling**	**Monte carlo**	**Mathematical modelling**
Proposed Topology	10	2	0	85.4	87.81	14.34	12.19
[21]	11	4	0	79.64	86.8	20.36	14
[22]	13	0	1	83.18	83.4	16.82	16.6

In Table 2 we have switches. These are shown by the letter S. We also have diodes and these are shown by the letter D. Then there are capacitors. These are shown by the letter C.

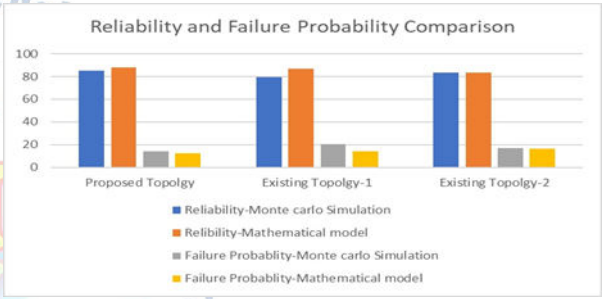


Figure 5b :Reliability and Failure Probability Comparison

It is clear from the above bar chart shown in Fig. 5b that there has been a comparative analysis conducted for the reliability and probability of failure for the topologies mentioned above, including the Proposed Topology, Existing Topology-1, and Existing Topology-2 by using two methods, namely Monte Carlo simulation and mathematical modeling method. From the above chart, it can be seen that the Proposed Topology has demonstrated better reliability of about 85% to 88% by using both Monte Carlo simulation and mathematical model, but on the other hand, the probability of failure has been found to be 14% to 12% for both cases. Similarly, for the Existing Topology-1, it is evident that the reliability factor of the topology is very low, i.e., 80% to 87%, however, the probability of failure is quite high, i.e., 15% to 20%.

C. Parameters Required for the Simulation

Parameter	Value
Input Voltage	(V_{dc}, V_{dc}, $2V_{dc}$, $2V_{dc}$)
Voltage Levels	(50 V, 50 V, 100 V, 100 V)
Reference Signal Frequency	50 Hz
Switching/Carrier Signal Frequency	4 kHz
Load Resistance (R)	80Ω
Load Inductance (L)	50mH
Modulation Index	0.98

Table 3: Comparative Analysis of Topologies

Components	P T**	[21]	[22]
No. of Switches	10	11	13
No. of DC Sources	4	4	1
Diodes	2	4	0
Capacitors	0	0	1
THD	8.68	11.93	9.68
Reliability	0.856	0.796	0.833

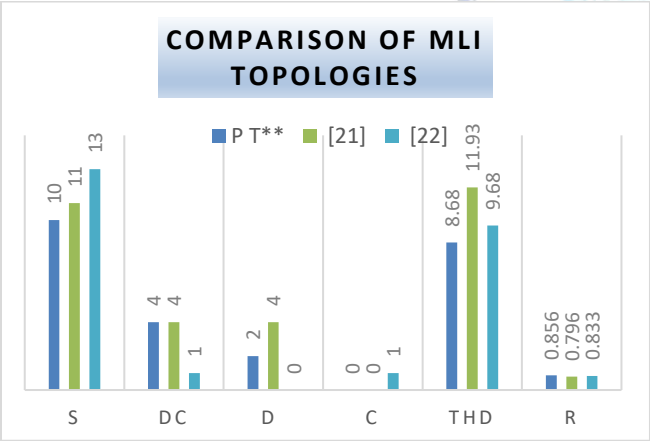


Figure 5c : Comparison of MLI Topologies

In Fig 5c, DC = DC sources, S = switches, D = diodes, C = capacitors, THD = total harmonic distortion, R – reliability.

Fig. 5c presents the comparison between the existing and proposed multilevel inverter topologies in terms of number of components, total harmonic distortion, and reliability. The proposed topology provides the advantages of having less switches and higher reliability with comparable harmonic characteristics.

VI. CONCLUSION

In this paper, the reliability analysis and harmonic performance of a reduced switch count 15-level inverter were analyzed under different PWM control schemes. In this topology, there are only ten active switches used which make the circuit design more simplified and help reduce costs. In the implementation of different control techniques like PD-PWM, PO-PWM, and POD-PWM, it has been proved that the inverter is able to generate good quality output voltage. In the Total Harmonic Distortion (THD) analysis section, it was shown that the designed topology shows good harmonic characteristics which are equal to or better than other traditional multilevel inverter configurations. Moreover, in the reliability analysis section, it has been proved that the reduction in the total switching components improves the system reliability due to fewer chances of failure. From the comparison section, it can be concluded that the designed inverter is having an effective combination of both performance and reliability. On the whole, from this analysis, it can be stated that the proposed topology of the inverter is efficient as well as a cost-effective solution.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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