



# Low Power, High Performance and Area Efficient 2-4 and 4-16 Decoders Design Using Modified Gate Diffusion Input (M-GDI) Technique for SRAM

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### KEYWORDS

Decoders, Low power Design, VLSI, Modified GDI · Mixed logic.

### ABSTRACT

This paper introduces the design of 2-4 and 4-16 line decoders using modified version of gate diffusion input (M-GDI) technique as it reduces the area that is the number of transistors and also it reduces the dissipation of power. The Combinational circuits like decoders which are used in the periphery circuitry of memory arrays like Static RAM are designed by using Modified Gate Diffusion Input (M-GDI) technique which eradicate the disadvantages of the pass transistor logic (PTL) and CMOS logic. The decoders which are designed using modified GDI technique offer better characteristics in terms of average power and delay, and also the transistor count is reduced compared to the decoders which are designed using mixed logic technology which are static CMOS, pass transistor logic and transmission gate logic. Finally, the decoders which are designed by using two techniques in 90 nm technology using Tanner T-Spice/S-Edit compared in terms of transistor count, average power, delay and power delay product (PDP) show an improvement when compared to the decoders of mixed logic.

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## 1. INTRODUCTION

In modern age, the main considerations are area, speed and power which are the important parameters for increasing demand for low power and the design of electronic circuits needs to be compatible with

minimized chip area which are handheld devices like mobiles, laptops, palmtops, wireless modems and remaining electronic devices.

A 2-4 decoder has two inputs A and B, and it generates its output D0-3 based on its logic operation. Depending

on the input combination A and B in non-inverting decoder, one of the four outputs (minterms) D0-3 is selected and is set to '1' and rest are set to '0'. Similarly, inverting 2-4 decoder generates the complementary

outputs I0-3; that is, selected output is set to '0' and the rest are set to '1'. Similarly, 4-16 decoders have 4 inputs and 16 outputs (minterms) generated based on the logic operation.

There are many efficient design styles suitable for the advancements in the VLSI technology; some of them are CMOS, PTL, gate diffusion input (GDI) techniques, etc. Among them, the gate diffusion input (GDI) designs the digital combinational circuits with less area, i.e., minimum transistor count and reduced power (low power), reduced propagation delay which overcomes the demerits of CMOS, PTL and other designing technologies [1]. It only uses two transistors for the implementation of logic gates.

GDI consists of three inputs G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS). The bulks of PMOS and NMOS are connected to N and P, respectively [2]; in the case of bulks, the fabrication of GDI cell is not possible in P well because when the bulk is connected to the drain, threshold voltage is increased and when in the case bulk is connected to the source the body effect is destroyed according to the threshold voltage equation so we have an alternate approach that is the modified GDI (M-GDI) in which bulks are not connected to respective drain/source [3] which is derived from GDI in order to eliminate the body effect and threshold voltage effects.

Modified Gate Diffusion Input (M-GDI) technique, highlighting reduced transistor count, power consumption, delay, and improved power-delay product (PDP) over mixed logic implementations.

## 2. RELATED WORK

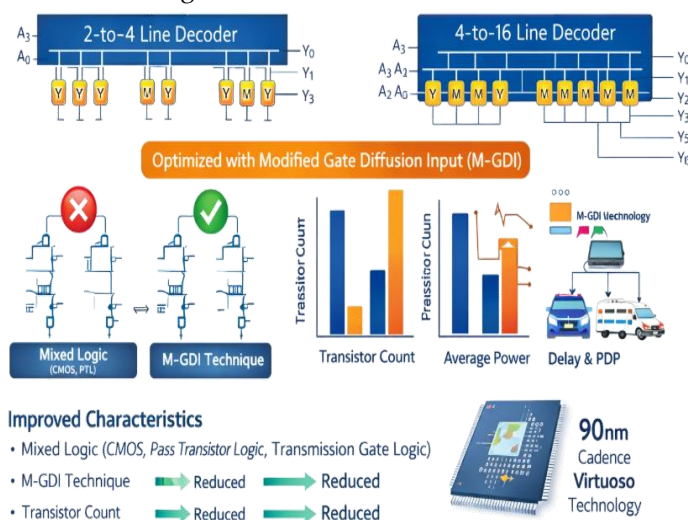
Recent advancements in intelligent transportation systems have focused on improving vehicle safety, monitoring, and detection using computer vision, machine learning, and IoT technologies. Several research studies have explored different techniques for vehicle detection, tracking, and accident monitoring in order to enhance road safety and traffic management.

Deep learning-based object detection algorithms have become widely used for vehicle detection in intelligent transportation systems. Vinoth and Sasikumar proposed a lightweight object detection approach optimized for low-light conditions using pixel-wise depth refinement and TensorRT optimization to improve detection performance and computational efficiency [1]. Similarly, Vellaidurai and Rathinam introduced a modified YOLOv5-based model for vehicle detection and classification under adverse weather conditions, which improves accuracy in challenging environments such as rain and fog [2]. Tahir et al. further extended this approach by proposing the PVDM-YOLOv8l model, which enhances pedestrian and vehicle detection reliability for autonomous driving systems [3].

Low-power and high-performance digital circuit design has become a major research focus in modern VLSI systems. Various techniques such as Gate Diffusion Input (GDI), pass transistor logic, and optimized CMOS architectures have been proposed to reduce power consumption, delay, and area in digital circuits.

The Gate Diffusion Input (GDI) technique was first introduced by Morgenshtein et al. in [1], where the authors proposed a power-efficient method for implementing digital combinational circuits. The GDI technique reduces transistor count and power consumption compared to conventional CMOS logic, making it suitable for low-power VLSI applications. In a further study, Morgenshtein et al. [2] analyzed and characterized the GDI technique in detail and demonstrated that it provides significant improvements in terms of area efficiency and switching power reduction in digital logic implementations.

Several researchers have extended and improved the



**Figure 1** Conceptual design and performance comparison of 2-to-4 and 4-to-16 line decoders using the

original GDI concept. Soni and Shah [3] presented a review of modified GDI techniques aimed at improving logic functionality and reducing design complexity. Their work highlighted how modified GDI structures can overcome some limitations of the basic GDI approach, such as reduced voltage swing and fabrication constraints.

Decoder circuits are also an important component in many digital systems, and efforts have been made to design low-power decoder architectures. Balobas and Konofaos [4] proposed low-power and high-performance mixed-logic decoders such as 2–4 and 4–16 decoders. Their work demonstrated that combining different logic styles can significantly improve performance and reduce energy consumption in decoder circuits.

Transmission switch theory has also played an important role in digital circuit design. Wu [5] presented a theoretical framework for transmission switches and demonstrated their application in CMOS digital circuits. This work provided a foundation for implementing efficient switching structures in modern VLSI systems.

The fundamentals of CMOS VLSI circuit design are extensively discussed by Weste and Harris in [6], which provides a comprehensive overview of CMOS design methodologies, power optimization techniques, and circuit-level implementation strategies used in modern integrated circuits.

Another important approach to reducing power consumption is pass transistor logic. Oklobdzija and Duchene [7] introduced pass-transistor dual value logic, which enables the implementation of low-power CMOS circuits with reduced transistor count and improved switching efficiency.

Further advancements in GDI logic were explored by Morgenshtein et al. [8], where the authors demonstrated the implementation of GDI logic in standard CMOS nanoscale processes. Their work showed that the technique can be successfully integrated into modern fabrication technologies while maintaining low power consumption and high performance.

In addition to logic circuit design, efficient arithmetic architectures are also essential in VLSI systems. Dake and Terlapu [9] proposed a high-throughput digit-serial redundant basis multiplier architecture over finite fields, demonstrating improved computational efficiency in digital signal processing applications.

Similarly, Gali and Terlapu [10] implemented VLSI architectures for FM0 and Manchester encoding schemes used in short-range communication systems. Their design focused on optimizing hardware resources while maintaining reliable data transmission performance.

Overall, these studies highlight the importance of developing efficient logic design techniques such as GDI, pass transistor logic, and optimized CMOS architectures to achieve low-power and high-performance digital systems.

### 3. PROPOSED SYSTEM

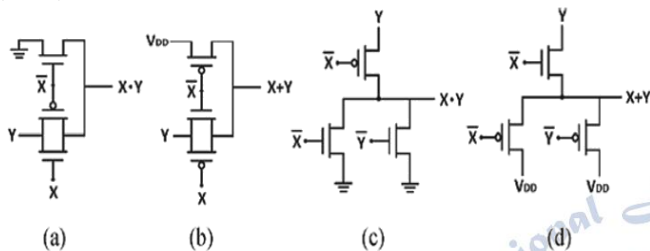
The combinational circuits like decoders can be designed by using different logic styles; the transistor count may defer in case of decoders designed by using the conventional CMOS; the 2-4 decoder takes 20 transistors; taking 2-4 decoder as predecoder, then we design the 4-16 decoder; it takes 104 transistors for the design using CMOS NAND and NOR gates. The circuits that are designed using mixed logic [4] exhibit good performance when compared to the circuits designed using the single logic. The existing decoders are designed by using the mixed logic style which is a combination of transmission gate logic (TGL) [5], static CMOS [6] and dual value logic (DVL) [7] which combines the advantages of the above three logic styles.

Transmission Gate Logic (TGL) is same as relay that conducts in both directions, and is also a CMOS based switch which is used to implement electronic switches and analog multiplexers. It reduces the noise margin and static power dissipation caused because of increased threshold voltage, but it requires control signal and its complement; generally, the clock signal is used as control signal. TGL implements logic gates, AND/OR gates; thus, the gates are used to design the decoders that gates are full swinging.

Static CMOS is logic circuit designs which have pull-up network which contains PMOS transistors and pull-down network which contains NMOS transistors which gives good performance and resistance to noise. In static CMOS, the operating voltages are low and small transistor sizes and inputs are connected to the gate terminal of transistors; thereby, the designing becomes easy. It generates the output levels as long as the power supply is provided and consumes less power.

Dual value logic (DVL) is one of the pass transistor logic (PTL) circuit techniques, and it is derived from the

double pass transistor logic (DPL) with the main objective of speed improvement and power consumption [8]. Dual value is obtained from the double pass transistor logic by elimination of redundant branches present in the circuit, and there is rearrangement of signals in the circuit of DPL. The DVL gates have full swinging with less transistors and it uses both NMOS and PMOS transistors with good speed of operation. Among the pass transistor logic design styles, DVL is more advantageous over conventional CMOS, double pass transistor logic (DPL), complementary pass transistor logic (CPL) and double pass transistor logic (DPL).



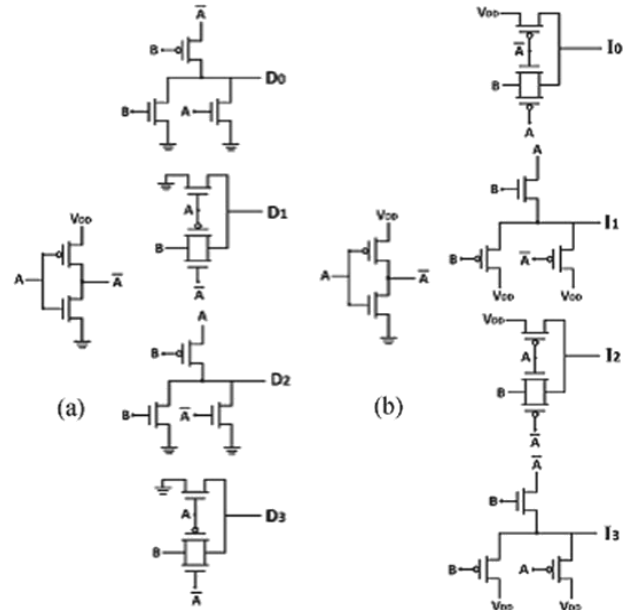
**Figure 2** a. TGL AND gate. b. TGL OR gate. c. DVL AND gate. d. DVL OR gate.

The above shown gates in Fig. 2 which are designed by using TGL and DVL both have the inputs X and Y which are applied at gate terminals. In TGL gates, input X is the control signal to the gates of three transistors and Y propagates output through the transmission gate. In DVL gates, input X is the control signal of two transistor gates and Y controls one transistor gate and propagates the output through the pass transistor [9, 10]. Hence, X and Y signals are considered as control and propagate signals, respectively. When we use inverted input as a propagate signal is not a good practice because it has some disadvantages, so an inverter is added to the propagation path which further increases the delay, respectively [4].

### A. Transistor 2-4 Decoder

The 2-4 decoders can be designed by using TGL or DVL gate as it takes 16 transistors which includes 12 AND/OR gates and 2 inverters. By using some proper signal arrangement, we can eliminate one of the two inverters A or B; therefore, decoder can be designed by using 14 transistors shown in Fig. 3. The first minterm  $D_0 = \bar{A}B$  and the third minterm  $D_2 = A\bar{B}$  can be implemented by using DVL logic, and the second and fourth minterms  $D_1 = A\bar{B}$  and  $D_3 = A\bar{B}$  can be implemented by using TGL logic. For  $D_0$  and  $D_2$ , A is the propagate signal, and for  $D_1$  and  $D_3$ , B is the propagate signal; this eliminates the

inverter B. Hence, the 14-transistor decoder consists of 9 NMOS and 5 PMOS for non-inverting decoder.



**Figure 3** 14 transistor low-power 2-4 decoder. a. 2-4 LP. b. 2-4 LPI

Similarly for the inverting decoder which is designed by using OR gates which is of 14 transistors topology consists of 5 NMOS and 9 PMOS. Same as non-inverting decoder, here also  $I_0$  and  $I_2$  minterms are implemented with TGL gates and  $I_1$  and  $I_3$  minterms are implemented with DVL gates. For  $I_0$  and  $I_2$ , B is the propagate signal, and for  $I_1$  and  $I_3$ , A is the propagate signal. By the elimination of inverter B, there is reduction of two transistors, logical effort, switching activity and also power dissipation. Here, we have two new topologies which are 2-4 LP and 2-4 LPI, I for invert.

In the 2-4 LP and LPI decoder, there is a drawback of worst-case delay because the complementary signal A is used as propagate signal for  $D_0$  and  $I_3$  minterms. So to overcome this, we can implement the minterms  $D_0$  and  $I_3$  using static CMOS gates.  $D_0$  is implemented with CMOS NOR, and  $I_3$  is implemented with CMOS NAND gates. Due to the addition of one transistor to the 14 transistor topology Decoder then this results new topology 15 transistor is obtained which has the advantage of delay but there is slightly there is increase in power.

Similarly as 14 transistor topology, 15 transistor topology also has two topologies called 2-4 HP and 2-4 HPI shown in Fig. 4. Hence, 15 transistor topology decoder is called high-performance decoder. Similarly, 4-16 decoders can be designed by using 2-4 decoders but when we cascade the PTL circuits it cannot give good

performance due to poor driving capability so we can design 4-16 by using PTL and CMOS [8] combination instead of using mixed topology.

4-16 decoders are implemented with 2-4 decoder as pre-decoder combines with CMOS NOR or NAND gates which produce the decoded output. As 2-4 decoders have 4 new topologies, 4-16 decoders also have 4 new topologies as shown in Fig. 5, namely 4-16LP, 4-16LPI, 4-16HP and 4-16HPI. In case of 4-16, the transistor count decreases from 104 to 92 in case of low power (LP) and 94 in high performance (HP).

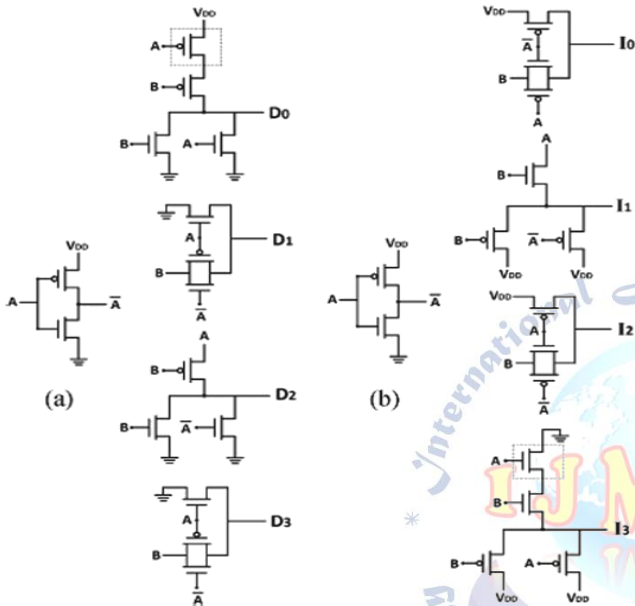


Figure 4 15 transistor high-performance 2-4 decoder. a 2-4 HP. b 2-4 HPI

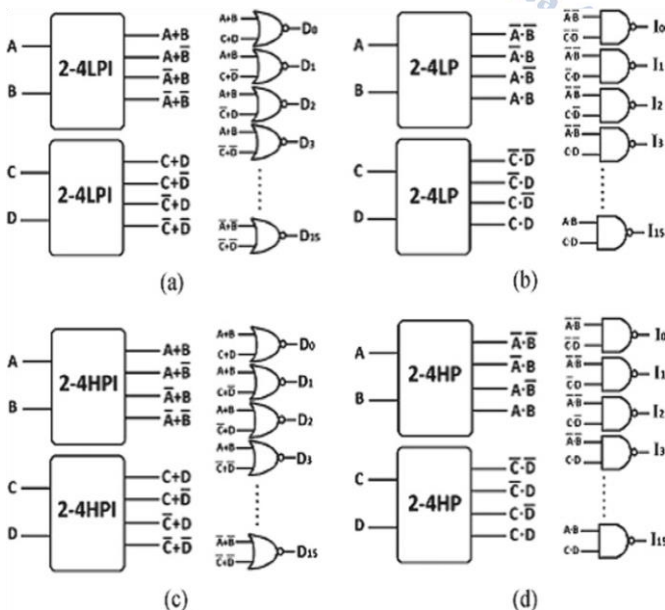


Figure 5 4-16 decoders. a 4-16 LP. b 4-16 LPI. c 4-16 HP. d. 4-16 HP

#### 4. METHODOLOGY

The proposed design is the modified GDI decoders which have minimum transistor count and consume less power and high speed when compared to the decoders designed using mixed logic. The GDI logic has the drawback of bulk issue in fabrication process which uses twin tub or silicon on insulator (SOI). This increases the complexity of the design as well as cost of fabrication then to overcome the above drawbacks the decoders designed using modified GDI designed using Modified GDI AND gate, Inverters and Modified GDI OR gates all the set here gates can be designed using only two transistors.

The above gates in Fig. 6 are the modified GDI AND and modified GDI OR gates used in the design of the decoders. The operation of the modified AND gate is given as an example. In the AND gate, the drain terminal of PMOS is connected to input A and source terminal of NMOS is connected to input B. Both the gate terminals of PMOS and NMOS are connected to input A. When the two inputs are low (0), PMOS operates in linear region and NMOS is in cutoff region. When A = high (1) and B = low (0), the PMOS is in cutoff region and NMOS is in linear region. When A = low (0) and B = high (1), then PMOS is in linear region and NMOS is in cutoff region. When the two inputs are '1', then both PMOS and NMOS are in linear region and they produce the output as '1'.

Here Fig. 7 non-inverting decoder designed using four OR Gates and two inverters that are 12 transistors are required to design and also for inverting decoder requires Mod-GDI AND Gates and two inverters that is 12 transistors are required when compared to the existing decoders 3 transistors reduced in case of 2-4 HP and HPI, similarly 2 transistors are reduced in case of 2-4 LP and LPI. Taken 2-4 decoder as pre-decoders, 4-16 decoders are designed. Finally, the proposed decoders have the reduced transistor count, low power and high speed.

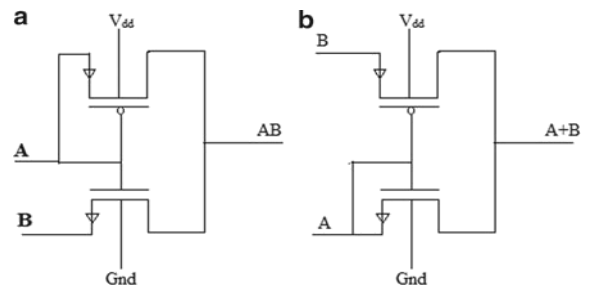
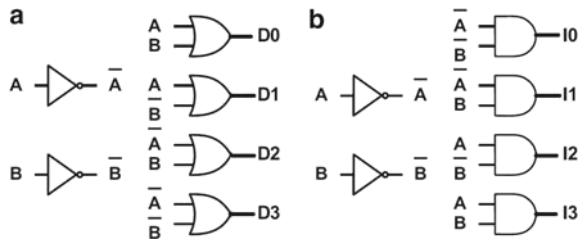


Figure 6 Modified GDI AND gate. b Modified GDI OR gate



**Figure 7** 2-4 modified GDI OR-based decoder. b 2-4 modified GDI AND-based decoder.

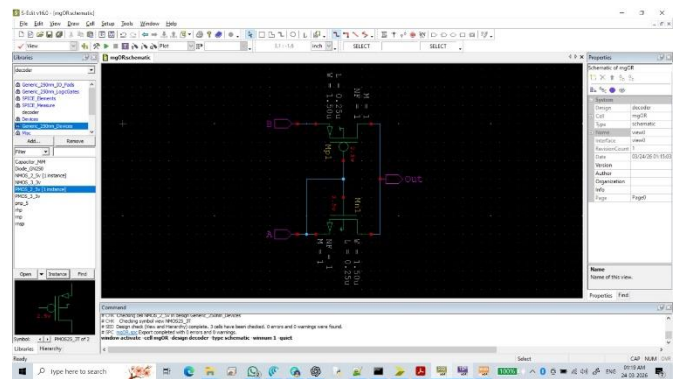
### 5. RESULTS AND DISCUSSIONS

The decoders of conventional CMOS, mixed logic and modified GDI are compared with transistor count, average power, delay and the power delay product (PDP). All the results are simulated using Tanner Tools 90 nm CMOS technology. The power delay product (PDP) is defined as the product of average power and delay which is used to determine the performance of the digital circuits. Simulation results are performed in Tanner Tools 90 nm CMOS technology.

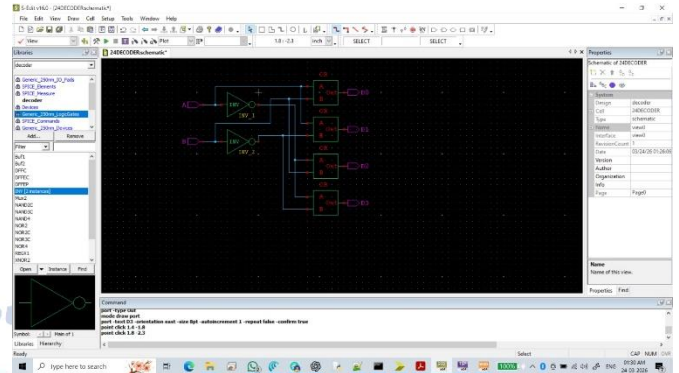
Table 1 gives the information about the average power dissipation of 2-4 decoders and similarly Table 2 about the 4-16 decoders. Table 3 gives the information about the delay of all the decoders discussed above, Tables 4 and 5 about the power delay product (PDP) of all the decoders Table 6 about the transistor count of the 2-4 and 416 decoders designed using the mixed logic, modified GDI and conventional CMOS. All the decoders are simulated at supply voltages 0.8, 1 and 1.2 v with time period 2, 1 and 0.5 ns.

**Table I** Delay results (in ns)

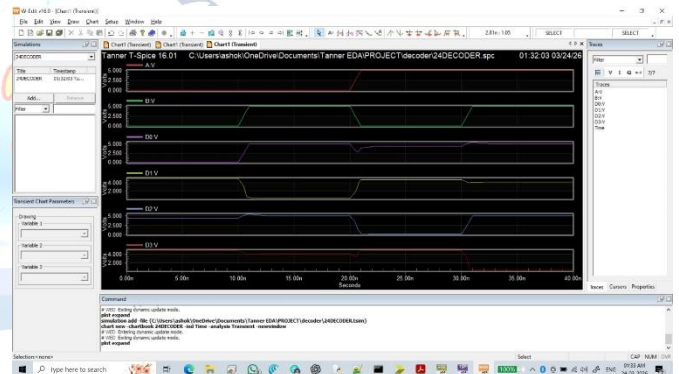
2-4 decoder	Delay (ns)	4-16 decoder	Delay (ns)
NOR-based decoder	15.04	NOR-based decoder	38.12
2-4LP (14T)	8.015	4-16LP	20.05
2-4 HP(15T)	10.01	4-16 HP	25.09
NAND-based decoder	15.02	NAND-based decoder	34.89
2-4 LPI	11.017	4-16 LPI	19.56
2-4 HPI	13.02	4-16 HPI	24.87
M-GDI AND decoder	5.011	M-GDI AND decoder	13.09
M-GDI OR decoder	6.028	M-GDI OR decoder	15.02



**Figure 8** OR Schematic



**Figure 9** Decoder Schematic



**Figure 10** Decoder Waveform

### 6. CONCLUSION

This paper introduces an efficient and low-power design for decoder circuit. By using modified gate diffusion input (M-GDI) methodology, 2-4 and 4-16 decoders are designed with minimum transistor count, low power, high performance, and minimum delay compared with mixed logic design and conventional CMOS decoders and simulation results are performed in Tanner Tools 90 nm CMOS technology. These decoders are used in the applications where minimum area and less power are required and used as pre-decoders in designing the larger decoders, multiplexers, and combinational circuits. The proposed modified GDI (M-GDI) decoder design excelled existing mixed logic decoder design in all aspects.

## Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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