



Design and Analysis of a Wide-Range Voltage Shifter for IoT and Portable Devices

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KEYWORDS	ABSTRACT
Voltage Level Shifter, Low Power VLSI, Leakage Reduction, 45nm CMOS Technology, Wide Conversion Range, Sub-Threshold Operation	<i>This paper represents an in-depth investigation into the design and evaluation of an ultra-low-leakage, wide-range voltage level shifter tailored for modern System-on-Chip (SoC) architectures. In these systems, diverse modules function across multiple voltage domains to optimize performance and energy consumption, necessitating reliable signal bridging via voltage level shifters (LS). Conventional LS topologies, however, face challenges like elevated leakage currents, diminished output amplitude, and prolonged propagation delays, especially in sub-threshold modes. The proposed LS, realized in 45nm CMOS technology, integrates leakage-suppressing transistors to curtail static dissipation, hysteresis mechanisms to rectify amplitude issues, and low-threshold NMOS elements to boost switching velocity. Simulation data from 45nm CMOS indicate a broad conversion spectrum spanning sub-threshold 0.2V to 1.2V, with notable enhancements in delay minimization and energy conservation relative to traditional designs. This innovative architecture is particularly advantageous for energy-frugal IoT platforms, mobile electronics, and power-optimized VLSI frameworks.</i>

INTRODUCTION

The power budgets of modern integrated systems are increasingly dominated by leakage and standby energy as devices move into deep submicron nodes. Concurrently, the adoption of multiple voltage domains within a single SoC each tuned to the performance needs

of specific blocks is a well established power reduction technique.

Seamless and energy-efficient communication between these domains is necessary enabling technology for such heterogeneous power management. Level Shifters fulfil this role, translating logic levels from a low supply rail

to a higher one and vice versa.

However, achieving this translation at ultra low voltage is non trivial. When input domains operate in the near - threshold or sub-threshold region ($V_{DDL} < 0.5$), the reduced overdrive of MOS transistors, increased sensitivity to process and temperature variation, and the presence of unwanted static current paths lead to unreliable behaviour in the many classical LS topologies. In particular, current-mirror and DCVS based designs can present persistent contention between pull-up and pull-down networks during switching, causing prolonged transitions, partial internal node voltages, and an associated rise in the static and dynamic energy consumption.

For battery powered and always-on devices e.g., IoT nodes, wearable health monitors, and remote sensors standby leakage must be minimized without sacrificing the correctness of voltage translation. To address this dual objective we propose a 45 nm CMOS level shifter that prioritizes ultra-low leakage while maintaining robustness over a wide conversion range. The design integrates an active leakage shut-off, low-threshold discharge devices for speed, and hysteresis aids for swing recovery. In this paper we describe the design rationale, transistor-level architecture, simulation methodology, and results, and we position the contribution with respect to existing approaches.

RELATED WORK

Voltage level shifters are fundamental building blocks in modern VLSI systems that employ multiple voltage domains to reduce over all power consumption. With the continued scaling of CMOS technologies and the widespread adoption of multi-voltage domain architectures, voltage level shifters have become a critical component in low-power VLSI systems. Aggressive voltage scaling is widely used to reduce both dynamic and leakage power; however, it introduces significant challenges for reliable signal translation between low-voltage and high-voltage domains. Recent VLSI research has therefore focused on developing level shifter circuits that operate reliably at ultra-low input voltages while minimizing static and dynamic power dissipation.

Wang et al. [2] proposed an ultra-low-voltage and energy-efficient level shifter incorporating a current limiter and an improved split-controlled inverter. Their design demonstrates reliable operation at very low input

voltages and significantly reduces short-circuit current during switching. While the approach effectively lowers power consumption, the inclusion of additional control circuitry increases design complexity and may impact area efficiency in dense VLSI integrations.

Sivakumar et al. [3] introduced a fast and ultra-low-energy subthreshold level shifter using a split-gate buffer architecture for low-power digital VLSI systems. By improving the pull-up and pull-down switching behavior in the subthreshold region, the proposed design achieves reduced delay and energy per transition. However, the circuit's performance is sensitive to process variations, which can limit robustness in scaled CMOS technologies.

Pappu et al. [4] presented a high-performance and ultra-low-power level shifter designed for digital CMOS circuits. Their work focuses on reducing leakage power while ensuring stable voltage conversion across operating conditions in a 45 nm CMOS process. Although the design achieves low power consumption, reliable full-swing operation at extremely low input voltages remains challenging.

Chandrasekhar et al. [5] proposed a pass-transistor-based split-input level shifter for ultra-low-power VLSI applications. The design supports wide voltage conversion and reduces leakage using multi-threshold CMOS techniques. However, voltage degradation associated with pass-transistor logic may affect robustness under varying load conditions.

PROPOSED LEVEL SHIFTER ARCHITECTURE

The proposed level shifter is designed to convert signals from a low-voltage domain (V_{DDL}) to a high-voltage domain (V_{DDH}) while maintaining ultra low leakage power. The architecture is based on a modified current topology enhanced with additional control elements to improve performance under low-voltage conditions.

3.1 Design Requirements

The key feature of the design is the incorporation of leakage shut-off transistors. Minimisation of leakage power is another critical requirement, as level shifters frequently remain in Low- power mode in multi-voltage architectures. The proposed design targets ultra-low static power dissipation by suppressing unnecessary current paths during steady state operation. This is achieved through appropriate threshold voltage selection

and leakage control techniques that reduce both gate and sub-threshold leakage currents.

The level shifter must also provide robust switching performance with minimal propagation delay. Balanced pull-up and pull-down networks are required to avoid contention and short-circuit currents during voltage transitions. Additionally, the design must ensure full output voltage swing and stable operation across process, voltage, and temperature variations.

3.2 Proposed Architecture Overview

Based on the above design requirements, a leakage-controlled level shifter architecture is proposed to achieve wide-range voltage conversion with improved energy efficiency. The architecture employs a current-mirror-based structure combined with optimised pull-up and pull-down paths to enhance switching speed while suppressing static power dissipation.

Low-threshold NMOS transistors are utilised in the input stage to ensure reliable operation at ultra-low input voltages. To minimise leakage in the output stage, high-threshold devices and leakage shut-off paths are incorporated, effectively isolating the voltage domains during steady-state conditions while allowing fast transitions during switching events.

In addition, voltage hysteresis is integrated into the architecture to improve noise immunity and prevent false switching due to small input fluctuations. Through coordinated operation of the input sensing circuitry and output driving stage, the proposed level shifter achieves full voltage swing, reduced leakage power, and stable performance over a wide range of supply.

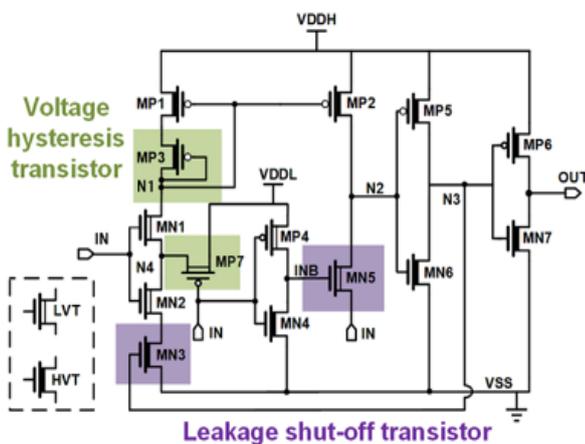


Fig.1 Proposed level shifter

CIRCUIT OPERATION

The operation of the proposed level shifter is explained by analysing the input signal transitions and their impact on the internal nodes and output stage. The architecture ensures reliable voltage translation from the low-voltage domain to the high-voltage domain while suppressing leakage current and maintaining stable output levels.

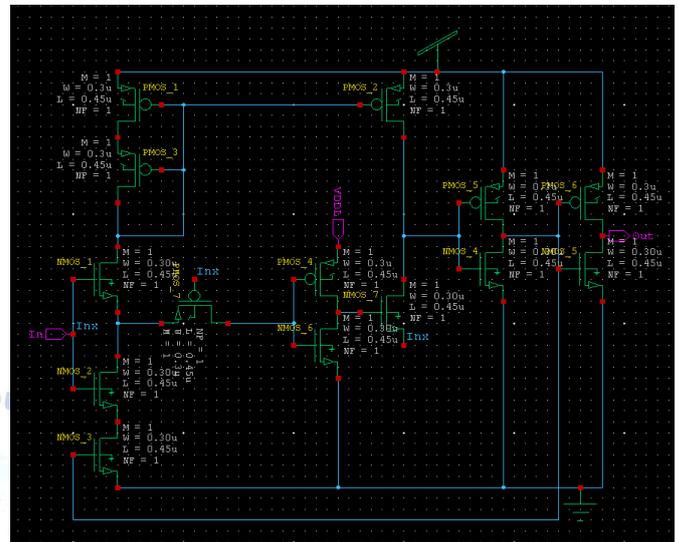


Fig. 2. Schematic diagram of the proposed level shifter

4.1 Low-to-High Input Transition (VDDL rising)

When the input signal transitions from logic low to logic high in the low-voltage domain (VDDL), the low-threshold NMOS transistors in the input stage turn ON, enabling effective discharge of the internal sensing node even at ultra-low input voltages. This action activates the pull-down path through the current mirror-based network, which weakens the competing pull-up path and prevents contention. As a result, the output. After the transition is completed, the leakage shut-off transistors isolate inactive paths, thereby minimising static power dissipation and maintaining a stable output level without continuous current flow.

4.2 High-to-Low Input Transition (VDDL falling)

When the input signal transitions from logic high to logic low, the input NMOS network Turns OFF, allowing the PMOS pull-up network connected to a higher voltage domain to charge the output node. The current-mirror structure enables controlled charging, Reducing short-circuit current and avoiding contention. This results in a stable full-swing logic high at the output, while leakage control devices suppress unnecessary static current in the steady state.

4.3 Timing Delay Analysis

The propagation delay of the proposed level shifter is governed by the charging and discharging of internal nodes and the strength of the pull-up and pull-down networks. The use of low-threshold input devices and reduced contention paths enables faster transitions at low input voltages. Consequently, the proposed design achieves improved timing performance while maintaining ultra-low leakage power.

METHODOLOGY

The methodology begins with identifying the limitations of conventional voltage level shifters operating at ultra-low input voltages. Based on the observations, a leakage-controlled level shifter architecture is developed using current mirror assistance and appropriate device selection. Low-threshold transistors are employed to ensure reliable.

Low voltage operation, while leakage control mechanisms are incorporated to reduce static power, and output voltage swing. Finally, the proposed design is validated through transistor-level simulations to evaluate leakage power, propagation delay, and signal integrity.

SIMULATION

The performance of the proposed level shifter is verified through detailed transistor-level simulations to evaluate voltage conversion accuracy, leakage power and timing behaviour under different operating conditions.

6.1 Simulation Setup

The proposed level shifter is simulated at the transistor level using a standard CMOS technology to validate its functionality and performance. The circuit is implemented in 45nm CMOS technology, and simulations are carried out for both steady-state and transient conditions. The low-voltage input supply (VDDL) is varied over a wide range to examine sub-threshold and near -threshold operation, while the high-voltage supply (VDDH) is maintained at its nominal value

Transient simulations are performed to analyse low-to-high and high-to-low input transitions and verify full output voltage swing. Propagation delay is measured as the time difference between the 50% transition points of the input and output waveforms. Leakage power is

evaluated under static conditions to assess the effectiveness of the leakage reduction mechanism incorporated in the design.

6.2 Software Used for Simulation

All simulations are performed using Tanner EDA tools, which are widely used for transistor-level VLSI circuit analysis. The schematic design and simulations are carried out using S-Edit and T-Spice, respectively. T-Spice is used to perform transient and DC analyses

The simulation environment allows detailed observation of internal node voltages, output waveforms, and current flow paths, facilitating analysis of leakage behaviour and switching performance. The use of Tanner EDA ensures reliable validation of the proposed level shifter architecture.

RESULTS AND DISCUSSION

7.1 Transient Simulation Results

The transient simulation results of the proposed ultra-low-power voltage level shifter are illustrated in Fig. X. The lower waveform represents the low-voltage input signal applied at the VDDL domain, while the corresponding output signal is translated to the higher voltage domain. The input signal switches between 0V and the low supply voltage, and the output follows the input transitions with full voltage swing, indicating a correct level-shifting operation.

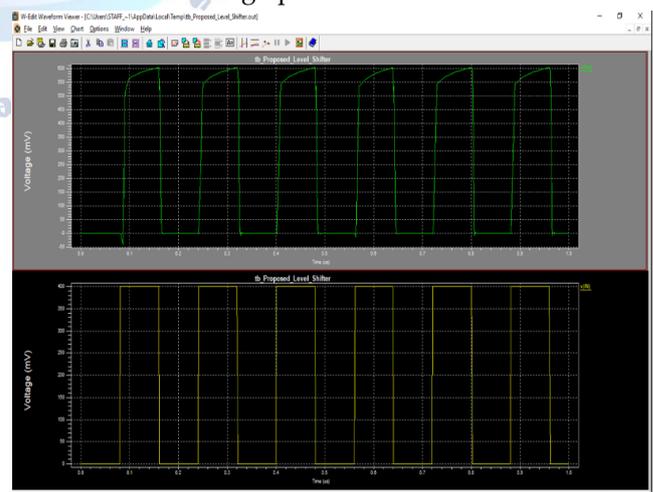


Fig.3 Transient simulation waveforms of the proposed level shifter

7.2 Discussion

From the comparison results, it is evident that the proposed level shifter achieves a favourable balance between delay, power consumption, and circuit complexity. Compared output voltage levels. Although

Kabirpour's design shows lower delay. It suffers from significantly higher power consumption, making it less suitable for ultra-low-power applications.

Table 1. Performance comparison of the proposed levelshifter with existing design

Level shifters	MOSFET count	Technology (nm)	Input Voltage(V)	Delay(ns)	Power consumption(nW)	Output Voltage
Le's	11	45	0.6	9.8365	0.0225	0.6
Kabirpour	8	45	0.4	1.2655	0.1637	1.2
Kim's	11	45	0.5	5.306	0.0291	1.0
Proposed	14	45	0.4	6.2585	0.0196	0.6

Kim's level shifter exhibits moderate delay and power performance, but its reliability reduces at lower input voltages. In contrast, the proposed level shifter operates reliably at an input voltage of 0.4V with controlled leakage power due to optimized transistor sizing and minimized contention paths. These result indicate that the proposed design is well suited for low power VLSI applications such as IoT and energy-constrained systems.

CONCLUSION

This paper presented an ultra-low-power and wide - range voltage level shifter suitable for modern low-voltage VLSI systems. The proposed architecture achieves reliable voltage conversion at reduced input voltage while maintaining low leakage power and acceptable propagation delay. Overall, the proposed level shifter proves to be an efficient solution for energy-constrained applications such as IoT devices, wearable electronics, and low-power digital systems.

FUTURE SCOPE

Future work may focus on implementing the proposed level shifter in advanced CMOS technology nodes to further reduce power and area. The design can be extended to support wider voltage ranges and higher operating frequencies. Additionally, integrating the level shifter into a system-on-chip (SoC) platform and validating it through hardware implementation will help assess real-time performance.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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