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Implementation of Low-Power Carry Save Adder Using a Novel 18-Transistor Hybrid Full Adder

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KEYWORDS

Hybrid Full Adder, Carry Save Adder (CSA), Low Power VLSI, Power-Delay Product (PDP), 18T.

ABSTRACT

In the era of portable electronics, the demand for VLSI designs with improved power-delay characteristics is critical. This paper proposes a novel 1-bit hybrid full adder circuit implemented using eighteen transistors (18T). The design is evaluated based on speed, average power consumption, and power-delay product (PDP) using 180 nm and 90 nm technologies. Furthermore, a four-operand, eight-bit Carry Save Adder (CSA) with a final carry propagate adder is implemented using the proposed full adder. Simulation results demonstrate that the proposed hybrid full adder achieves significantly lower power and energy consumption compared to existing designs, with the 8-bit CSA consuming only 55.24 μW.

1. INTRODUCTION

The rapid growth in the usage of battery-operated portable devices, such as mobile phones and laptops, has created a significant demand for VLSI designs with improved power-delay characteristics. As full adders are the fundamental building blocks of arithmetic units like compressors, comparators, and parity checkers, optimizing their performance is critical for enhancing the overall efficiency of digital systems.

Designers face the challenge of balancing speed, power consumption, and driving capability. Classical designs, such as the standard static CMOS full adder, offer robustness and good driving capabilities but suffer from high input capacitance and reduced speed due to PMOS mobility limitations. Alternative logic styles, such as Complementary Pass-transistor Logic (CPL), provide high-speed operation but consume significant static power due to internal nodes and inverters. Conversely, Transmission Gate Adders (TGA) consume less power but lack driving capability, causing performance degradation when cascaded.

To address these limitations, Hybrid-CMOS logic styles have been developed, utilizing various logic modules to achieve desired performance metrics. However, many existing hybrid designs still struggle

with trade-offs between power consumption and output swing stability.

In this paper, we propose a novel 1-bit hybrid full adder circuit implemented using eighteen transistors (18T). The proposed design utilizes a modified XOR-XNOR cell with a feedback loop to ensure full-swing outputs and adequate driving capability. This design aims to achieve low power and energy consumption compared to existing full adder styles. To validate its performance in practical applications, a four-operand, eight-bit Carry Save Adder (CSA) with a final carry propagate adder is implemented using the proposed full adder. Simulation results in 180 nm and 90 nm technologies demonstrate significant improvements in the power-delay product (PDP).

2. PREVIOUS WORK

The design of full adders has been a subject of extensive research, resulting in a wide range of published architectures. Although these circuits perform the identical logical function, their internal logic structures vary significantly, which directly impacts propagation delay and power consumption. Existing full adder designs can be broadly classified into three categories based on their module-level structures and logical equations.

- **Hybrid-CMOS Full Adder:** This category, discussed in [1], is known for its superior driving capability and ability to provide full-swing output voltage. However, a major limitation of this design style is its higher power consumption compared to other architectures.
- **Double Pass-Transistor Logic (DPL):** The DPL logic style [2] was developed specifically to optimize the power-delay product (PDP) . despite this optimization, DPL circuits often suffer from high power consumption and area overhead due to a large transistor count, typically requiring 28 transistors (28T).
- **Kumar's Full Adder:** The design proposed by Kumar [3] addresses some efficiency concerns but introduces a significant drawback regarding speed. The propagation delay of the carry signal is notably higher in this design due to the sharing of the carry input signal across multiple modules.

These limitations in existing designs highlight the need for a novel architecture that balances power consumption, delay, and driving capability.

3. 1-BIT FULL ADDER CELL

The proposed full adder architecture is structured into three distinct modules[1]. Module 1 functions as a combined XOR and XNOR gate, generating the intermediate signals required to drive the subsequent stages[2]. Module II and Module III are responsible for producing the Sum and Carry (Cout) outputs, respectively[3].

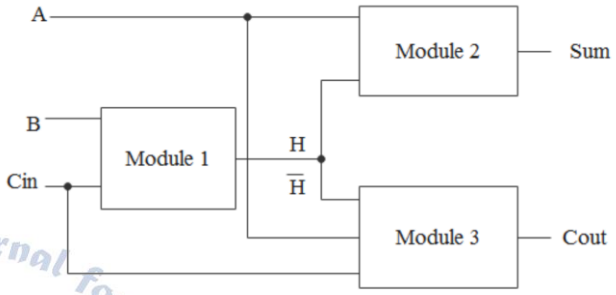

Fig. 1. Schematic structure of hybrid full adder [4]

The boolean expressions governing the Sum and Carry outputs are defined as:

$$Sum = H\overline{C_{in}} + \overline{H}C_{in} = A \oplus B \oplus C_{in} \quad (1)$$

$$Cout = HC_{in} + \overline{H}A \quad (2)$$

- **A. Module-1: Modified XOR-XNOR Cell**

Module 1 generates the intermediate signals H and Hbar which drive the remaining modules[4] as shown in Fig. 1. The design is based on a modified three-transistor XOR-XNOR gate, enhanced with an inverter connected to input B[5].

To address the issue of weak logic levels typical in such designs, a feedback loop is incorporated[6]. This loop utilizes pMOS (Mpf) and nMOS (Mnf) transistors to restore the output voltage levels:

- **Case A=B=0:** The modified XOR output H initially produces a weak logic 0 (VTP). However, this weak signal turns ON Mpf in the feedback loop, which passes a strong logic 1 to the gate of Mnf, turning it ON. Consequently, a perfect logic 0 is pulled down at the H output.
- **Case A=B=1:** A weak logic 1 (VDD - VTN) appears at H. This signal turns ON Mnf, passing logic 0 to the complementary output H. This, in turn, activates Mpf, pulling H to a perfect logic 1[8888].

This feedback mechanism ensures that Module 1 provides full-swing outputs capable of driving Modules 2 and 3 without voltage degradation[9].

- **B. Module-2: Sum Generation**

The second module generates the Sum output using the intermediate signal H and the input carry Cin, where Sum = Cin \oplus H [10]. This module is implemented using the Gate Diffusion Input (GDI) design style[11].

The GDI technique allows for the generation of full-swing outputs for all input combinations[12]. Although GDI XOR gates typically require an inverter to provide a complementary input, this design leverages the \bar{H signal already generated in Module 1[13]. Consequently, Module 2 requires only four transistors, significantly reducing the transistor count[14].

- **C. Module-3: Carry Generation**

Module 3 is a four-transistor multiplexer that generates the carry output Cout[15]. It utilizes pass transistor logic with inputs A and Cin, controlled by the select line H[16].

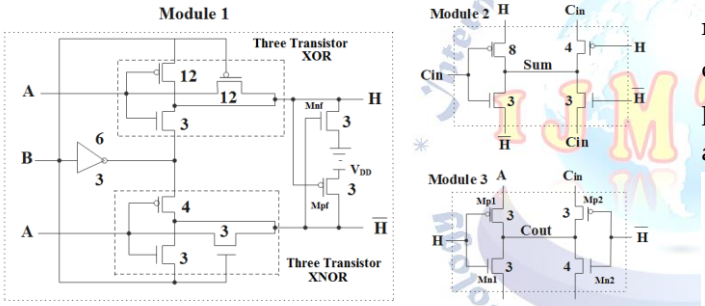

Fig. 2. 1-bit hybrid full adder circuit

- **When H=0 (A=B):** Transistors Mp1 and Mn2 turn on. If A=0, logic 0 is passed to Cout.
- **When H=1 (A≠B):** Transistors Mp2 and Mn1 turn on. If Cin=1, logic 1 is passed to Cout.

Since one pMOS and one nMOS transistor conduct for each input combination, the circuit eliminates the threshold voltage drop, ensuring a strong logic 1 and perfect logic 0 at the output [17]. This module also requires only four transistors, contributing to the overall area efficiency of the design. The complete circuit diagram of the 1-bit Hybrid Full adder cell circuit diagram is shown in Fig. 2. Module 1 is an XORXNOR cell.

4. PERFORMANCE ANALYSIS OF HYBRID FULL ADDER

The performance of the proposed hybrid full adder was evaluated through simulations at both 180 nm and 90 nm technology nodes. The simulations were conducted at a supply voltage of 1.8 V for 180 nm and 1.2 V for 90 nm. The hybrid full adder simulations were carried out in both the technology nodes, as shown in Fig 3.

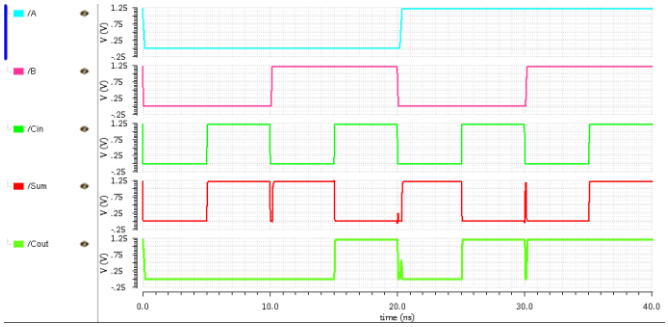

Fig. 3. Simulated output of hybrid full adder

Simulation results indicate that the proposed design minimizes glitches often caused by signal arrival time differences. A comparative analysis of delay, average power consumption, and Power-Delay Product (PDP) against existing designs is presented below.

TABLE I
PERFORMANCE OF FULL ADDERS IN 180 nm

Full Adder	Delay (ps)	Average Power (μW)	PDP (fJ)	Transistor Count	Refer-ence
Hybrid CMOS	252.3	5.978	1.508	24	[1]
DPL FA	212.3	11.18	2.37	22	[2]
New Hybrid	224	4.156	0.931	16	[7]
Proposed FA	231.3	3.353	0.8165	18	[Present]

TABLE II
PERFORMANCE OF FULL ADDERS IN 90 nm

Full Adder	Delay (ps)	Average Power (μW)	PDP (fJ)	Transistor Count	Refer-ence
Hybrid CMOS	143	6.21	0.888	24	[1]
DPL FA	254	7.34	2.37	22	[2]
New Hybrid	91.3	1.1766	0.107	16	[7]
Proposed FA	85.22	1.104	0.0941	18	[Present]

As observed in Tables I and II, the proposed full adder demonstrates lower average power consumption and improved PDP compared to existing Hybrid CMOS and DPL designs across both technologies.

5. FOUR OPERAND EIGHT-BIT CARRY SAVE ADDER USING THE PROPOSED FULL ADDER

To demonstrate the applicability of the proposed cell in larger arithmetic circuits, a four-operand, eight-bit Carry Save Adder (CSA) with a final carry propagation adder was implemented[23].

Architecture

The CSA architecture consists of four operands (A, B, C, D) arranged in columns, where each operand comprises eight bits (A_0 to A_7) [24]. The computation is distributed across blocks implemented using the proposed 1-bit hybrid full adder:

First Stage: The first block in a column accepts inputs (A_i, B_i, C_i). It produces a Sum which serves as an input to the second block in the same column, and a Carry-out which propagates to the adjacent block on the left [25].

Second Stage: The second block accepts the fourth operand (D_i), the Sum from the first block, and the Carry from the previous stage. It generates the corresponding Sum (S_i) and a Carry that propagates to the immediate left column [26].

This hierarchical structure allows for the efficient reduction of partial products, producing a final Sum and Carry output for the 8-bit addition.

6. PERFORMANCE OF FOUR OPERAND EIGHT-BIT CARRY SAVE ADDER

The block-level simulation of the CSA is shown in Fig.5. The performance of eight-bit, 4-operand CSA, was evaluated in 180 and 90 nm technologies. Table III shows the performance of newly implemented CSA in terms of power consumption compared to the existing ones. The delay is also increased by increasing the number of stages because the 1-bit full adder carry structure contains only pass transistors to produce output. This problem can be avoided by adding appropriate buffers between the stages [7].

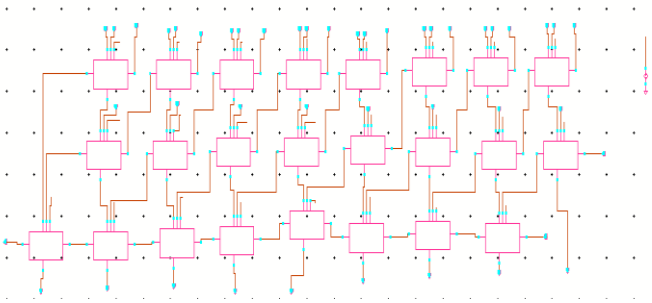

Fig. 5. Four operand eight-bit CSA implementation

TABLE III
PERFORMANCE OF FOUR OPERAND EIGHT-BIT CSA IN 90 nm TECHNOLOGY

CSA Design Using:	Power (μW)	Reference
Hybrid-CMOS FA	158.4	[1]
Proposed FA	112.2	Present

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7. CONCLUSION

An 18T hybrid full adder is proposed. The simulations were done in 180 and 90 nm technology using the Cadence Virtuoso tool in 1.8 and 1.2 V supply voltage. The full adder performances are analysed in both the technology nodes. The present full adder circuit has only 3.353 _W power consumption and 231.3 ps delay at 180 nm, the power reduced to 1.104 _W, and delay to 85.22 ps in case of 90 nm. The power-delay products are significantly improved by 0.81648 fJ and 0.09408 fJ in 180 and 90 nm, which is better than the existing 1-bit full adder circuits. An eight-bit, four operands carry-save adder implemented using our eighteen transistor hybrid full adder shows low-power consumption, i.e., only 112.2 _W, which is far better than the CSA implemented using the other existing 1-bit full adder design styles.

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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